ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.
7/93

MAXIM

Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

General Description

The MAX915/MAX916 high-speed, single and dual TTL voltage comparators eliminate oscillation by separating the comparator input and output stages with a negative edge-triggered master/slave flip-flop. Comparator propagation delay is typically 6ns, and is insensitive to input overdrive. The MAX915 and MAX916 resolve input signals as small as 2mV and 3mV, respectively.

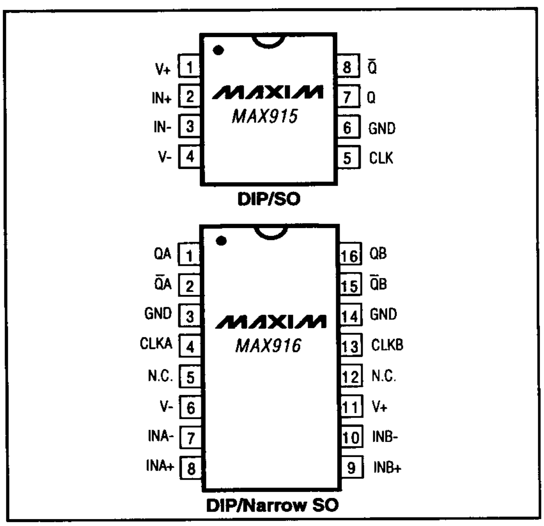
These comparators operate either from dual supplies or from a single +5V supply. The input common-mode voltage range extends below the negative supply rail, allowing ground-sensing applications with a single +5V supply.

The MAX915 is a single TTL comparator, available in 8-pin DIP and SO packages. The MAX916 is a dual version available in 16-pin DIP and SO packages. For equivalent devices with complementary ECL outputs and 2ns propagation delay, see the single/dual MAX905/MAX906.

Applications

High-Speed A/D Converters
High-Speed Line Receivers
Peak Detectors
Threshold Detectors
High-Speed Triggers
Synchronous Data Discriminators

Pin Configurations



Features

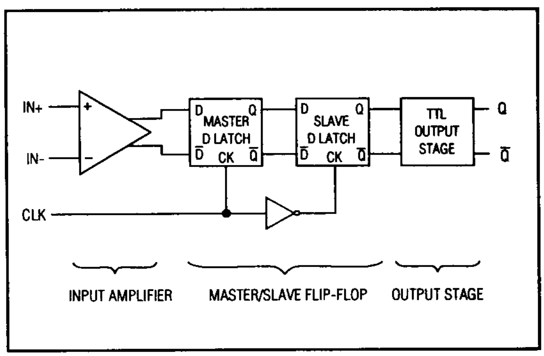
- ♦ **Oscillation Free: Clocked Architecture**
- ♦ **6ns Propagation Delay**
- ♦ **Propagation Delay Insensitive to Overdrive**
- ♦ **Single +5V or Dual ±5V Supplies**
- ♦ **2mV Input Resolution (MAX915)**
- ♦ **Input Range Includes Negative Supply Rail**
- ♦ **Low Power: 14mA (70mW) per Comparator, +5V**
- ♦ **1.5ns Setup Time with 5mV Overdrive**
- ♦ **No Minimum Requirement for Input Signal Slew Rate**
- ♦ **Complementary TTL Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX915CPA	0°C to +70°C	8 Plastic DIP
MAX915CSA	0°C to +70°C	8 SO
MAX915C/D	0°C to +70°C	Dice*
MAX915EPA	-40°C to +85°C	8 Plastic DIP
MAX915ESA	-40°C to +85°C	8 SO
MAX915MJA	-55°C to +125°C	8 CERDIP
MAX916CPE	0°C to +70°C	16 Plastic DIP
MAX916CSE	0°C to +70°C	16 Narrow SO
MAX916C/D	0°C to +70°C	Dice*
MAX916EPE	-40°C to +85°C	16 Plastic DIP
MAX916ESE	-40°C to +85°C	16 Narrow SO

* *Contact factory for dice specifications.*

Functional Diagram



Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V+ to GND) ....+6V
Negative Supply Voltage (V- to GND)......................................-6V
Differential Input Voltage ....(V- - 0.3V) to (V+ + 0.3V)
Common-Mode Input Voltage ....(V- - 0.3V) to (V+ + 0.3V)
Clock Input Voltage..........................(GND - 0.3V) to (V+ + 0.3V)
Output Short-Circuit Duration
To V+, GND ....Continuous
To V- 10sec
Output Current (Q or $\bar{Q}$)..20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C).................471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C).........640mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C)..696mW
Storage Temperature Range ....-65°C to +150°C
Junction Temperature Range ....-65°C to +170°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = 0V	MAX915		0.5	1.0	mV
			MAX916		0.5	1.5	
Input Bias Current	I_B	I_B+ or I_B-			5	10	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			0.2	1.0	µA
Input Referred Noise Voltage	e_n	(Note 1)			600	900	µV
Input Common-Mode Range	V_{CMR}			V- - 0.1		V+ - 2.2	V
Common-Mode Rejection Ratio	CMRR	(Note 2)			90	120	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)			60	120	µV/V
Output High Voltage	V_{OH}	(Note 4)		2.8	3.5		V
Output Low Voltage	V_{OL}	(Note 4)			0.3	0.4	V
Clock Input Voltage High	V_{IH}			2			V
Clock Input Voltage Low	V_{IL}					0.8	V
Clock Input Current High	I_{IH}				0.5	10	µA
Clock Input Current Low	I_{IL}				2.5	10	µA
Positive Supply Current (Note 5)	I+	MAX915			14	18	mA
		MAX916			28	36	
Negative Supply Current (Note 5)	I-	MAX915			3	4	mA
		MAX916			6	8	
Power Dissipation (Note 5)	PD	V+ = 5.25V, V- = -5.25V	MAX915		85	115	mW
			MAX916		170	230	
Propagation Delay (Notes 6,7)	t_{PD+}	Q, $\bar{Q}$ rising			6	8	ns
	t_{PD-}	Q, $\bar{Q}$ falling			6	8	
Propagation-Delay Skew	t_{SKEW}	(Notes 6, 7, 8)			0.5	3.0	ns
Clock Setup Time (Notes 8,9)	t_{SU}	V_{OD} = 5mV			1.5		ns
		V_{OD} = 10mV			1.0	2.0	

ELECTRICAL CHARACTERISTICS

($V+ = +5V$, $V- = -5V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_{CM} = 0V$	MAX915		0.5	1.4	mV
			MAX916		0.5	2.5	
Input Bias Current	I_B	I_{B+} or I_{B-}			5	15	µA
Input Offset Current	I_{OS}	$V_{CM} = 0V$			0.2	2.0	µA
Input Referred Noise Voltage	e_n	(Note 1)			600	900	µV
Input Common-Mode Range	V_{CMR}			V- - 0.1		V+ - 2.2	V
Common-Mode Rejection Ratio	CMRR	(Note 2)			90	150	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)			60	150	µV/V
Output High Voltage	V_{OH}	(Note 4)		2.8	3.5		V
Output Low Voltage	V_{OL}	(Note 4)			0.3	0.4	V
Clock Input Voltage High	V_{IH}			2			V
Clock Input Voltage Low	V_{IL}					0.8	V
Clock Input Current High	I_{IH}				0.5	15	µA
Clock Input Current Low	I_{IL}				2.5	15	µA
Positive Supply Current (Note 5)	I+	MAX915			14	22	mA
		MAX916			28	44	
Negative Supply Current (Note 5)	I-	MAX915			3	6	mA
		MAX916			6	12	
Power Dissipation (Note 5)	PD	V+ = 5.25V, V- = -5.25V	MAX915		85	150	mW
			MAX916		170	300	
Propagation Delay (Notes 6, 7)	t_{PD+}	Q, $\overline{Q}$ rising	MAX91_C		6	10	ns
			MAX91_E		6	12	
			MAX91_M		6	15	
	t_{PD-}	Q, $\overline{Q}$ falling	MAX91_C		6	10	
			MAX91_E		6	12	
			MAX91_M		6	15	
Propagation-Delay Skew	t_{SKEW}	(Notes 6, 7, 8)			0.5	4.0	ns
Clock Setup Time (Notes 8, 9)	t_{SU}	$V_{OD} = 5mV$			1.5		ns
		$V_{OD} = 10mV$			1.0	2.0	

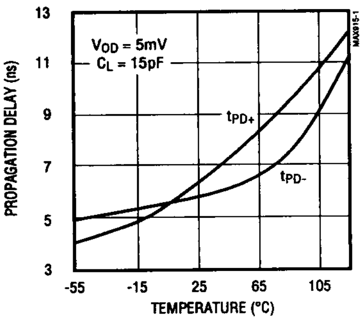
Note 1: Guaranteed by design. Input referred noise voltage uncertainty is specified over the full bandwidth of the device.
Note 2: Common-mode rejection ratio is tested over the full common-mode range. The common-mode range for dual-supply operation is from (V- - 0.1V) to (V+ - 2.2V). The common-mode range for single-supply operation is from -0.1V to (V+ - 2.2V).
Note 3: Tested for 4.75V < V+ < 5.25V and -5.25V < V- < 0V.
Note 4: TTL output voltage high and low tested with V+ = 4.75V, $I_{OH} = 4mA$, $I_{OL} = 8mA$.
Note 5: I+, I-, and PD tested for worst-case condition of V+ = 5.25V and V- = -5.25V. Output not loaded.
Note 6: Guaranteed by design. Measured in a high-speed fixture with $C_L = 15pF$, $I_Q = 2mA$. See Figure 1 for timing parameter definitions. Guaranteed for both single- and dual-supply operation.
Note 7: Propagation delay measured with an input signal of 100mV, with 5mV overdrive.
Note 8: Propagation delay skew is defined as the difference in t_{PD} for the complementary outputs, Q and $\overline{Q}$ (see Figure 1).

Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

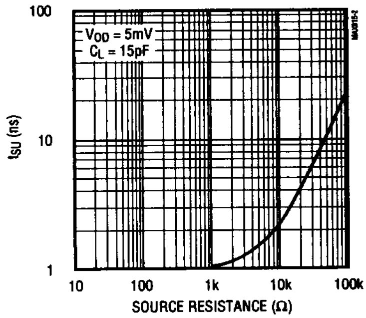
Typical Operating Characteristics

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

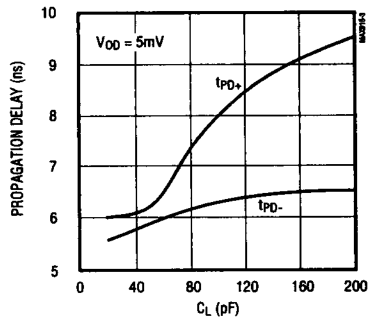
PROPAGATION DELAY vs. TEMPERATURE



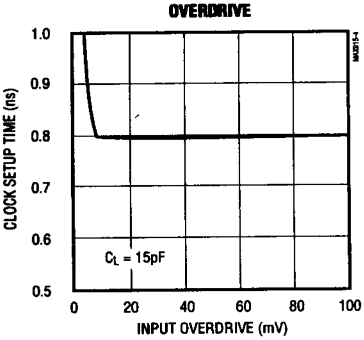
CLOCK SETUP TIME vs. SOURCE RESISTANCE



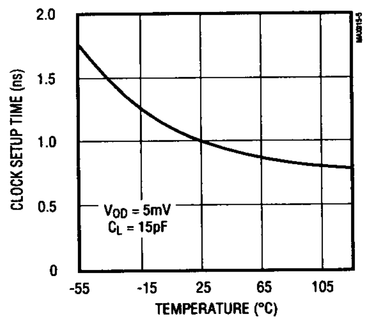
PROPAGATION DELAY vs. CAPACITIVE LOAD



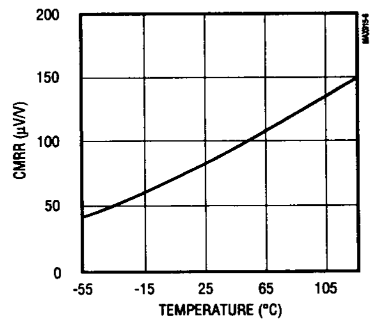
CLOCK SETUP TIME vs. INPUT OVERDRIVE



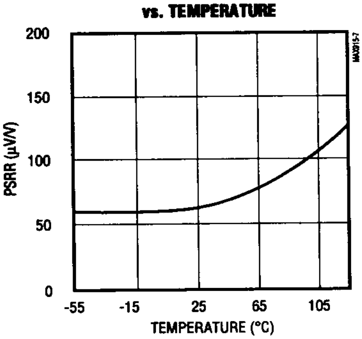
CLOCK SETUP TIME vs. TEMPERATURE



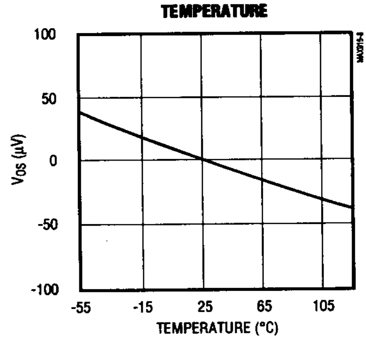
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



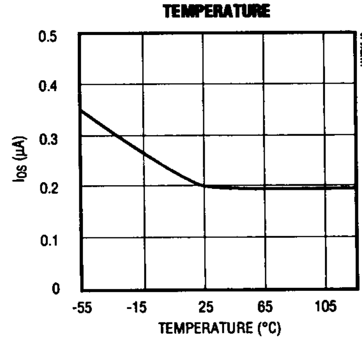
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



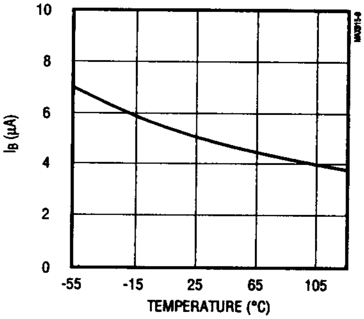
INPUT OFFSET CURRENT vs. TEMPERATURE



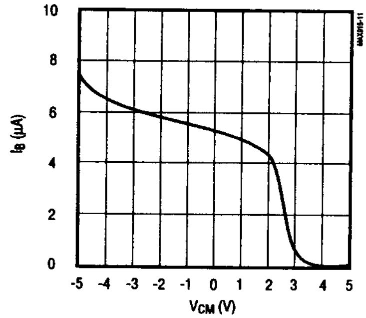
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

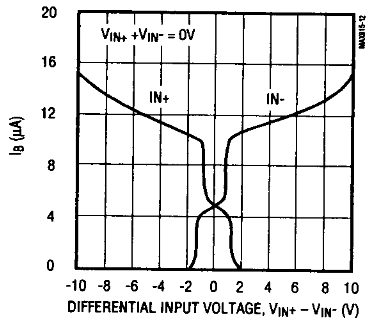
INPUT BIAS CURRENT vs. TEMPERATURE



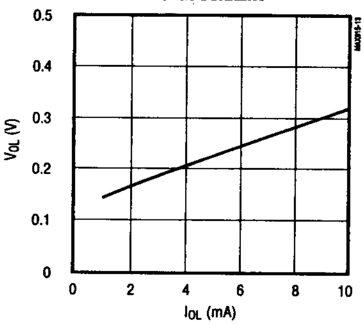
INPUT BIAS CURRENT vs. COMMON-MODE INPUT VOLTAGE



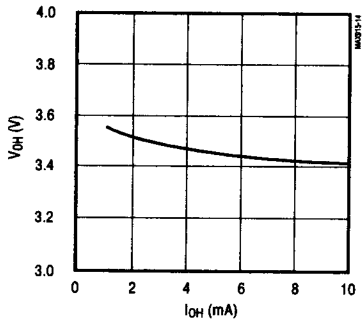
INPUT BIAS CURRENTS vs. DIFFERENTIAL INPUT VOLTAGE



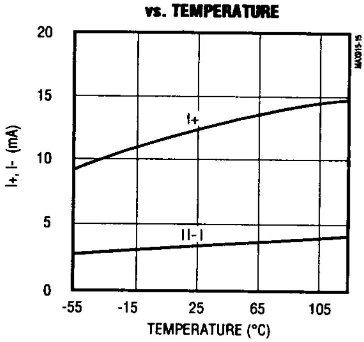
OUTPUT VOLTAGE LOW vs. SINK CURRENT



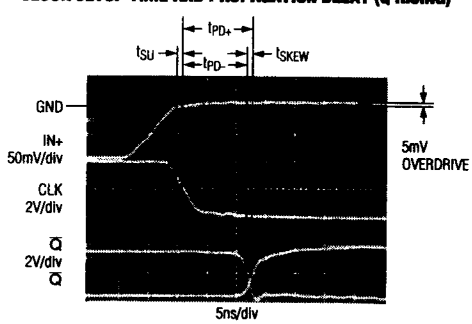
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT



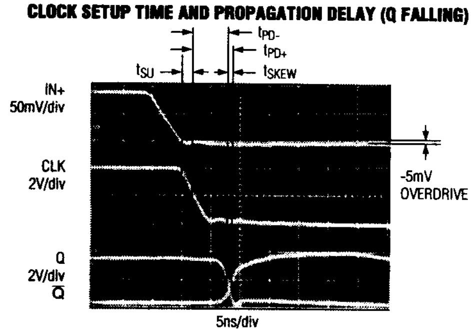
SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE



CLOCK SETUP TIME AND PROPAGATION DELAY (Q RISING)



CLOCK SETUP TIME AND PROPAGATION DELAY (Q FALLING)



Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

Pin Descriptions

MAX915		
PIN	**NAME**	**FUNCTION**
1	V+	Positive Supply
2	IN+	Noninverting Input
3	IN-	Inverting Input
4	V-	Negative Supply. Connect to GND for single-supply operation.
5	CLK	Clock Input
6	GND	Ground
7	Q	TTL Output
8	$\overline{Q}$	Complementary TTL Output

MAX916		
PIN	**NAME**	**FUNCTION**
1	QA	TTL Output, Channel A
2	$\overline{QA}$	Complementary TTL Output, Channel A
3	GND	Ground
4	CLKA	Clock Input, Channel A
5, 12	N.C.	No Connect. Not internally connected.
6	V-	Negative Supply. Connect to GND for single-supply operation.
7	INA-	Inverting Input, Channel A
8	INA+	Noninverting Input, Channel A
9	INB+	Noninverting Input, Channel B
10	INB-	Inverting Input, Channel B
11	V+	Positive Supply
13	CLKB	Clock Input, Channel B
14	GND	Ground
15	$\overline{QB}$	Complementary TTL Output, Channel B
16	QB	TTL Output, Channel B

Detailed Description

The MAX915 (single) and MAX916 (dual) are very high-speed TTL-compatible comparators. Each has an internal negative edge-triggered master/slave D flip-flop, and complementary TTL outputs. Unlike other TTL comparators, this architecture breaks the input-to-output signal path to accomplish the following:

1) Prevent oscillations caused by unwanted parasitic feedback when the comparator is in its linear region. No minimum input slew rate is required.
2) Maintain a constant propagation delay with varying input overdrive.

The comparator can be divided into three stages, as shown in the *Functional Diagram:*

1) Input Amplifier
2) Master/Slave D Flip-Flop
3) TTL Output Stage.

Input Amplifier

The comparator input amplifier is fully differential. Input offset voltage is trimmed to less than 1.0mV (MAX915) or 1.5mV (MAX916) at +25°C. Input common-mode range extends from 100mV below the negative supply rail (V-) to 2.2V below the positive supply (V+). Total common-mode input voltage range is 7.9V when operating from ±5V supplies.

The input amplifier has no built-in hysteresis. External resistors should not be connected with the aim of creating hysteresis. The master/slave flip-flop makes hysteresis unnecessary, and impossible to add externally.

Resolution

A comparator's ability to resolve small signal differences—its resolution—is affected by various factors. The most significant of these are: input offset voltage (V_{OS}), input referred noise (e_n), common-mode rejection error, and power-supply rejection error. If the source has a high impedance, input bias and offset currents may also impact resolution. Avoid unbalanced source impedances.

The MAX915 can compare input signals as small as 2.0mV over the entire common-mode voltage range. Similarly, the MAX916 can resolve input signals of less than 3.0mV (see Table 1).

Master/Slave D Flip-Flop

The negative edge-triggered master/slave D flip-flop incorporates two D latches, which makes propagation delay independent of input overdrive (V_{OD}). When open, the master latch samples the output of the input amplifier; when closed, it holds the sampled data. When open, the slave latch samples the output of the master latch; when closed, it holds the sampled data. The master and slave latches are open on opposite phases of the clock, preventing a direct path from input to output at all times. This makes the MAX915 and MAX916 different from comparators with simple output latches, and delivers high-speed performance without oscillations, even with slow-moving input signals.

The input amplifier continuously monitors the input signal. The master latch samples the output of the input amplifier when the clock is high. The data is held by the master latch and is transferred to the slave latch only on the clock's falling edge. The TTL outputs do not change on the clock's rising edge.

Clock Cycle

When the clock is high, the master stage is transparent, and the data at the slave output is latched. On the clock's falling edge, the input data is latched into the master stage, just before the slave stage becomes transparent and the new data becomes valid at the output. On the clock's rising edge, the slave latches the data at its input (which is also present at the flip-flop's output), just before the master becomes transparent to new data

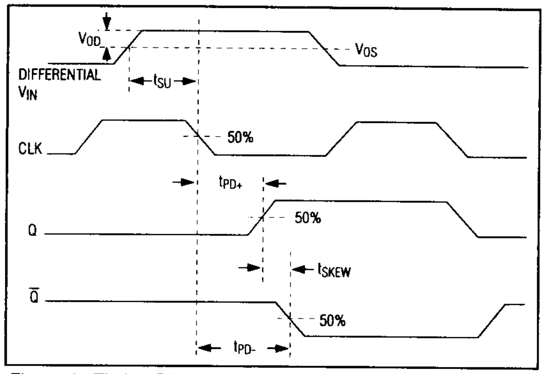


Figure 1. Timing Diagram

at its input. Thus the comparator's inputs are sampled and the new data is transferred to the TTL outputs on the falling edge of the clock.

TTL Output Stage

The complementary TTL outputs can drive high-speed Schottky TTL with a fan-out of four.

Applications Information

Maximum Clock Rate

The maximum permitted clock rate exceeds 50MHz and is a function of the device's propagation delay. The maximum output toggle rate is half the clock frequency because the comparator triggers only on the falling edge of each clock cycle.

Table 1. Input-Referred Error/ Resolution

TEMPERATURE	ERROR/RESOLUTION	MAX915	MAX916	UNITS
T_A = +25°C	RMS error	1.6	2.0	mV
	Worst-case error	2.9	3.4	mV
	R_{SOURCE}*	2.9	3.4	kΩ
T_A = T_{MIN} to T_{MAX}	RMS error	2.0	3.0	mV
	Worst-case error	3.9	4.9	mV
	R_{SOURCE}*	2.0	2.5	kΩ

*R_{SOURCE} is the balanced source resistance that will contribute the same input-referred error as the sum of the worst-case errors from the other four sources (V_{OS}, CMRR, e_n, PSRR)

Ultra High-Speed, High-Resolution, Single-/Dual-Supply TTL Comparators

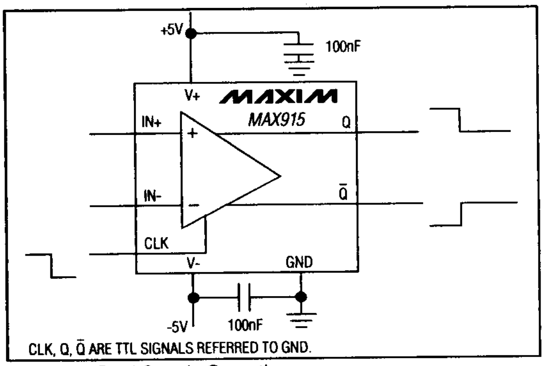


Figure 2. Dual-Supply Operation

Power Supplies

The MAX915/MAX916 are tested while operating from ±5V supplies, providing an input common-mode voltage range (V_{CMR}) of 7.9V (-5.1V to +2.8V) (see Figure 2). Operation from a single +5V supply provides a V_{CMR} from -0.1V to +2.2V below V+ (-0.1V to +2.8V). Connect V- to GND for single-supply operation (see Figure 3).

The V+ supply provides power to the analog input stage and to the digital circuitry, whereas the V- supply only powers the analog section. Pay special attention to bypassing the V+ pin if the V+ supply is noisy.

Input Slew Rate

The MAX915/MAX916's master/slave architecture eliminates the minimum input slew-rate requirement common to standard comparator architectures. As long as the comparator is clocked after the minimum data-to-clock setup time requirement, and the input is greater than the comparator's total DC error, the output will be valid without oscillations. It is not necessary to bypass the input, even if the input signal is very slow moving.

Board Layout and Bypassing

As with all high-speed components, careful high-speed board layout and bypassing are essential for optimal performance; although forgiving, the clocked architecture is not a substitute for good layout and decoupling. A printed circuit board with an unbroken ground plane is recommended. Pay close attention to the bandwidth of the bypass components, and keep ground leads short. Avoid sockets; solder the IC and other components directly to the board to minimize unwanted parasitic capacitance.

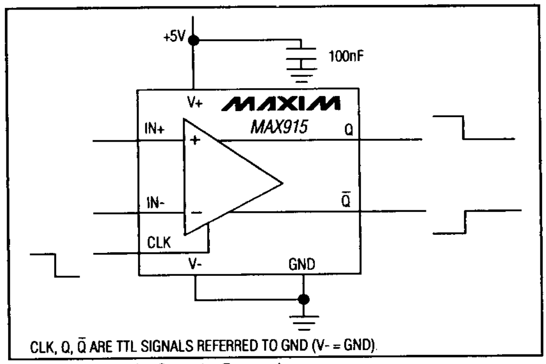
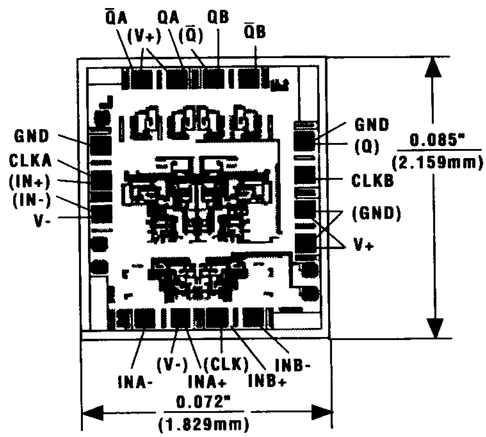


Figure 3. Single-Supply Operation

Bypass V+ and V- to GND with 100nF ceramic capacitors placed very close to the IC supply pins. Keep the leads of through-hole capacitors as short as possible. Do not connect bypass capacitors directly from V+ to V-.

Chip Topography



( ) INDICATE MAX915 CALLOUTS.

TRANSISTOR COUNT: MAX915–82; MAX916–164;

SUBSTRATE CONNECTED TO V-.