19-2878; Rev 0; 7/03

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

MAX9394/MAX9395

General Description

The MAX9394/MAX9395 consist of a 2:1 multiplexer and a 1:2 demultiplexer with loopback. The multiplexer section (channel B) accepts two low-voltage differential signaling (LVDS) inputs and generates a single LVDS output. The demultiplexer section (channel A) accepts a single LVDS input and generates two parallel LVDS outputs. The MAX9394/MAX9395 feature a loopback mode that connects the input of channel A to the output of channel B and connects the selected input of channel B to the outputs of channel A.

Three LVCMOS/LVTTL logic inputs control the internal connections between inputs and outputs, one for the multiplexer portion of channel B (BSEL), and the other two for loopback control of channels A and B (LB_SELA and LB_SELB). Independent enable inputs for each differential output pair provide additional flexibility.

Fail-safe circuitry forces the outputs to a differential low condition for undriven inputs or when the common-mode voltage exceeds the specified range. The MAX9394 provides high-level input fail-safe detection for HSTL, LVDS, and other GND-referenced differential inputs. The MAX9395 provides low-level fail-safe detection for CML, LVPECL, and other V_{CC}-referenced differential inputs.

Ultra low $91ps_{P-P}$ (max) pseudorandom bit sequence (PRBS) jitter ensures reliable communications in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery, or serializers and deserializers. The high-speed switching performance guarantees 1.5GHz operation and less than 87ps (max) skew between channels.

LVDS inputs and outputs are compatible with the TIA/EIA-644 LVDS standard. The LVDS outputs drive 100Ω loads. The MAX9394/MAX9395 are offered in 32-pin TQFP and 28-pin thin QFN packages and operate over the extended temperature range (-40°C to +85°C).

Applications

High-Speed Telecom/Datacom Equipment

Central Office Backplane Clock Distribution

DSLAM

Protection Switching

Fault-Tolerant Systems

Pin Configurations and Functional Diagram appear at end of data sheet.

Features

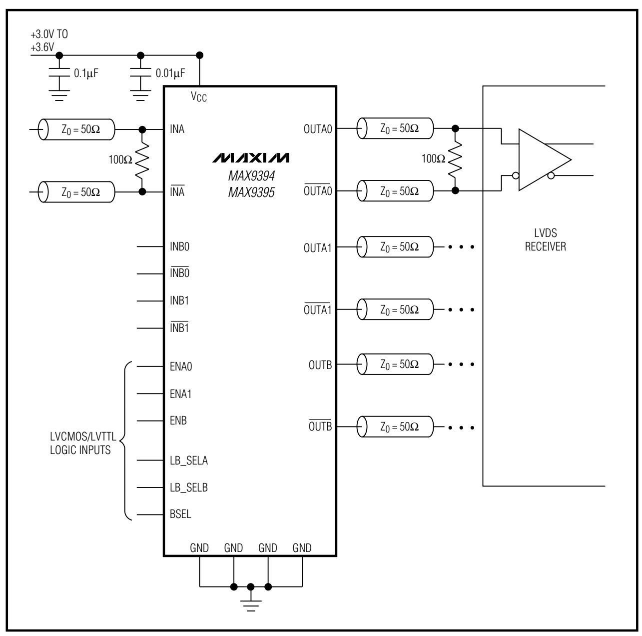
- ♦ **Guaranteed 1.5GHz Operation with 250mV Differential Output Swing**
- ♦ **Simultaneous Loopback Control**
- ♦ **$2ps_{(RMS)}$ (max) Random Jitter**
- ♦ **AC Specifications Guaranteed for 150mV Differential Input**
- ♦ **Signal Inputs Accept Any Differential Signaling Standard**
- ♦ **LVDS Outputs for Clock or High-Speed Data**
- ♦ **High-Level Input Fail-Safe Detection (MAX9394)**
- ♦ **Low-Level Input Fail-Safe Detection (MAX9395)**
- ♦ **+3.0V to +3.6V Supply Voltage Range**
- ♦ **LVCMOS/LVTTL Logic Inputs**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9394EHJ	-40°C to +85°C	32 TQFP
MAX9394ETI*	-40°C to +85°C	28 Thin QFN
MAX9395EHJ	-40°C to +85°C	32 TQFP
MAX9395ETI*	-40°C to +85°C	28 Thin QFN

**Future product—contact factory for availability.*

Typical Operating Circuit



2:1 Multiplexers and 1:2 Demultiplexers with Loopback

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +4.1V
IN_ _, $\overline{IN\_\_}$, OUT_ _, $\overline{OUT\_\_}$, EN_ _, _SEL, LB_SEL_
to GND..........-0.3V to (V_{CC} + 0.3V)
IN_ _ to $\overline{IN\_\_}$..........±3V
Short-Circuit Duration (OUT_ _, $\overline{OUT\_\_}$) ....Continuous
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFP (derate 13.1mW/°C above +70°C)........1047mW
28-Pin 5mm x 5mm Thin QFN
(derate 20.8mW/°C above +70°C)..........1667mW
Junction-to-Ambient Thermal Resistance in Still Air
32-Pin TQFP..........+76.4°C/W
28-Pin 5mm x 5mm Thin QFN..........+48°C/W
Junction-to-Case Thermal Resistance
28-Pin 5mm x 5mm Thin QFN..........+2°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..........+150°C
Storage Temperature Range ....-65°C to +150°C
ESD Protection (Human Body Model)
(IN_ _, $\overline{IN\_\_}$, OUT_ _, $\overline{OUT\_\_}$, EN_ _, SEL_, LB_SEL_) ..±2kV
Soldering Temperature (10s)..........+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, EN_ _ = V_{CC}, V_{CM} = +0.05V to (V_{CC} - 0.6V) (MAX9394), V_{CM} = +0.06V to (V_{CC} - 0.05V) (MAX9395), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, T_A = +25°C.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVCMOS/LVTTL INPUTS (EN_ _, BSEL, LB_SEL_)							
Input High Voltage	V_{IH}			2.0		V_{CC}	V
Input Low Voltage	V_{IL}			0		0.8	V
Input High Current	I_{IH}	V_{IN} = +2.0V to V_{CC}		0		20	µA
Input Low Current	I_{IL}	V_{IN} = 0V to +0.8V		0		10	µA
DIFFERENTIAL INPUTS (IN_ _, $\overline{IN\_\_}$)							
Differential Input Voltage	V_{ID}	$V_{ILD} \geq$ 0V and $V_{IHD} \leq V_{CC}$, Figure 1		0.1		3.0	V
Input Common-Mode Range	V_{CM}	MAX9394		0.05		V_{CC} - 0.6	V
		MAX9395		0.6		V_{CC} - 0.05	
Input Current	$I_{IN\_\_}$, $I_{\overline{IN\_\_}}$	MAX9394	$\lvert V_{ID}\rvert \leq$ 3.0V	-75		10	µA
		MAX9395	$\lvert V_{ID}\rvert \leq$ 3.0V	-10		100	
LVDS OUTPUTS (OUT_ _, $\overline{OUT\_\_}$)							
Differential Output Voltage	V_{OD}	R_L = 100Ω, Figure 2		250	350	450	mV
Change in Magnitude of V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 2			1.0	50	mV
Offset Common-Mode Voltage	V_{OS}	Figure 2		1.125	1.25	1.375	V
Change in Magnitude of V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 2			1.0	50	mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, EN_ _ = V_{CC}, V_{CM} = +0.05V to (V_{CC} - 0.6V) (MAX9394), V_{CM} = +0.06V to (V_{CC} - 0.05V) (MAX9395), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, |V_{ID}| = 0.2V, V_{CM} = +1.2V, T_A = +25°C.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current (Output(s) Shorted to GND)	$\|I_{OS}\|$	V_{ID} = ±100mV (Note 4)	$V_{OUT\_\_}$ or $V_{\overline{OUT\_\_}}$ = 0V		30	40	mA
			$V_{OUT\_\_}$ = $V_{\overline{OUT\_\_}}$ = 0V		17	24	
Output Short-Circuit Current (Outputs Shorted Together)	$\|I_{OSB}\|$	V_{ID} = ±100mV, $V_{OUT\_\_}$ = $V_{\overline{OUT\_\_}}$ (Note 4)			5	12	mA
SUPPLY CURRENT							
Supply Current	I_{CC}	R_L = 100Ω, EN_ _ = V_{CC}			53	65	mA
		R_L = 100Ω, EN_ _ = V_{CC}, switching at 670MHz (1.34Gbps)			53	65	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, f_{IN} < 1.34GHz, t_{R_IN} = t_{F_IN} = 125ps, R_L = 100Ω ±1%, |V_{ID}| ≥ 150mV, V_{CM} = +0.075V to (V_{CC} - 0.6V) (MAX9394 only), V_{CM} = +0.6V to (V_{CC} - 0.075V) (MAX9395 only), EN_ _ = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, |V_{ID}| = 0.2V, V_{CM} = +1.2V, f_{IN} = 1.34GHz, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEL to Switched Output	t_{SWITCH}	Figure 3			1.1	ns
Disable Time to Differential Output Low	t_{PHD}	Figure 4			1.7	ns
Enable Time to Differential Output High	t_{PDH}	Figure 4			1.7	ns
Switching Frequency	f_{MAX}	V_{OD} ≥ 250mV	1.5	2.2		GHz
Low-to-High Propagation Delay	t_{PLH}	Figures 1, 5	340	567	720	ps
High-to-Low Propagation Delay	t_{PHL}	Figures 1, 5	340	562	720	ps
Pulse Skew $\|t_{PLH} - t_{PHL}\|$	t_{SKEW}	Figures 1, 5 (Note 6)		12.4	86	ps
Output Channel-to-Channel Skew	t_{CCS}	Figure 6 (Note 7)		16	87	ps
Output Low-to-High Transition Time (20% to 80%)	t_R	$f_{IN\_\_}$ = 100MHz, Figures 1, 5	112	154	187	ps
Output High-to-Low Transition Time (80% to 20%)	t_F	$f_{IN\_\_}$ = 100MHz, Figures 1, 5	112	152	187	ps
Added Random Jitter	t_{RJ}	$f_{IN\_\_}$ = 1.34GHz, clock pattern (Note 8)			2	$ps_{(RMS)}$
Added Deterministic Jitter	t_{DJ}	1.34Gbps, 2^{23} - 1 PRBS (Note 8)		60	91	ps_{P-P}

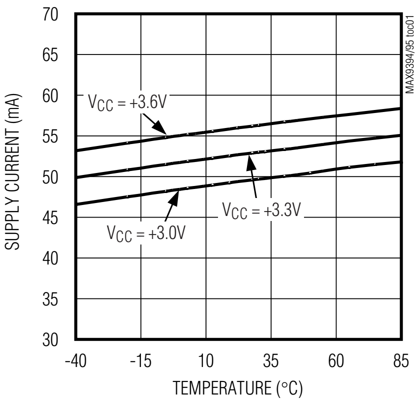
Note 1: Measurements obtained with the device in thermal equilibrium. All voltages referenced to GND except V_{ID}, V_{OD}, and ΔV_{OD}.
Note 2: Current into the device defined as positive. Current out of the device defined as negative.
Note 3: DC parameters production tested at T_A = +25°C and guaranteed by design and characterization for T_A = -40°C to +85°C.
Note 4: Current through either output.
Note 5: Guaranteed by design and characterization. Limits set at ±6 sigma.
Note 6: t_{SKEW} is the magnitude difference of differential propagation delays for the same output over the same condtions. t_{SKEW} = $|t_{PHL} - t_{PLH}|$.
Note 7: Measured between outputs of the same device at the signal crossing points for a same-edge transition under the same conditions. Does not apply to loopback mode.
Note 8: Device jitter added to the differential input signal.

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

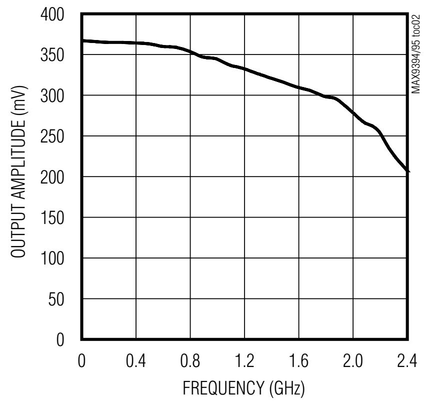
Typical Operating Characteristics

(V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, T_A = +25°C, f_{IN} = 1.34GHz, Figure 5.)

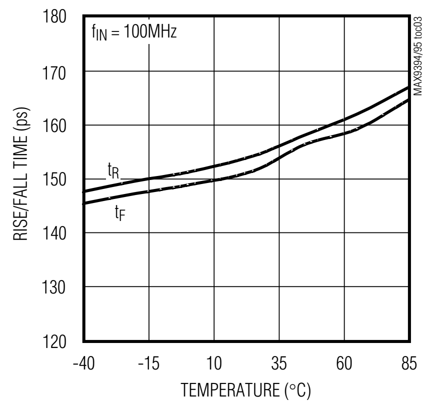
SUPPLY CURRENT vs. TEMPERATURE



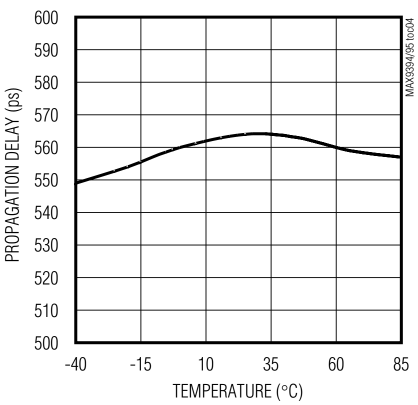
OUTPUT AMPLITUDE vs. FREQUENCY



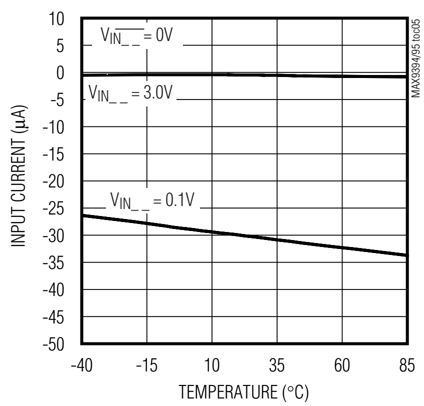
OUTPUT RISE/FALL TIME vs. TEMPERATURE



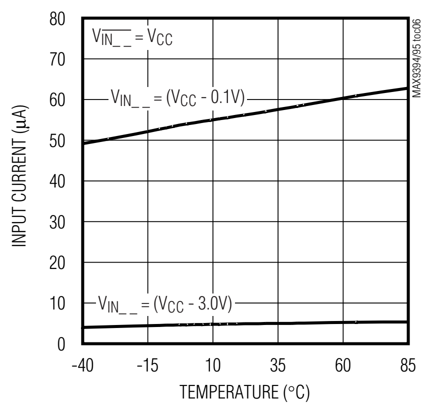
PROPAGATION DELAY vs. TEMPERATURE



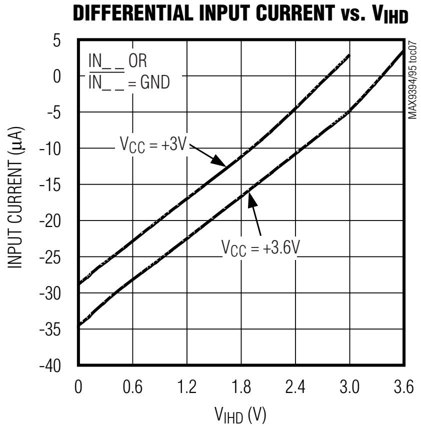
MAX9394 DIFFERENTIAL INPUT CURRENT vs. TEMPERATURE



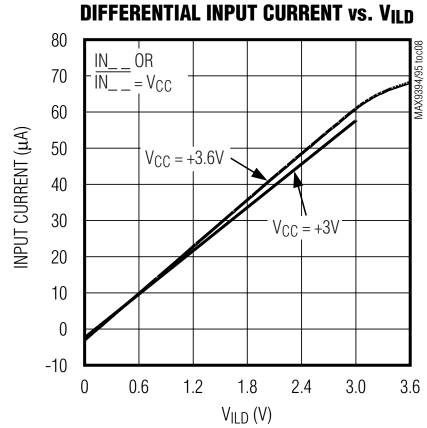
MAX9395 DIFFERENTIAL INPUT CURRENT vs. TEMPERATURE



MAX9394 DIFFERENTIAL INPUT CURRENT vs. V_{IHD}



MAX9395 DIFFERENTIAL INPUT CURRENT vs. V_{ILD}



2:1 Multiplexers and 1:2 Demultiplexers with Loopback

Pin Description

PIN		NAME	FUNCTION
TQFP	QFN		
1, 2, 3, 30, 31, 32	1, 2, 28	N.C.	No Connection. Not internally connected.
4, 9, 20, 25	3, 8, 18, 23	GND	Ground
5	4	ENB	Channel B Output Enable. Drive ENB high to enable the LVDS outputs for channel B. An internal 435kΩ resistor to GND pulls ENB low when unconnected.
6	5	OUTB	Channel B LVDS Noninverting Output. Connect a 100Ω termination resistor between OUTB and $\overline{\text{OUTB}}$ at the receiver inputs to ensure proper operation.
7	6	$\overline{\text{OUTB}}$	Channel B LVDS Inverting Output. Connect a 100Ω termination resistor between OUTB and $\overline{\text{OUTB}}$ at the receiver inputs to ensure proper operation.
8, 13, 24, 29	7, 22, 27	V_{CC}	Power-Supply Input. Bypass each V_{CC} to GND with a 0.1µF and 0.01µF ceramic capacitor. Install both bypass capacitors as close to the device as possible, with the 0.01µF capacitor closest to the device.
10	9	$\overline{\text{INB0}}$	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Inverting Input. An internal 128kΩ pullup resistor to V_{CC} pulls the input high when unconnected (MAX9394). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9395).
11	10	INB0	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Noninverting Input. An internal 128kΩ pullup resistor to V_{CC} pulls the input high when unconnected (MAX9394). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9395).
12	11	LB_SELB	Loopback Select for Channel B Output. Connect LB_SELB to GND or leave unconnected to reproduce the INB_ ($\overline{\text{INB\_}}$) differential inputs at OUTB ($\overline{\text{OUTB}}$). Connect LB_SELB to V_{CC} to loop back the INA ($\overline{\text{INA}}$) differential inputs to OUTB ($\overline{\text{OUTB}}$). An internal 435kΩ resistor to GND pulls LB_SELB low when unconnected.
14	12	$\overline{\text{INB1}}$	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Inverting Input. An internal 128kΩ pullup resistor to V_{CC} pulls the input high when unconnected (MAX9394). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9395).
15	13	INB1	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Noninverting Input. An internal 128kΩ pullup resistor to V_{CC} pulls the input high when unconnected (MAX9394). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9395).
16	14	BSEL	Channel B Multiplexer Control Input. Selects the differential input to reproduce at the B channel differential output. Connect BSEL to GND or leave unconnected to select the INB0 ($\overline{\text{INB0}}$) set of inputs. Connect BSEL to V_{CC} to select the INB1 ($\overline{\text{INB1}}$) set of inputs. An internal 435kΩ resistor to GND pulls BSEL low when unconnected.
17	15	ENA1	Channel A1 Output Enable. Drive ENA1 high to enable the A1 LVDS outputs. An internal 435kΩ resistor to GND pulls the ENA1 low when unconnected.
18	16	$\overline{\text{OUTA1}}$	Channel A1 LVDS Inverting Output. Connect a 100Ω termination resistor between OUTA1 and $\overline{\text{OUTA1}}$ at the receiver inputs to ensure proper operation.
19	17	OUTA1	Channel A1 LVDS Noninverting Output. Connect a 100Ω termination resistor between OUTA1 and $\overline{\text{OUTA1}}$ at the receiver inputs to ensure proper operation.

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	QFN		
21	19	ENA0	Channel A0 Output Enable. Drive ENA0 high to enable the A0 LVDS outputs. An internal 435kΩ resistor to GND pulls ENA0 low when unconnected.
22	20	$\overline{\text{OUTA0}}$	Channel A0 LVDS Inverting Output. Connect a 100Ω termination resistor between OUTA0 and $\overline{\text{OUTA0}}$ at the receiver inputs to ensure proper operation.
23	21	OUTA0	Channel A0 LVDS Noninverting Output. Connect a 100Ω termination resistor between OUTA0 and $\overline{\text{OUTA0}}$ at the receiver inputs to ensure proper operation.
26	24	INA	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Noninverting Input. An internal 128kΩ pullup resistor to V_{CC} pulls the input high when unconnected (MAX9394). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9395).
27	25	$\overline{\text{INA}}$	LVDS/HSTL (MAX9394) or LVPECL/CML (MAX9395) Inverting Input. An internal 128kΩ pullup resistor to V_{CC} pulls the input high when unconnected (MAX9394). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9395).
28	26	LB_SELA	Loopback Select for Channel A Output. Connect LB_SELA to GND or leave unconnected to reproduce the INA ($\overline{\text{INA}}$) differential inputs at OUTA_ ($\overline{\text{OUTA\_}}$). Connect LB_SELA to V_{CC} to loop back the INB_ ($\overline{\text{INB\_}}$) differential inputs to OUTA_ ($\overline{\text{OUTA\_}}$). An internal 435kΩ resistor to GND pulls LB_SELA low when unconnected.
—	—	EP	Exposed Paddle. Connect to GND for optimal thermal and EMI characteristics.

Detailed Description

The LVDS interface standard provides a signaling method for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 standard. LVDS utilizes a lower voltage swing than other communication standards, achieving higher data rates with reduced power consumption, while reducing EMI emissions and system susceptibility to noise.

The MAX9394/MAX9395 high-speed, low-power 2:1 multiplexers and 1:2 demultiplexers with loopback provide signal redundancy switching in telecom and storage applications. These devices select one of two remote signal sources for local input and buffer a single local output signal to two remote receivers.

The multiplexer section (channel B) accepts two differential inputs and generates a single LVDS output. The demultiplexer section (channel A) accepts a single differential input and generates two parallel LVDS outputs. The MAX9394/MAX9395 feature a loopback mode that connects the input of channel A to the output of channel B and connects the selected input of channel B to the outputs of channel A. LB_SELA and LB_SELB provide independent loopback control for each channel.

Three LVCMOS/LVTTL logic inputs control the internal connections between inputs and outputs, one for the multiplexer portion of channel B (BSEL), and the other two for loopback control of channels A and B (LB_SELA and LB_SELB). Independent enable inputs for each differential output pair provide additional flexibility.

Input Fail-Safe

The differential inputs of the MAX9394/MAX9395 possess internal fail-safe protection. Fail-safe circuitry forces the outputs to a differential-low condition for undriven inputs or when the common-mode voltage exceeds the specified range. The MAX9394 provides high-level input fail-safe detection for LVDS, HSTL, and other GND-referenced differential inputs. The MAX9395 provides low-level input fail-safe detection for LVPECL, CML, and other V_{CC}-referenced differential inputs.

Select Function

BSEL selects the differential input pair to transmit through OUTB ($\overline{\text{OUTB}}$) for LB_SELB = GND or through OUTA_ ($\overline{\text{OUTA\_}}$) for LB_SELA = V_{CC}. LB_SEL_ controls the loopback function for each channel. Connect LB_SEL_ to GND to select the normal inputs for each channel. Connect LB_SEL_ to V_{CC} to enable the loopback function. The loopback function routes the input of channel A to the output of channel B, and the inputs of channel B to the outputs of channel A. See Tables 1 and 2 for a summary of the input/output routing between channels.

Enable Function

The EN_ _ logic inputs enable and disable each set of differential outputs. Connect EN_ 0 to V_{CC} to enable the OUT_0/$\overline{\text{OUT\_0}}$ differential output pair. Connect EN_0 to GND to disable the OUT_0/$\overline{\text{OUT\_0}}$ differential output pair. The differential output pairs assert to a differential low condition when disabled.

Applications Information

Differential Inputs

The MAX9394/MAX9395 inputs accept any differential signaling standard within the specified common-mode voltage range. The fail-safe feature detects common-mode input signal levels and generates a differential output low condition for undriven inputs or when the common-mode voltage exceeds the specified range ($V_{CM} \geq V_{CC}$ - 0.6V, MAX9394; $V_{CM} \leq$ 0.6V, MAX9395). Leave unused inputs unconnected or connect to V_{CC} for the MAX9394 or to GND for the MAX9395.

Power-Supply Bypassing

Bypass each V_{CC} to GND with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible. Install the 0.01µF capacitor closest to the device.

Differential Traces

Input and output trace characteristics affect the performance of the MAX9394/MAX9395. Connect each input and output to a 50Ω characteristic impedance trace. Maintain the distance between differential traces and eliminate sharp corners to avoid discontinuities in differential impedance and maximize common-mode noise immunity. Minimize the number of vias on the differential input and output traces to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

Output Termination

Terminate LVDS outputs with a 100Ω resistor between the differential outputs at the receiver inputs. LVDS outputs require 100Ω termination for proper operation.

Ensure that the output currents do not exceed the current limits specified in the *Absolute Maximum Ratings*. Observe the total thermal limits of the MAX9394/MAX9395 under all operating conditions.

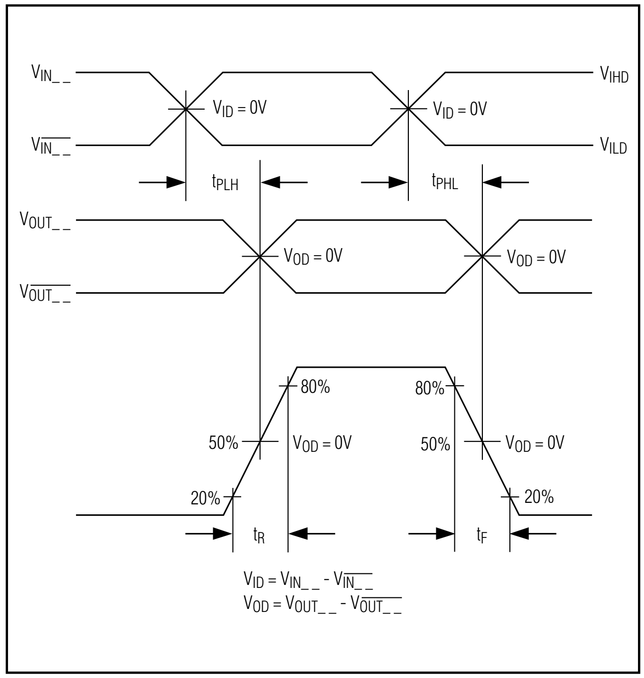


Figure 1. Output Transition Time and Propagation Delay Timing Diagram

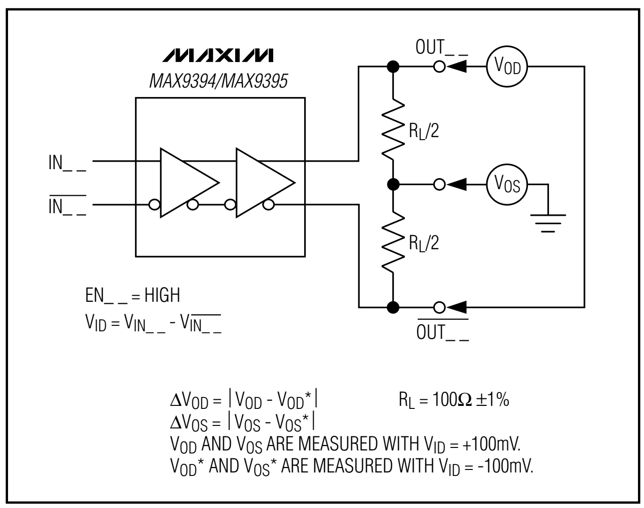


Figure 2. Test Circuit for V_{OD} and V_{OS}

Cables and Connectors

Use matched differential impedance for transmission media. Use cables and connectors with matched differential impedance to minimize impedance discontinuities. Avoid the use of unbalanced cables.

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

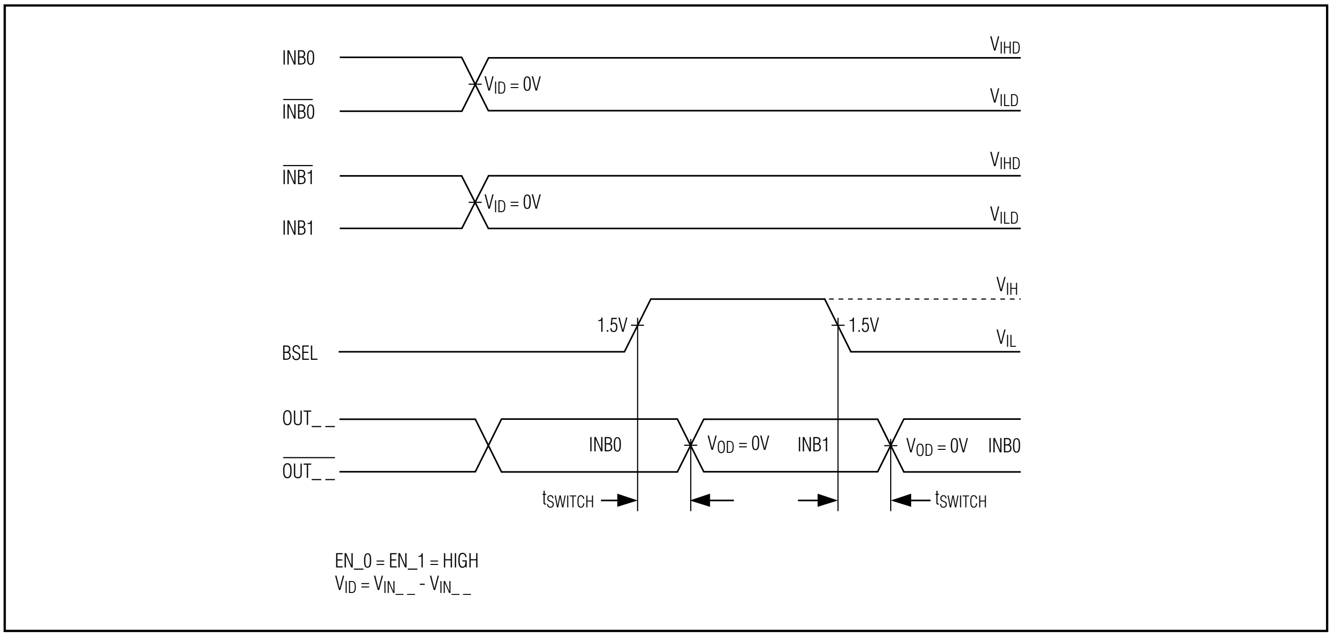


Figure 3. Input to Rising/Falling Edge Select and Mux Switch Timing Diagram

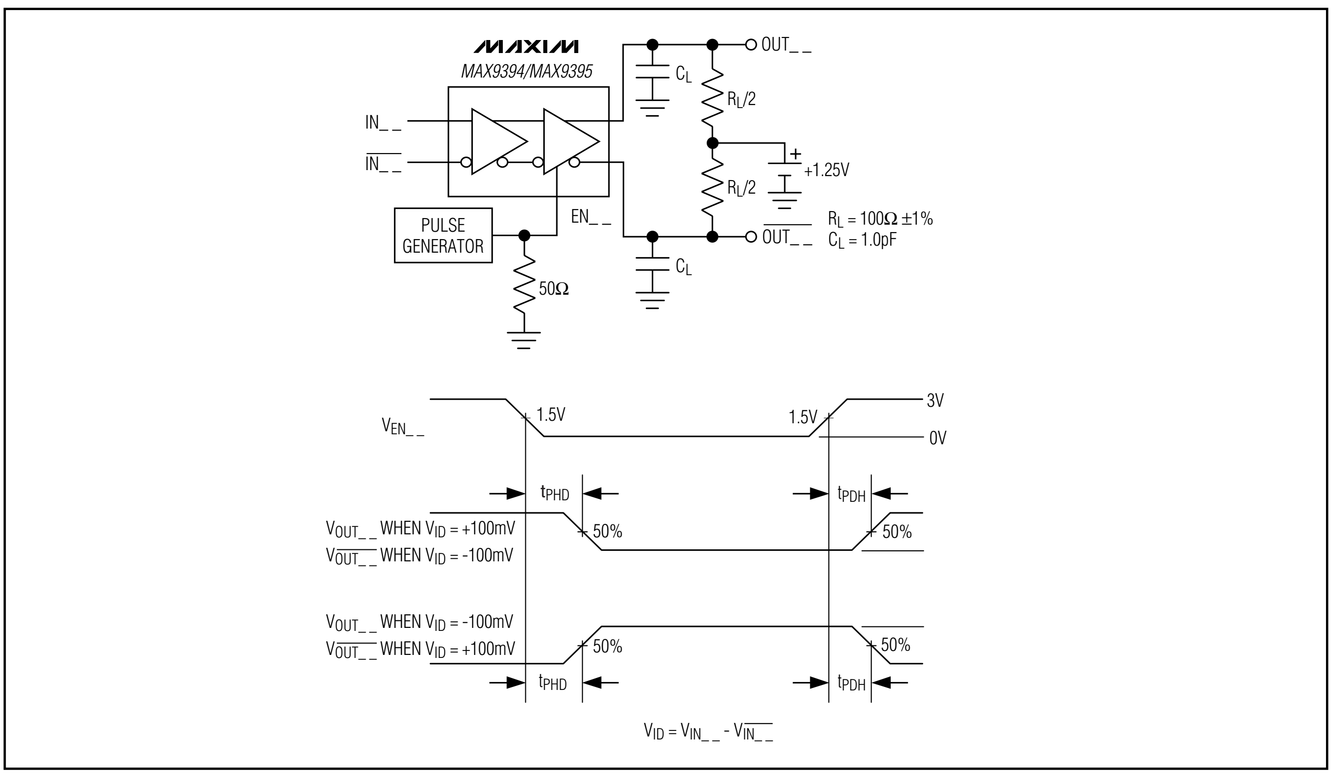


Figure 4. Output Active-to-Disable and Disable-to-Active Test Circuit and Timing Diagram

Table 1. Input Select Truth Table

LOGIC INPUTS			DIFFERENTIAL OUTPUTS	
LB_SELA	LB_SELB	BSEL	OUTA_ / $\overline{\text{OUTA\_}}$	OUTB / $\overline{\text{OUTB}}$
0	0	0	INA selected	INB0 selected
0	0	1	INA selected	INB1 selected
0	1	X	INA selected	INA selected
1	0	0	INB0 selected	INB0 selected
1	0	1	INB1 selected	INB1 selected
1	1	0	INB0 selected	INA selected
1	1	1	INB1 selected	INA selected

X = Don't care.

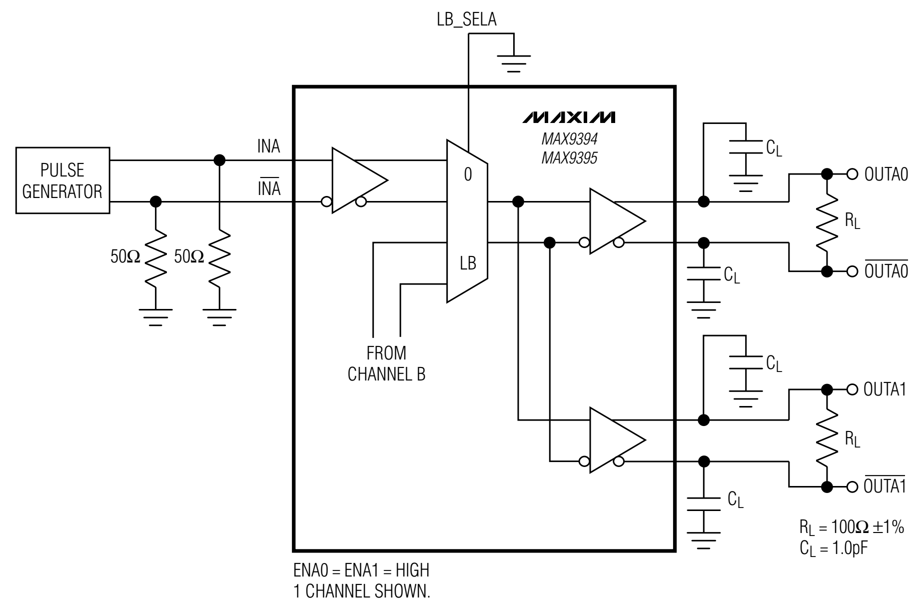


Figure 5. Output Transition Time, Propagation Delay, and Output Channel-to-Channel Skew Test Circuit

Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects.

Board Layout

Use a four-layer printed circuit (PC) board providing separate signal, power, and ground planes for high-speed signaling applications. Bypass V_{CC} to GND as close to the device as possible. Install termination resistors as close to receiver inputs as possible. Match the electrical length of the differential traces to minimize signal skew.

Table 2. Loopback Select Truth Table

LB_SEL_	OUT_ _
GND or open	Normal inputs selected.
V_{CC}	Loopback inputs selected.

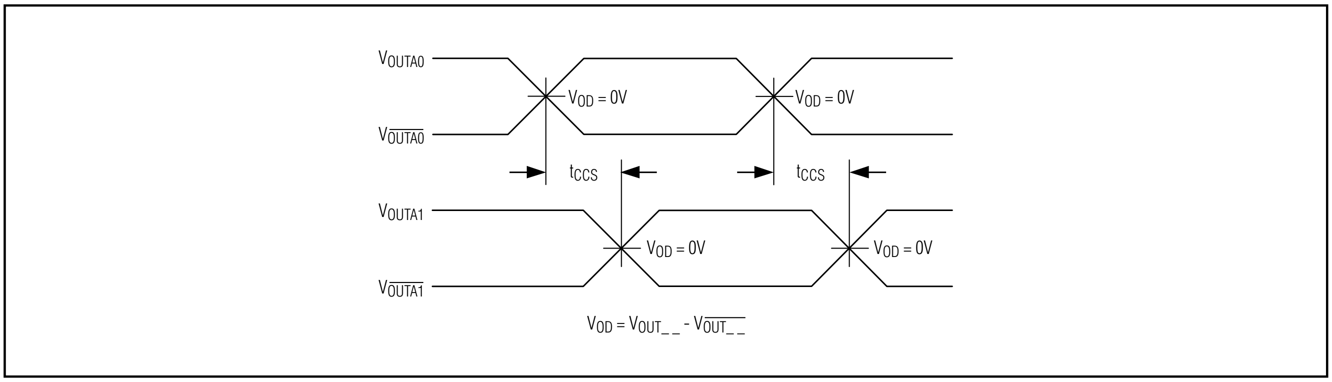
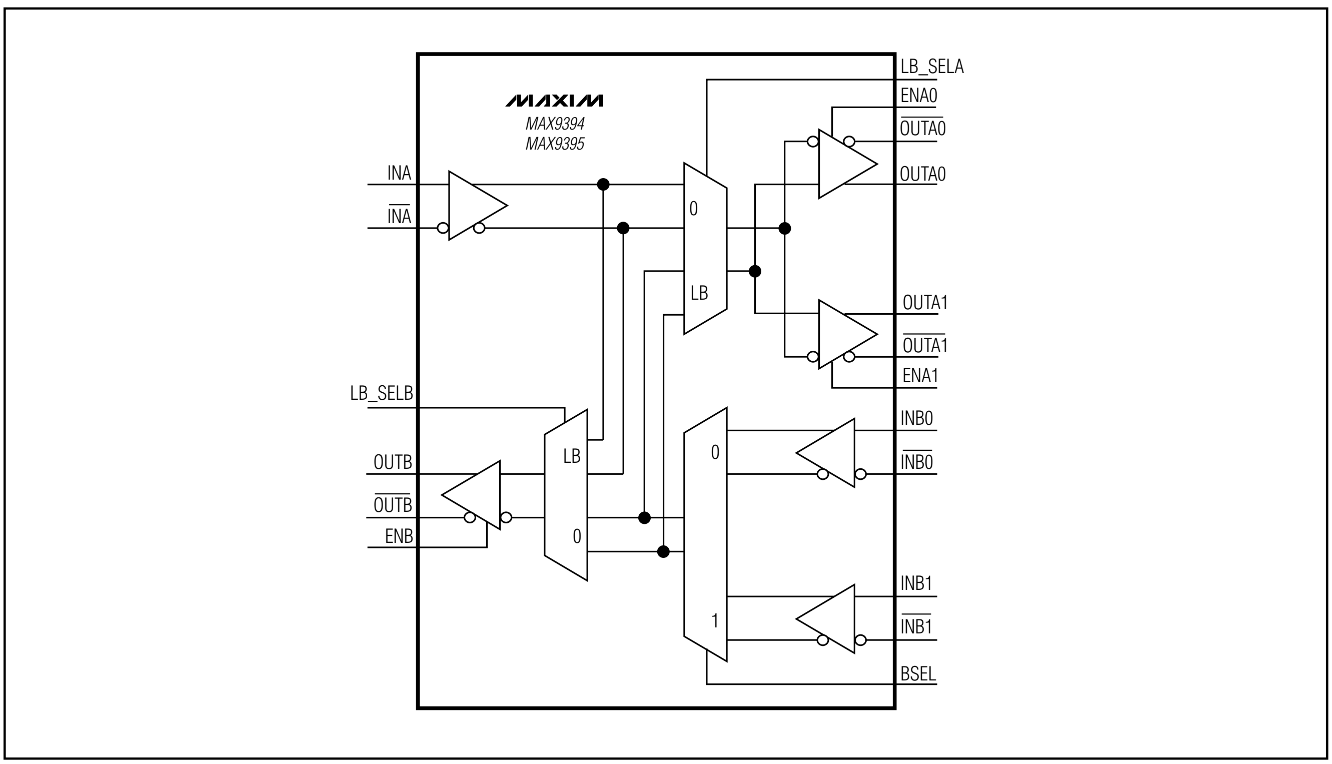
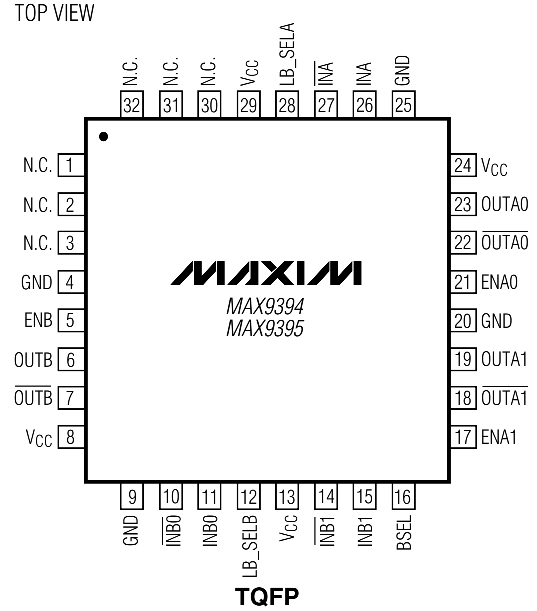


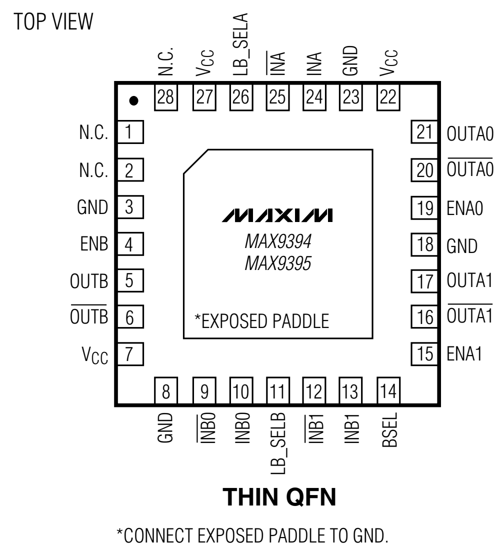
Figure 6. Output Channel-to-Channel Skew

Functional Diagram



Pin Configurations





Chip Information

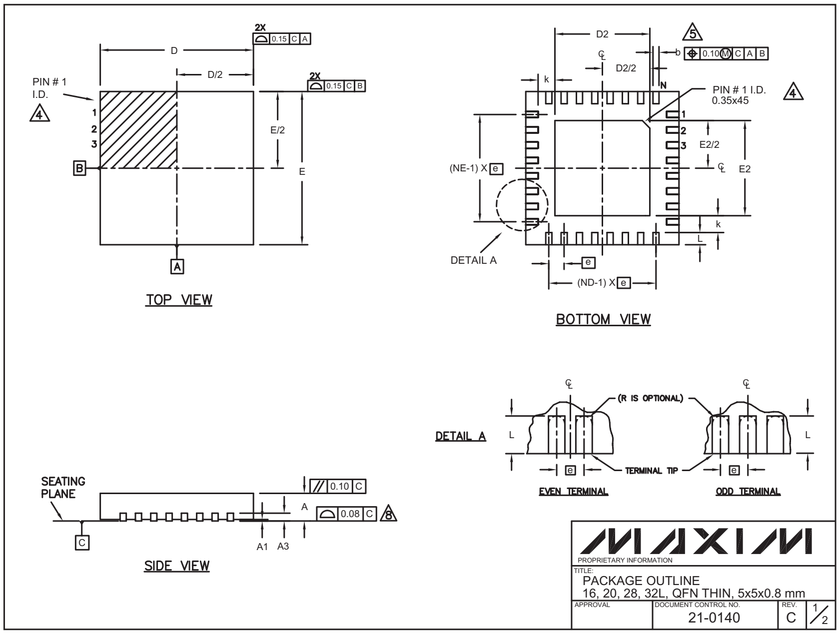
TRANSISTOR COUNT: 1565

PROCESS: Bipolar

2:1 Multiplexers and 1:2 Demultiplexers with Loopback

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

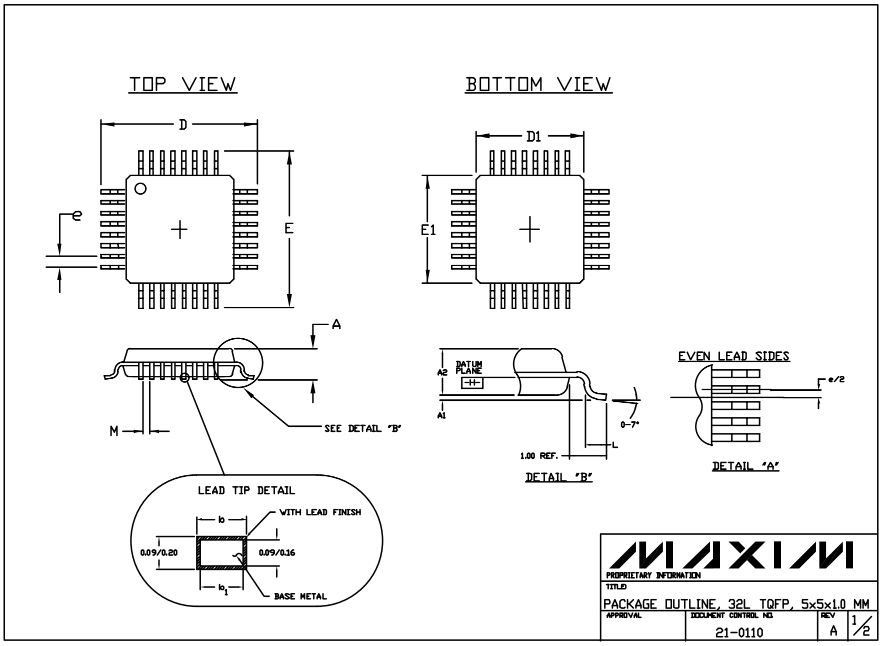
NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. C | 2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

	JEDEC VARIATIONS DIMENSIONS IN MILLIMETERS	
	AA	
	5x5x1.0 MM	
	MIN.	MAX.
A	~	1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	7.00 BSC.	
D_1	5.00 BSC.	
E	7.00 BSC.	
E_1	5.00 BSC.	
L	0.45	0.75
M	0.15	~
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32L TQFP, 5x5x1.0 MM

APPROVAL | DOCUMENT CONTROL NO. 21-0110 | REV A | 2/2