INTRODUCTORY

Dual Ultra-Fast ECL Output Comparator

MAX9687

General Description

The MAX9687 is a dual ultra-fast ECL comparator manufactured with a high-frequency bipolar process (f_T = 6GHz) that is capable of very short propagation delays, maintaining the excellent DC matching characteristics normally found only in slower comparators.

The device is pin comptabile with the AD9687 and Am6687, but it exceeds the AC characteristics of these devices.

The MAX9687 has differential inputs and complementary outputs fully compatible with ECL logic levels. Output current levels are capable of driving 50Ω terminated transmission lines. The ultra-fast operation makes signal processing possible at frequencies in excess of 600MHz.

A Latch Enable function is provided to allow the comparator to be used in a sample-hold or track-hold mode. The Latch Enable inputs are designed to be driven from the complementary outputs of a standard ECL gate. When LE is high and $\overline{LE}$ is low, the comparator functions normally. When LE is forced low and $\overline{LE}$ high, the comparator outputs are locked in the logical states determined by the input conditions at the time of the latch transition. If the Latch Enable function is not used on either of the comparators, the appropriate LE input must be connected to ground; the companion $\overline{LE}$ input can be left open.

Applications

High-Speed A/D Converters

High-Speed Line Receivers

Peak Detectors

Threshold Detectors

High-Speed Triggers

Features

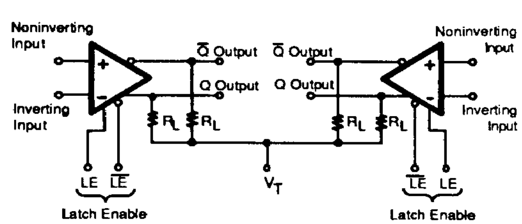
- **1.4ns Propagation Delay**
- **0.5ns Latch Setup Time**
- **2.0ns Latch Enable Pulse Width**
- **+5V, -5.2V Power Supplies**
- **Pin Compatible with AD9687, Am6687, SP9687**
- **Available in Commercial and Military Temp. Ranges**
- **Available in Narrow SO Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE*
MAX9687CPE	0°C to +70°C	16 Plastic DIP
MAX9687CSE	0°C to +70°C	16 Narrow SO
MAX9687CJE	0°C to +70°C	16 CERDIP
MAX9687C/D	0°C to +70°C	Dice
MAX9687MJE	-55°C to +125°C	16 CERDIP

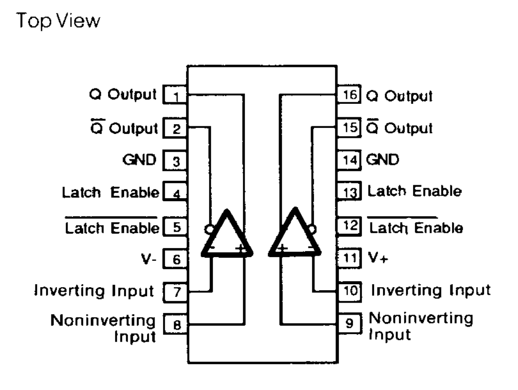
Contact factory for availability of 20-Pin LCC

Functional Diagram



The outputs are open emitters, requiring external pull-down resistors. These resistors may be in the range of 50Ω - 200Ω connected to -2.0V; or 240Ω - 2000Ω connected to -5.2V.

Pin Configuration



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Dual Ultra-Fast ECL Output Comparator

ABSOLUTE MAXIMUM RATINGS

Supply Voltages . . . . ±6V
Power Dissipation (Notes 1, 2) 700mW
Output Short-Circuit Duration (Note 2) . . . . Indefinite
Input Voltages . . . . ±5V
Differential Input Voltages 3.5V
Output Current 30mA

Operating Temperature Range:
Commercial (MAX9687C) . . . . 0°C to +70°C
Military (MAX9687M) . . . . -55°C to +125°C
Storage Temperature Range . . . . -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . 300°C

Note 1: Power derating above T_A = 70°C is based on a maximum junction temperature of 150°C and the thermal resistance factors of θ_{JC} = 75°C/W and θ_{JA} = 145°C/W. For SO package, θ_{JC} = 60°C/W and θ_{JA} = 110°C/W.

Note 2: Continuous short-circuit protection is allowed on 1 comparator per time up to case temperatures of 85°C and ambient temperatures of 30°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

($V+$ = +5V, $V-$ = -5.2V, V_T = -2.0V, R_L = 50Ω, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MAX9687C MIN	MAX9687C TYP	MAX9687C MAX	MAX9687M MIN	MAX9687M TYP	MAX9687M MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 100Ω	T_A = +25°C	-5		+5	-5		+5	mV
			T_A = MIN to MAX	-7		+7	-8		+8	
Temperature Coefficient	$\Delta V_{OS}/\Delta T$				10			15		µV/°C
Input Offset Current	I_{OS}	T_A = +25°C				5			5	µA
		T_A = MIN to MAX				8			12	
Input Bias Current	I_B	T_A = +25°C			10	20		10	20	µA
		T_A = MIN to MAX				30			40	
Input Voltage Range	V_{CM}	(Note 3)		-2.5		+2.5	-2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR			80			80			dB
Power-Supply Rejection Ratio	PSRR				60			60		dB
Input Resistance	R_{IN}	(Note 3)		60			60			kΩ
Input Capacitance	C_{IN}				3			3		pF
I/O Logic Levels										
Output High Voltage	V_{OH}	T_A = MIN		-1.05		-0.87	-1.16		-0.89	V
		T_A = MAX		-0.89		-0.70	-0.88		-0.69	
		T_A = +25°C		-0.96		-0.81	-0.96		-0.81	
Output Low Voltage	V_{OL}	T_A = MIN		-1.89		-1.65	-1.90		-1.65	V
		T_A = MAX		-1.83		-1.57	-1.82		-1.55	
		T_A = +25°C		-1.85		-1.65	-1.85		-1.65	
Positive Supply Current	I_{CC}	T_A = +25°C			30	46		30	46	mA
		T_A = MIN to MAX				50			52	
Negative Supply Current	I_{EE}	T_A = +25°C			54	68		54	68	mA
		T_A = MIN to MAX				72			74	

Note 3: Guaranteed by design, not tested.

SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MAX9687C MIN	MAX9687C TYP	MAX9687C MAX	MAX9687M MIN	MAX9687M TYP	MAX9687M MAX	UNITS
Input to Output High (Notes 3 and 4)	t_{pd+}	$T_A = +25°C$		1.4	1.9		1.4	1.9	ns
		$0°C \le T_A \le +70°C$		1.6	2.2				
		$-55°C \le T_A \le +125°C$					1.7	2.6	
Input to Output Low (Notes 3 and 4)	t_{pd-}	$T_A = +25°C$		1.4	1.9		1.4	1.9	ns
		$0°C \le T_A \le +70°C$		1.6	2.2				
		$-55°C \le T_A \le +125°C$					1.9	2.6	
Latch Enable to Output High (Notes 3 and 4)	$t_{pd+}(E)$	$T_A = +25°C$		1.3	1.8		1.3	1.8	ns
		$0°C \le T_A \le +70°C$		1.4	2.0				
		$-55°C \le T_A \le +125°C$					1.5	2.0	
Latch Enable to Output Low (Notes 3 and 4)	$t_{pd-}(E)$	$T_A = +25°C$		1.3	1.8		1.3	1.8	ns
		$0°C \le T_A \le +70°C$		1.4	1.9				
		$-55°C \le T_A \le +125°C$					1.7	2.6	
Latch Enable (Note 3) Pulse Width	$t_{pw}(E)$		3.0	2.0		3.0	2.0		ns
Min Setup Time	t_s			0.5	1.0		0.5	1.0	ns
Min Hold Time	t_h			0.5	1.0		0.5	1.0	ns

Note 4: V_{IN} = 100mV, V_{OD} = 10mV.

Application Information

Layout

Because of the large gain-bandwidth characteristic of the MAX9687, special precautions need to be taken if the high-speed capabilities of the device are to be utilized. A PC board with ground plane should be considered mandatory. All decoupling capacitors should be mounted as close as possible to the power-supply pins and the ECL outputs processed in microstrip fashion consistent with the load termination of 50Ω to 120Ω. For low impedance applications, microstrip layout at the input may also be helpful. Close attention should be paid to the bandwidth of the decoupling and terminating components. Chip components to minimize lead inductance can be used as an advantage here.

Input Slew Rate Requirement

As with all high-speed comparators, the high gain-bandwidth product of these devices creates oscillation problems when the input traverses through the linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew rate requirements. The tendency of the part to oscillate is a function of the layout and the source impedance of the circuit employed. Poor layout and larger source impedance will increase the minimum slew rate specification.

In many applications, the addition of regenerative feedback will assist the input signal through the linear region, which will lower the minimum slew rate requirement considerably. For example, with the addition of positive feedback components Rf = 1kΩ and Cf = 10pF, the minimum slew rate requirement can be reduced by a factor of 4.

Figure 1 shows a high-speed receiver application with 50Ω input and output termination. With this configuration, in which a ground plane and microstrip PC board were used, the minimum slew rate for clean output switching is 1.6V/µs. Sine wave inputs, imply a minimum

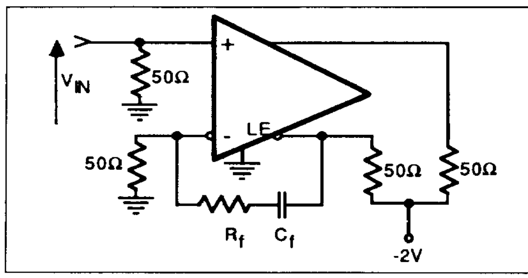

Figure 1. Regenerative Feedback. High-speed receiver with 50Ω input and output termination.

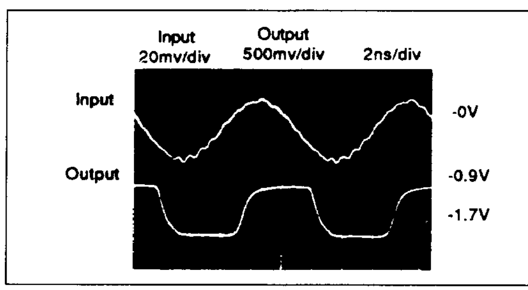

Figure 2. As a high-speed receiver, the MAX9687 is capable of processing signals in excess of 600MHz. Figure 2 is a 100MHz example with an input signal level of 14mVrms.

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signal size of 360mVrms at 500kHz and 90mV at 2MHz.

$$E_{RMS} = \frac{SlewRate}{2\sqrt{2}\pi f}$$

The timing diagram (Figure 3) illustrates worst-case conditions in representing the series of events to complete the compare function.

The top line of the diagram illustrates 2 Latch Enable pulses. Each pulse is high for the compare function and low for the latch function. The first pulse demonstrates the compare function; part of the input action takes place during the compare mode. The second pulse demonstrates a compare function interval during which there is no change in the input.

The leading edge of the input signal, illustrated as a large amplitude, small overdrive pulse, switches the comparator after time interval t_{pd}. Outputs Q and $\overline{Q}$ are essentially similar in timing. The input signal must occur at time t_s before the latch falling edge, and it must be maintained for time t_h after the edge to be acquired. After t_h, the output is no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of $t_{pw}(E)$ is needed for the strobe operation, and the output transitions occur after a time $t_{pd}(E)$.

Definition of Terms

V_{OS} Input Offset Voltage - The voltage required between the input terminals to obtain 0V differential at the output.

V_{IN} Input Voltage Pulse Amplitude

V_{OD} Input Voltage Overdrive

t_{pd+} Input to Output High Delay - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output low to high transition.

t_{pd-} Input to Output Low Delay - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output high to low transition.

$t_{pd+}(E)$ Latch Enable to Output High Delay - The propagation delay measured from the 50% point of the Latch Enable signal low to high transition to the 50% point of an output low to high transition.

$t_{pd-}(E)$ Latch Enable to Output Low Delay - The propagation dealy measured from the 50% point of the Latch Enable signal low to high transition to the 50% point of an output high to low transition.

$t_{pw}(E)$ Minimum Latch Enable Pulse Width - The minimum time the Latch Enable signal must be high to acquire and hold an input signal.

t_s Minimum Setup Time - The minimum time before the negative transition of the Latch Enable pulse that an input signal must be present to be acquired and held at the outputs.

t_h Minimum Hold Time - The minimum time after the negative transition of the Latch Enable signal that an input signal must remain unchanged to be acquired and held at the outputs.

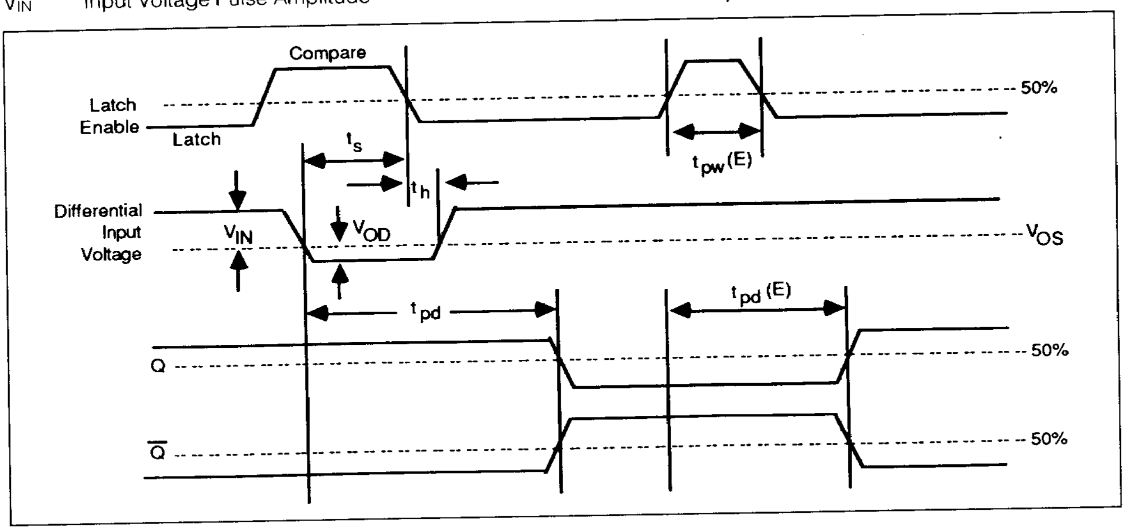

Figure 3. Timing Diagram