M51C98
HIGH-SPEED CHMOS 16,384 x 4-BIT STATIC RAM

Military

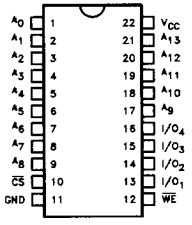
- **35 ns Max Access Time**
- **60 mA Typical Operating Current**
- **5 mA Typical Standby Current**

- **Static Operation**
  — No Clock/Refresh Required
- **Equal Access and Cycle Times**
  — Simplifies System Design
- **Single +5V Supply**
- **Power Down Mode**
- **Industry Standard Pin Out**
- **TTL Compatible**
- **Common Data Input and Output**
- **Three-State Outputs**

The 51C98 is a 65,536-bit high-speed static RAM configured 16K x 4. It is fabricated using Intel's high performance 1.0 micron CHMOS IV technology. This state of the art technology, coupled with Intel's innovative 6T cell design, virtually eliminates latch-up and alpha-induced soft errors without organic die coating.

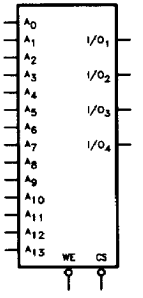
The power down feature, controlled by $\overline{CS}$, also contributes greatly to system reliability. The device's power consumption is reduced 10-fold when in this low power standby mode. This results in significant system power and cooling level savings. In fact, an 85% system power reduction is achievable in large systems where a majority of the devices are deselected.

Pin Configuration



270190-1

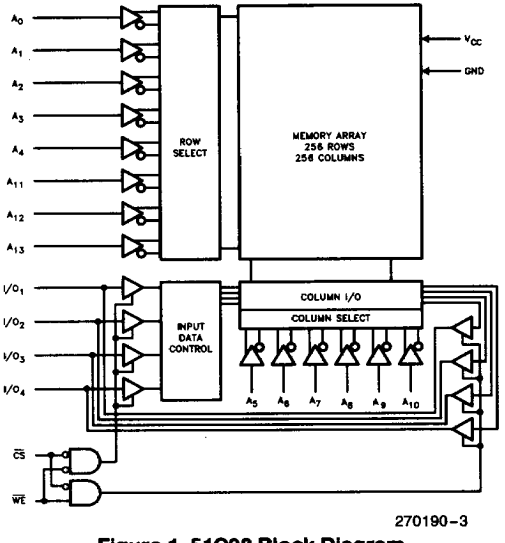
Logic Symbol



270190-2

Pin Names

A_0–A_{13}	Address Inputs	I/O_1–I/O_4	Data Input/Output
$\overline{WE}$	Write Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	GND	Ground



270190-3

Figure 1. 51C98 Block Diagram

February 1991
Order Number: 270190-004

DEVICE OPERATION

The 51C98 has two control inputs: Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$). $\overline{CS}$ is the power control pin and should be used for device selection. $\overline{WE}$ is the data control pin and should be used to gate data at the I/O pins.

Standby Power

The 51C98 is placed in a standby or reduced power consumption mode by applying a high (V_{IH}) to the $\overline{CS}$ input. When in standby mode, the device is deselected and the outputs are in a high impedance state, independent of the $\overline{WE}$ input.

Table 1. Mode Selection Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	Power
H	X	Standby	High-Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias . . . −65°C to +135°C

Storage Temperature Cerdip . . . . −65°C to +150°C

Voltage on any Pin with Respect to Ground . . . . . −0.5V to +7V(1)

D.C. Continuous Output Current . . . . . 20 mA

Power Dissipation 1.0W

Write Mode

Write cycles may be controlled by either $\overline{WE}$ or $\overline{CS}$. In either case, both $\overline{WE}$ and $\overline{CS}$ must be high (V_{IH}) during address transitions. During a $\overline{WE}$ controlled write cycle, $\overline{CS}$ must be held low (V_{IL}) while $\overline{WE}$ is low. Address transfers occur on the falling edge of $\overline{WE}$ and the data transfers on the rising edge of $\overline{WE}$. During a $\overline{CS}$ controlled write cycle, $\overline{WE}$ must be held low (V_{IL}) while $\overline{CS}$ is low. The addresses are then transferred on the falling edge of $\overline{CS}$ and data on the rising edge of $\overline{CS}$. Data, in both cases, must be valid for a time t_{DW} before the controlling input is brought high (V_{IH}) and remain valid for a time t_{DH} after the controlling input is high.

Read Mode

$\overline{CS}$ must be low (V_{IL}) and $\overline{WE}$ must be high (V_{IH}) to activate a read cycle and obtain data at the outputs. Given stable addresses, valid data is available after a time t_{AA}.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Parameter	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

D.C. AND OPERATING CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Unit	Comments
I_{LI}	Input Load Current (All Input Pins)		2	µA	V_{CC} = Max, V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		2	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max, V_{OUT} = GND to 4.5V
I_{CC}	Operating Current		100	mA	V_{CC} = Max, $\overline{CS}$ = V_{IL} Outputs Open, T_{cycle} = Min
I_{SB}	Standby Current		15	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}
V_{IL}	Input Low Voltage	−0.5(1)	0.8	V	
V_{IH}	Input High Voltage	2.2	6.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −4 mA

NOTE:
1. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.

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CAPACITANCE T_C = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	7	pF	V_{OUT} = 0V

A.C. TEST CONDITIONS

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times ..... 5 ns
Timing Reference Level 1.5V
Output Load ..... See Figures 2, 3

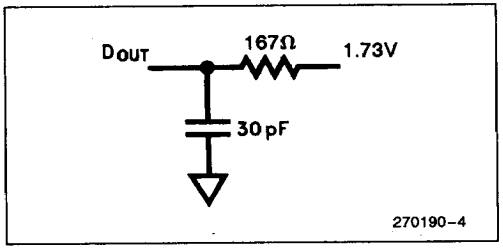


Figure 2. Output Load

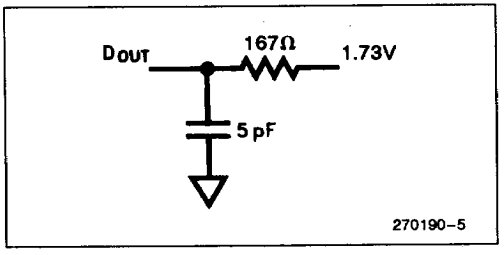


Figure 3. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

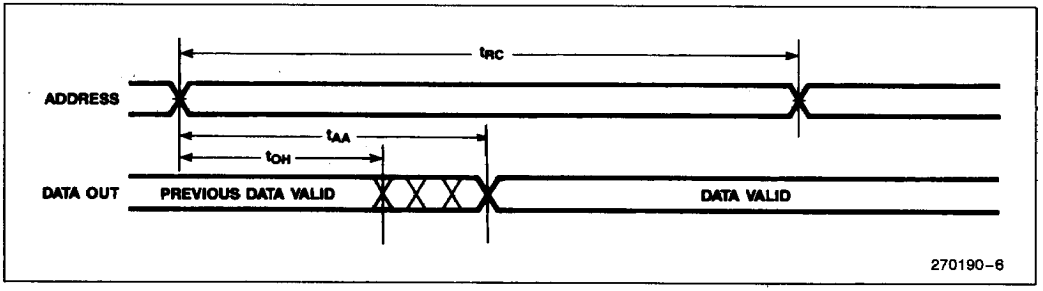
A.C. CHARACTERISTICS (Over Specified Operating Conditions)

READ CYCLE

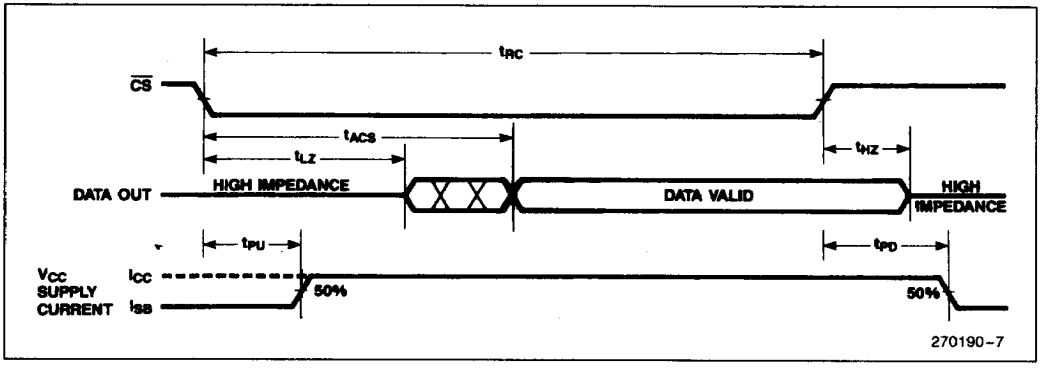
Symbol	Parameter	51C98-35		51C98-45		51C98-55		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}(1)	Read Cycle Time	35		45		55		ns
t_{AA}	Address Access Time		35		45		55	ns
t_{ACS}	Chip Select Access Time		35		45		55	ns
t_{OH}	Output Hold from Address Change	5		5		5		ns
t_{LZ}(2, 3)	Chip Selection to Output in Low Z	0		0		0		ns
t_{HZ}(2, 3)	Chip Deselection to Output in High Z	0	15	0	20	0	25	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		30		40		50	ns

NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured at ±500 mV from steady-state voltage with specified loading in Figure 3.

READ CYCLE NO. 1(1, 2)



READ CYCLE NO. 2(1, 3)



NOTES:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

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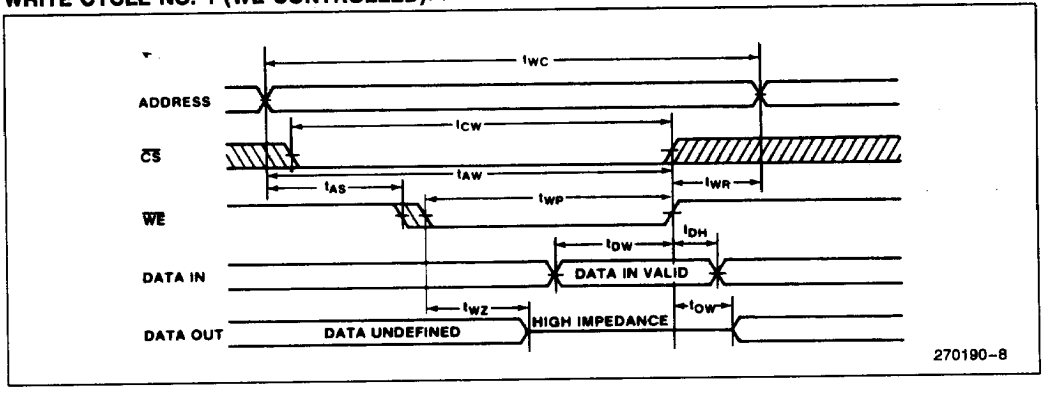
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

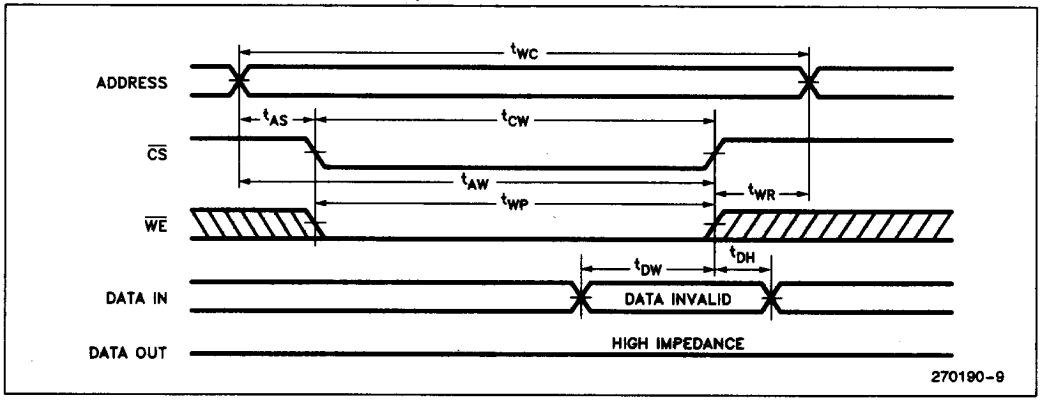
Symbol	Parameter	51C98-35		51C98-45		51C98-55		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}(1)	Write Cycle Time	35		45		55		ns
t_{CW}	Chip Selection to End of Write	30		35		45		ns
t_{AW}	Address Valid to End of Write	30		35		45		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	30		35		45		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DW}	Data Valid to End of Write	15		20		25		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WZ}(2)	Write Enabled to Output in High Z		15	0	15		20	ns
t_{OW}(2)	Output Active from End of Write	0		0		0		ns

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(3)



NOTES:
1. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
2. Transition is measured at ±500 mV from steady-state voltage with specified loading in Figure 3.
3. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2)



NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ switches low coincident with or after $\overline{WE}$ switches low, the outputs will stay in a high impedance state. If $\overline{CS}$ switches high coincident with or after $\overline{WE}$ switches high, the outputs will stay in a high impedance state.

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