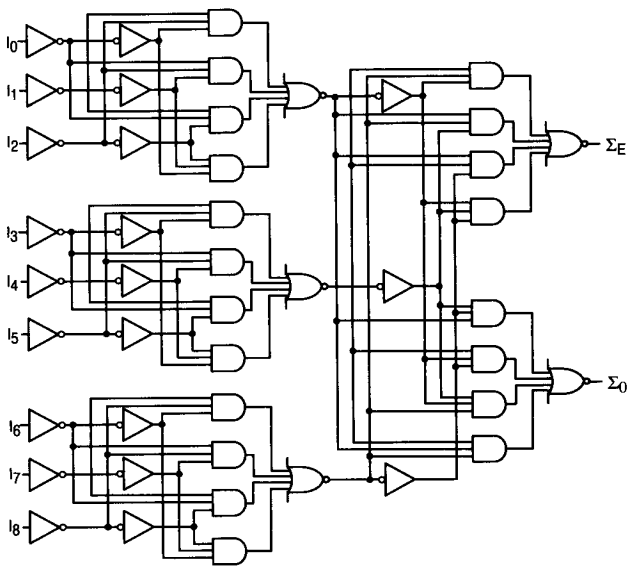
MOTOROLA

9-Bit Odd/Even Parity Generator/Checker

ELECTRICALLY TESTED PER:
MIL-M-38510/34901

The 54F280 is a high-speed parity generator/checker that accepts nine bits of data and detects whether an even or an odd number of these inputs is HIGH. If the number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Military 54F280

AVAILABLE AS:

1) JAN: JM38510/34901BXA
2) SMD: N/A
3) 883: 54F280/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
I_6	1	1	2	V_{CC}
I_7	2	2	3	V_{CC}
NC	3	3	4	OPEN
I_8	4	4	6	V_{CC}
Σ_E	5	5	8	OPEN
Σ_O	6	6	9	OPEN
GND	7	7	10	GND
I_0	8	8	12	V_{CC}
I_1	9	9	13	V_{CC}
I_2	10	10	14	V_{CC}
I_3	11	11	16	V_{CC}
I_4	12	12	18	V_{CC}
I_5	13	13	19	V_{CC}
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Number of High Inputs I_0–I_8	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

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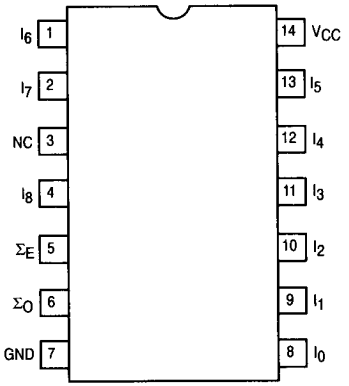
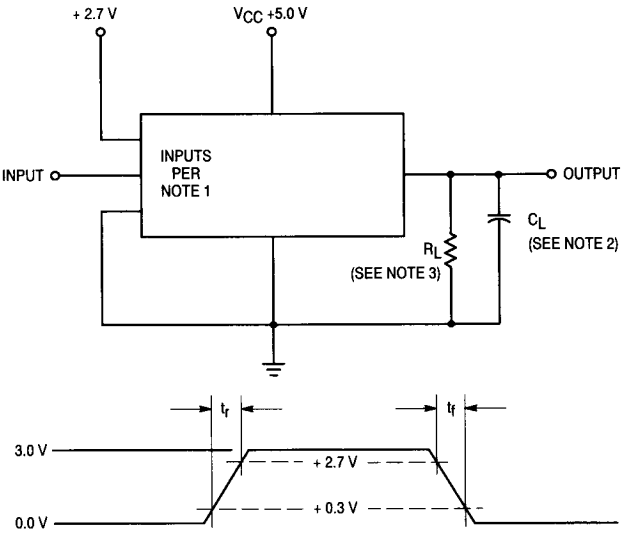
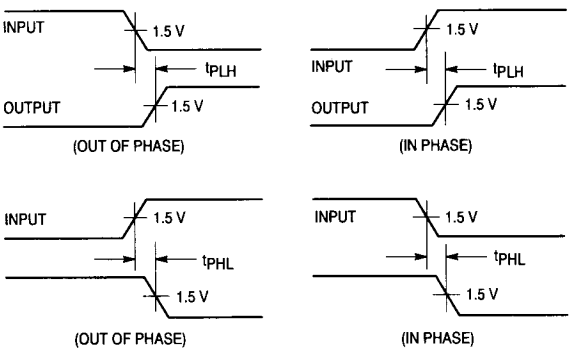
CONNECTION DIAGRAM



AC TEST CIRCUIT





NOTES:

1. Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, $Z_{OUT} \approx 50\ \Omega$.
2. $C_L = 50$ pF ±10%, including scope probe, wiring and stray capacitance without package in test fixture.
3. $R_L = 500\ \Omega$ ±5.0%.
4. Voltage measurements are to be made with respect to network ground terminal.
5. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IN} = 0.8 V (all inputs) or V_{IN} = 0.8 V, (pins 6, 10, 11) = 2.0 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IN} = 0.8 V or 2.0 V (all inputs).
V_{IC}	Input Clamping Voltage		− 1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "0" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (pins 4, 10, 13), V_{IN} = 0 V (all inputs), V_{OUT} = 0 V.
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (pins 4, 10, 13), or V_{IN} = 0 V (all inputs), V_{OUT} = 2.5 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, other inputs are open.
I_{CC}	Power Supply Current		40		40		40	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**) V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output I_n to Σ_E or Σ_O	1.5	16	1.0	21	1.0	21	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.
t_{PLH1}	Propagation Delay /Data-Output I_n to Σ_E or Σ_O	1.5	15	1.0	20	1.0	20	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 500 Ω.