Quad 3-State Bus Transceiver High-Performance Silicon-Gate CMOS

The MC74HC242 is identical in pinout to the LS242. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This quad bus transceiver is designed for asynchronous two-way communications between data buses. The states of the Output Enables (A-to-B Enable and B-to-A Enable) determine both the direction of data flow (from A to B or from B to A) and the modes of the Data Ports (input, output, or high-impedance).

Output Drive Capability: 15 LSTTL Loads

• Outputs Directly Interface to CMOS, NMOS and TTL

• Operating Voltage Range: 2 to 6V

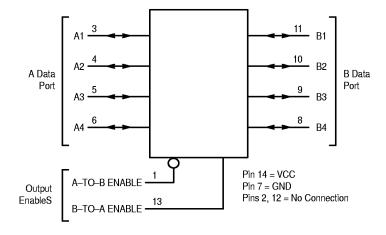
• Low Input Current: 1μA

• High Noise Immunity Characteristic of CMOS Devices

• In Compliance With the JEDEC Standard No. 7A Requirements

• Chip Complexity: 130 FETs or 32.5 Equivalent Gates

LOGIC DIAGRAM



MC74HC242



N SUFFIX PLASTIC PACKAGE CASE 646-06

ORDERING INFORMATION

MC74HCXXXN

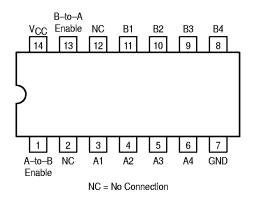
Plastic

FUNCTION TABLE

Control Inputs		Data Port Status		
A–to–B Enable	B–to–A Enable	A	В	
Н	Н	0	I	
L	Н	Z	Z	
Н	L	Z	<u>z</u>	
L	L	1	0	

I = Input; O = Output, O = Inverting OutputZ = High Impedance

Pinout: 14-Lead Plastic Package (Top View)



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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
Vcc	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	٧
V _{in}	DC Input Voltage (Referenced to GND)	- 1.5 to V _{CC} + 1.5	٧
V _{I/O}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	٧
lin	DC Input Current, per Pin	± 20	mA
1/0	DC Output Current, per Pin	± 35	mA
Icc	DC Supply Current, V _{CC} and GND Pins	± 75	mA
PD	Power Dissipation in Still Air Plastic DIP†	750	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter			Max	Unit
VCC	DC Supply Voltage (Referenced to GND)			6.0	٧
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)			VCC	٧
TA	Operating Temperature Range, All Package Types		- 55	+ 125	°C
t _r , t _f	Input Rise/Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

			vcc	Guaranteed Limit			
Symbol	Parameter	Condition	v	–55 to 25°C	≤85°C	≤125°C	Unit
VIH	Minimum High-Level Input Voltage	$V_{out} = 0.1V \text{ or } V_{CC} - 0.1V$ $ I_{out} \le 20 \mu A$	2.0 4.5 6.0	1.50 3.15 4.20	1.50 3.15 4.20	1.50 3.15 4.20	٧
V _{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1V$ or $V_{CC} - 0.1V$ $ I_{out} \le 20\mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	٧
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μΑ	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL} \qquad I_{out} \le 6.0 \text{mA} \\ I_{out} \le 7.8 \text{mA}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{iH} \text{ or } V_{iL}$ $ I_{out} \le 20\mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	٧
		$V_{in} = V_{IH} \text{ or } V_{IL} \qquad I_{out} \le 6.0 \text{mA} $ $ I_{out} \le 7.8 \text{mA}$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
lin	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μΑ
loz	Maximum Three–State Leakage Current	Output in High-Impedance State Vin = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	±0.5	±5.0	±10.0	μА
Icc	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0μA	6.0	8	80	160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

^{*} Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

[†]Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

		VCC	Gua			
Symbol	Parameter	V	–55 to 25°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, A to B or B to A (Figures 2 and 4)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
tPLZ, tPHZ	Maximum Propagation Delay, Output Enable to Output A or B (Figures 3 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tPZL, tPZH	Maximum Propagation Delay, Output Enable to Output A or B (Figures 3 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
tTLH, tTHL	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C _{in}	Maximum Input Capacitance		10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High Impeda State)	ance	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V _{CC} = 5.0 V	
C_PD	Power Dissipation Capacitance (Per Transceiver)*	31	pF

^{*}Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

DATA PORTS

A1-A4 (Pins 3,4,5,6) and B1-B4 (Pins 11,10,9,8)

Data on these pins may be transferred between data buses. Depending upon the states of the Output Enables, these pins may be inputs, outputs or open circuits (high-impedance).

CONTROL INPUTS

A-to-B Enable (Pin 1) and B-to-A Enable (Pin 13)

Data on these Output Enables determine both the direction of the data flow (from A to B or from B to A) and the states of the outputs (standard or high impedance), according to the Function Table.

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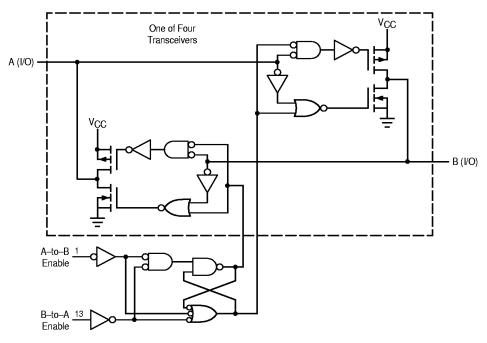
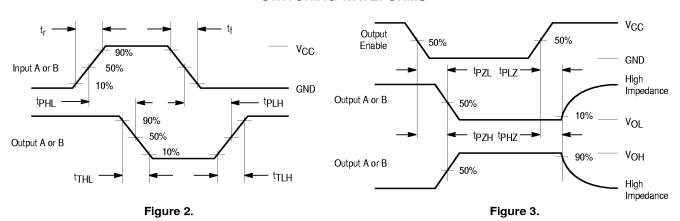
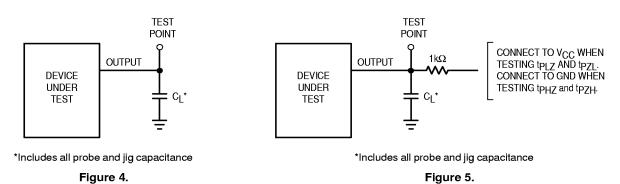


Figure 1. Expanded Logic Diagram

SWITCHING WAVEFORMS



TEST CIRCUITS



MOTOROLA 4

OUTLINE DIMENSIONS

N SUFFIX PLASTIC DIP PACKAGE CASE 646-06 ISSUE L В

NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 DIMENSION L TO CENTER OF LEADS WHEN
- FORMED PARALLEL
- DIMENSION B DOES NOT INCLUDE MOLD
- ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	0.715	0.770	18.16	19.56		
В	0.240	0.260	6.10	6.60		
С	0.145	0.185	3.69	4.69		
D	0.015	0.021	0.38	0.53		
т	0.040	0.070	1.02	1.78		
G	0.100	BSC	2.54	2.54 BSC		
Н	0.052	0.095	1.32	2.41		
_	0.008	0.015	0.20	0.38		
K	0.115	0.135	2.92	3.43		
Ĺ	0.300	BSC	7.62 BSC			
М	0°	10°	0°	10°		
N	0.015	0.039	0.39	1.01		

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