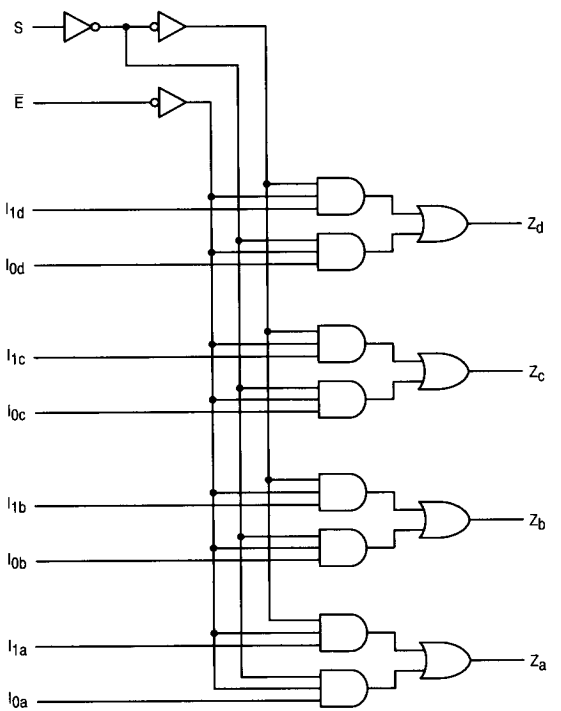
MOTOROLA

Quad 2-Input Data Selector/Multiplexer

ELECTRICALLY TESTED PER:
MIL-M-38510/33903

The 54F157A is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The 'F157A can also be used to generate any four of the 16 different functions of two variables.

LOGIC DIAGRAM



Military 54F157A

AVAILABLE AS:

1) JAN: JM38510/33903BXA
2) SMD: N/A
3) 883: 54F157A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
S	1	1	2	V_{CC}
I_{0a}	2	2	3	V_{CC}
I_{1a}	3	3	4	V_{CC}
Z_a	4	4	5	OPEN
I_{0b}	5	5	7	V_{CC}
I_{1b}	6	6	8	V_{CC}
Z_b	7	7	9	OPEN
GND	8	8	10	GND
Z_d	9	9	12	OPEN
I_{1d}	10	10	13	V_{CC}
I_{0d}	11	11	14	V_{CC}
Z_c	12	12	15	OPEN
I_{1c}	13	13	17	V_{CC}
I_{0c}	14	14	18	V_{CC}
$\overline{E}$	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs				Output
$\overline{E}$	S	I_{0n}	I_{1n}	Z_n
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

FUNCTIONAL DESCRIPTION

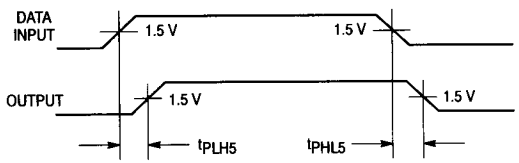
The F157A is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The F157A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are Shown below:

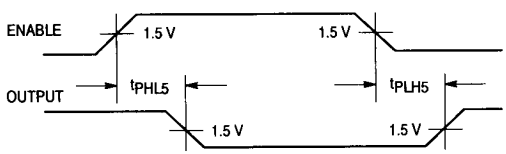
$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$ $\quad Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$

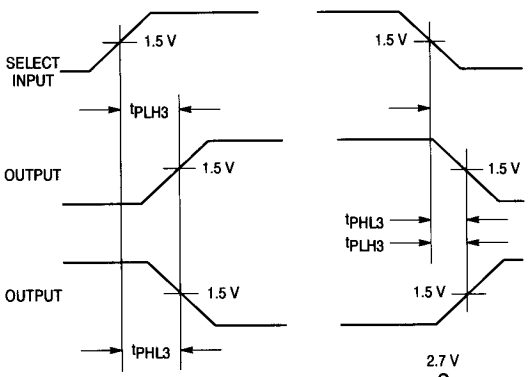
$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0C} \bullet \overline{S})$ $\quad Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

A common use of the F157A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F157A can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

WAVEFORMS







NOTES:

1. Input pulse and has the following characteristics: PRR ≤ 1.0 MHz, $t_r = t_f \leq 2.5$ ns, $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. $R_1 = R_2 = 499\ \Omega \pm 5.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.

AC TEST CIRCUIT

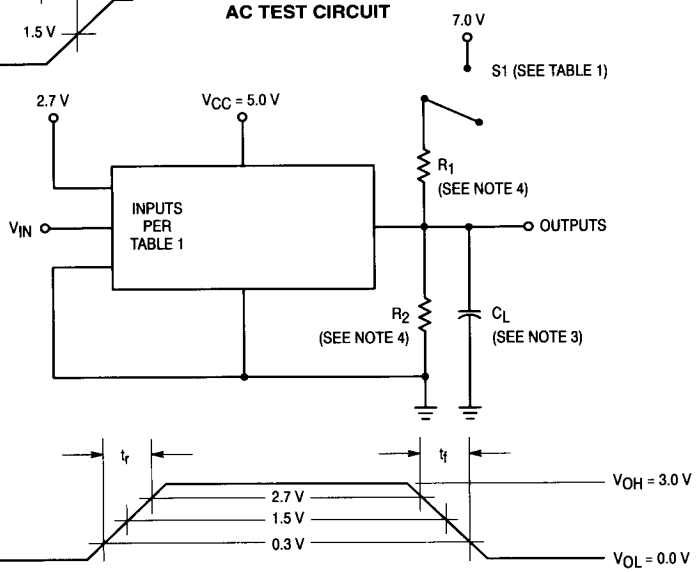


Table 1

Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V, S = 0.8 V or 2.0 V, V_{IL} = 0.8 V, $\overline{E}$ = 0.8 V or open.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, S = 0.8 V or 2.0 V, V_{IN} = 2.0 V, $\overline{E}$ = 0.8 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{E}$ = 2.7 V or 4.5 V, S = 2.7 V, 0 V or 4.5 V.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open, $\overline{E}$ = 7.0 V or 4.5 V, S = 7.0 V, 0 V or 4.5 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open, $\overline{E}$ = 0.5 V, S = 0.5 V, 4.5 V or 0 V.
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 4.5 V, all inputs are open, V_{OUT} = 2.5 V, $\overline{E}$ = 5.5 V or open.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other inputs are open, V_{OUT} = 0 V, S = 0 V, $\overline{E}$ = 0 V.
I_{CC}	Power Supply Current Off		23		23		23	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**) V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output I_n to Z_n	2.5	5.5	1.5	7.5	1.5	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output I_n to Z_n	2.5	6.0	2.5	7.5	2.5	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL3}	Propagation Delay /Data-Output S to Z_n	3.0	7.0	3.0	9.0	3.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH3}	Propagation Delay /Data-Output S to Z_n	4.0	10	4.0	12	4.0	12	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL5}	Propagation Delay /Data-Output $\overline{E}$ to Z_n	2.5	6.5	2.5	7.5	2.5	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH5}	Propagation Delay /Data-Output $\overline{E}$ to Z_n	5.0	9.5	5.0	13	5.0	13	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.