MOTOROLA

Military 54F534

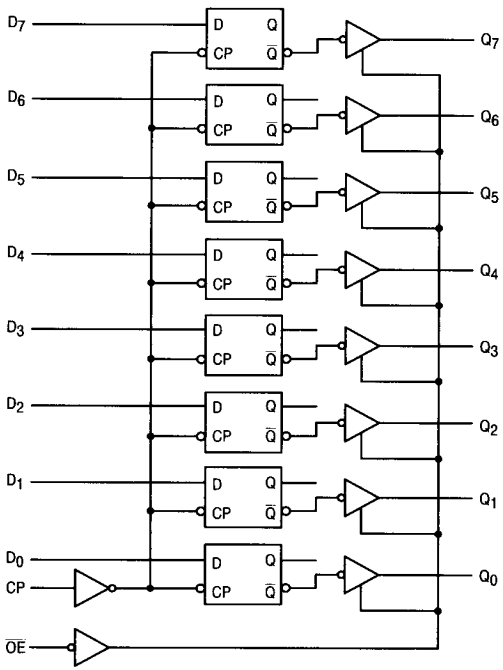
Octal D-Type Positive Edge-Triggered Flip-Flop With 3-State Inverted Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/34106

The 54F534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus Oriented Applications

LOGIC DIAGRAM



AVAILABLE AS:

1) JAN: JM38510/34106BXA
2) SMD: N/A
3) 883: 54F534/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$\overline{OE}$	1	1	1	V_{CC}
$\overline{Q}_0$	2	2	2	OPEN
D_0	3	3	3	V_{CC}
D_1	4	4	4	V_{CC}
$\overline{Q}_1$	5	5	5	OPEN
$\overline{Q}_2$	6	6	6	OPEN
D_2	7	7	7	V_{CC}
D_3	8	8	8	V_{CC}
$\overline{Q}_3$	9	9	9	OPEN
GND	10	10	10	GND
CP	11	11	11	V_{CC}
$\overline{Q}_4$	12	12	12	OPEN
D_4	13	13	13	V_{CC}
D_5	14	14	14	V_{CC}
$\overline{Q}_5$	15	15	15	OPEN
$\overline{Q}_6$	16	16	16	OPEN
D_6	17	17	17	V_{CC}
D_7	18	18	18	V_{CC}
$\overline{Q}_7$	19	19	19	OPEN
V_{CC}	20	20	20	V_{CC}

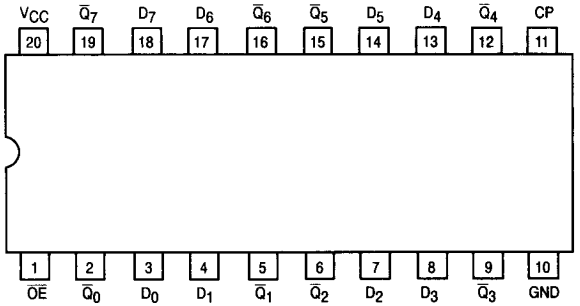
BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

4

TRUTH TABLE			
Inputs		Outputs	
D_n	CP	$\overline{OE}$	Q_n
H	↑	L	H
L	↑	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

LOGIC DIAGRAM

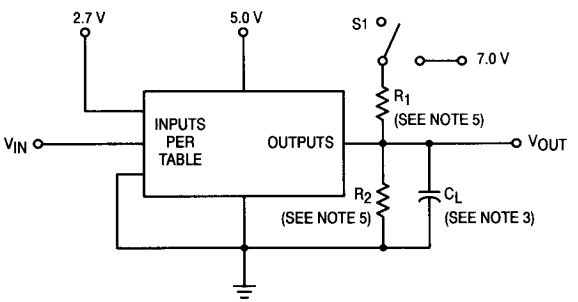


FUNCTIONAL DESCRIPTION

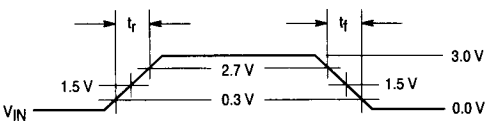
The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

4

AC TEST CIRCUIT

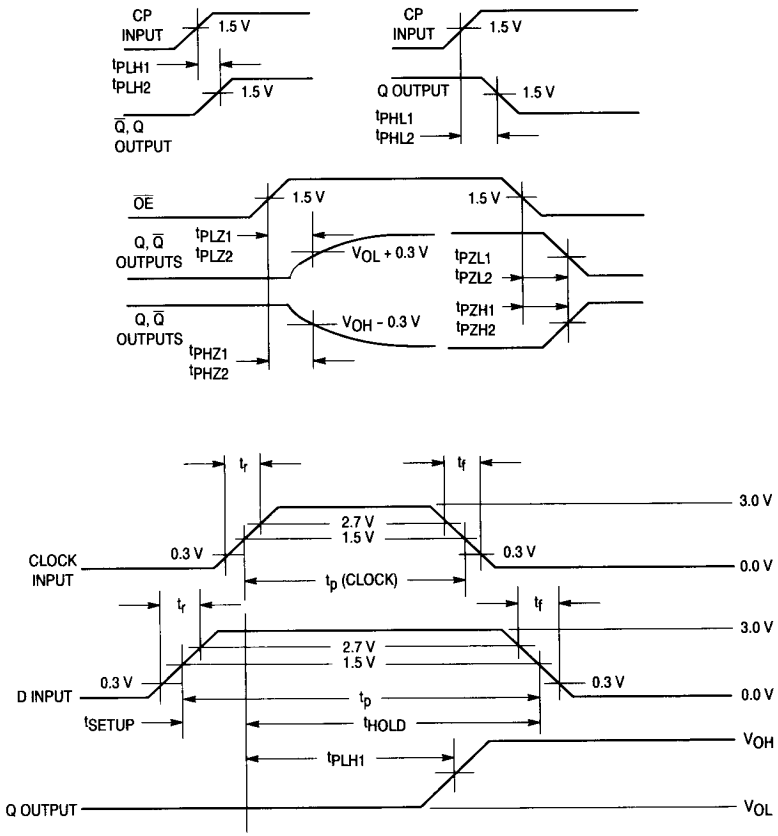


Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed



REFERENCE NOTES ON PAGE 4-219

WAVEFORMS



NOTES:
1. $t_r = t_f \leq 2.5$ ns.
2. PRR as in table, duty cycle 50 ± 15%.
3. When testig f_{MAX}, the output frequency shall be 1/2 the input frequency.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IL} = 0.8 V (all inputs), CP = (See Note 6).
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IH} = 2.0 V (all inputs), CP = (See Note 6), $\overline{OE}$ = 0.8 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V (all inputs).
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V (all inputs).
I_{OD}	Diode Current	35		35		35		mA	V_{CC} = 4.5 V, V_{IN} = 5.5 V (all inputs), $\overline{OE}$ = 0 V, CP = (See Note 6), V_{OUT} = 2.5 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V (all inputs).
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), V_{OUT} = 0 V, CP = (See Note 6).
I_{IOZH}	Output Off Current High		50		50		50	µA	V_{CC} = 5.5 V, V_{IN} = 2.7 V (all inputs), V_{OUT} = 2.7 V, $\overline{OE}$ = 2.0 V, CP = (See Note 6).
I_{IOZL}	Output Off Current Low		−50		−50		−50	µA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), V_{OUT} = 0.5 V, $\overline{OE}$ = 2.0 V, CP = (See Note 6).
I_{CCZ}	Power Supply Current Off		86		86		86	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**) V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2}	Propagation Delay /Data-Output CP to $\overline{Q}_n$	4.0	8.5	4.0	11	4.0	11	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output CP to $\overline{Q}_n$	4.0	8.5	4.0	10.5	4.0	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLZ2}	Propagation Delay /Data-Output $\overline{OE}$ to $\overline{Q}_n$	1.5	5.5	1.5	7.5	1.5	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHZ2}	Propagation Delay /Data-Output $\overline{OE}$ to $\overline{Q}_n$	1.5	7.0	1.5	8.0	1.5	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZL2}	Propagation Delay /Data-Output $\overline{OE}$ to $\overline{Q}_n$	2.0	7.5	2.0	10	2.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZH2}	Propagation Delay /Data-Output $\overline{OE}$ to $\overline{Q}_n$	2.0	11.5	2.0	14	2.0	14	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
f_{MAX}	Maximum Clock Frequency	80		60		60		MHz	V_{CC} = 5.0 V, C_L = 50 pF, (See Note 7).
$t_{s(H)}$	Setup Time, HIGH D_n to CP	2.5		2.5		2.5		ns	V_{CC} = 5.0 V, C_L = 50 pF, (See Note 7).
$t_{s(L)}$	Setup Time, LOW D_n to CP	2.0		2.0		2.0		ns	V_{CC} = 5.0 V, C_L = 50 pF, (See Note 7).
$t_{h(H)}$	Hold Time, HIGH D_n to CP	2.0		2.0		2.0		ns	V_{CC} = 5.0 V, C_L = 50 pF, (See Note 7).
$t_{h(L)}$	Hold Time, LOW D_n to CP	2.5		2.5		2.5		ns	V_{CC} = 5.0 V, C_L = 50 pF, (See Note 7).

NOTES:
1. V_{IN} = Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = R_2$ = 499 Ω ± 5.0%.
6. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to CP, then make measurement.
7. This is for information only, no test required.
8. f_{MAX} minimum limit specified is the frequency of the input pulse. The output frequency shall be 1/2 the input frequency.