

4K × 4 Bit Static Random Access Memory

The MCM6168 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other high speed applications.

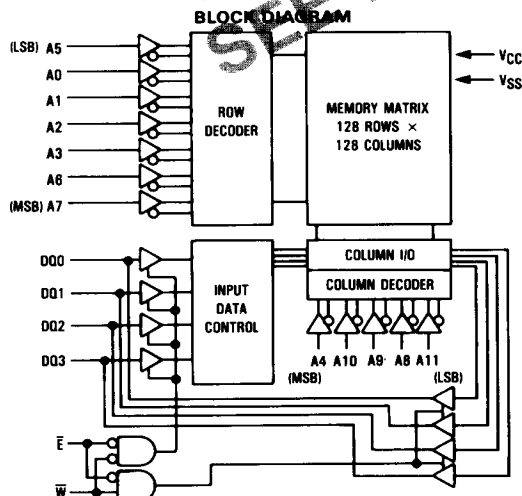
The chip enable (\bar{E}) pin is not a clock. In less than a cycle time after \bar{E} goes high, the part enters a low-power standby mode, remaining in that state until \bar{E} goes low again. This feature provides reduced system power requirements without degrading access time performance.

The MCM6168 is available in a 300 mil, 20 lead plastic dual-in-line package with the standard JEDEC pinout.

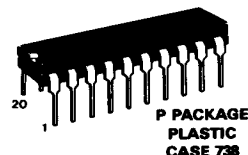
- Single 5 V Supply, $\pm 10\%$
- 4K × 4 Bit Organization
- Fully Static—No Clock or Timing Strokes Necessary
- Three State Output
- Fast Access Time (Maximum):

| | Address | Chip Enable |
|------------|---------|-------------|
| MCM6168-45 | 45 ns | 45 ns |
| MCM6168-55 | 55 ns | 55 ns |
| MCM6168-70 | 60 ns | 70 ns |

- Low Power Operation: 10 mA Max (Active)
20 mA Max (Standby—TTL Levels)
2 mA Max (Standby—CMOS Levels)
- Fully TTL Compatible



MCM6168



PIN ASSIGNMENT

| | | | |
|-----------|----|----|-----------|
| A4 | 1 | 20 | VCC |
| A5 | 2 | 19 | A3 |
| A6 | 3 | 18 | A2 |
| A7 | 4 | 17 | A1 |
| A8 | 5 | 16 | A0 |
| A9 | 6 | 15 | DQ0 |
| A10 | 7 | 14 | DQ1 |
| A11 | 8 | 13 | DQ2 |
| \bar{E} | 9 | 12 | DQ3 |
| VSS | 10 | 11 | \bar{W} |

PIN NAMES

| | |
|-----------|-------------------|
| A0-A11 | Address Input |
| \bar{W} | Write Enable |
| \bar{E} | Chip Enable |
| DQ0-DQ3 | Data Input/Output |
| VCC | +5 V Power Supply |
| VSS | Ground |

TRUTH TABLE

| \bar{E} | \bar{W} | Mode | V_{CC} Current | I/O Pin |
|-----------|-----------|--------------|------------------|-----------|
| H | X | Not Selected | ISB1, ISB2 | High-Z |
| L | H | Read | I_{CC} | D_{out} |
| L | L | Write | I_{CC} | D_{in} |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

| Rating | Symbol | Value | Unit |
|--|----------------------|------------------------|------------------|
| Power Supply Voltage | V_{CC} | -0.5 to +7.0 | V |
| Voltage Relative to V_{SS} for Any Pin Except V_{CC} | V_{in} , V_{out} | -0.5 to $V_{CC} + 0.5$ | V |
| Output Current (per I/O) | I_{out} | ± 20 | mA |
| Power Dissipation ($T_A = 25^\circ\text{C}$) | P_D | 1.0 | W |
| Temperature Under Bias | T_{bias} | -10 to +85 | $^\circ\text{C}$ |
| Operating Temperature | T_A | 0 to +70 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -55 to +125 | $^\circ\text{C}$ |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 10\%$, $T_A = 0$ to 70°C , Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|----------|------|-----|----------------|------|-------|
| Supply Voltage (Operating Voltage Range) | V_{CC} | 4.5 | 5.0 | 5.5 | V | |
| Input High Voltage | V_{IH} | 2.0 | — | $V_{CC} + 0.3$ | V | 1 |
| Input Low Voltage | V_{IL} | -0.3 | — | 0.8 | V | 1, 2 |

DC CHARACTERISTICS

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|-------------|-----|-----------|---------------|-------|
| Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC}) | $I_{lk}(I)$ | — | ± 1.0 | μA | |
| Output Leakage Current ($\bar{E} = V_{IH}$ or $\bar{W} = V_{IL}$, $V_{out} = 0$ to V_{CC}) | $I_{lk}(O)$ | — | ± 2.0 | μA | 3 |
| Power Supply Current ($\bar{E} = V_{IL}$, $I_{out} = 0$ mA) | I_{CC} | — | 80 | mA | 3 |
| TTL Standby Current ($\bar{E} = V_{IH}$) | I_{SB1} | — | 20 | mA | |
| CMOS Standby Current ($\bar{E} \geq V_{CC} - 0.2\text{ V}$, $V_{in} \leq 0.2\text{ V}$ or $\geq V_{CC} - 0.2\text{ V}$) | I_{SB2} | — | 2 | mA | |
| Output Low Voltage ($I_{OL} = 8.0$ mA) | V_{OL} | — | 0.4 | V | |
| Output High Voltage ($I_{OH} = -4.0$ mA) | V_{OH} | 2.4 | — | V | |

CAPACITANCE ($f = 1.0\text{ MHz}$, $T_A = 25^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)

| Characteristic | Symbol | Typ | Max | Unit |
|-------------------|-----------|-----|-----|------|
| Input Capacitance | C_{in} | 3 | 5 | pF |
| | | 5 | 7 | |
| I/O Capacitance | $C_{I/O}$ | 5 | 7 | pF |

NOTES:

- Address rise and fall times while the chip is selected are 50 ns maximum.
- $V_{IL}(\text{min}) = -0.3\text{ V dc}$; $V_{IL}(\text{min}) = -3.0\text{ V ac}$ (pulse width $\leq 20\text{ ns}$).
- Input levels less than -0.3 V or greater than $V_{CC} + 0.3\text{ V}$ will cause I/O and power supply currents to exceed maximum rating.

AC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V Output Timing Measurement Reference Level 0.8 and 2.0 V
Input Pulse Levels 0 to 3.0 V Output Load Figure 1A Unless Otherwise Noted
Input Rise/Fall Time 5 ns

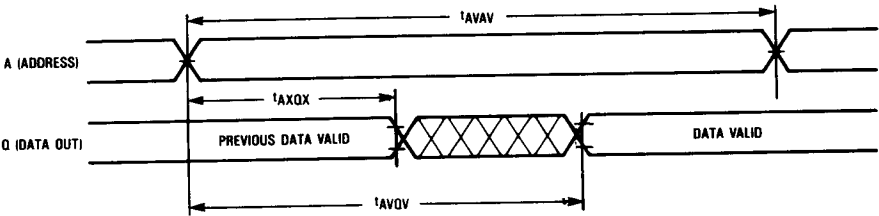
READ CYCLE (See Note 1)

| Parameter | Symbol | | MCM6168-46 | | MCM6168-55 | | MCM6168-70 | | Unit | Notes |
|---------------------------------|---------------------|------------------|------------|-----|------------|-----|------------|-----|------|-------|
| | Standard | Alternate | Min | Max | Min | Max | Min | Max | | |
| Read Cycle Time | t _{AVAV} | t _{RC} | 45 | — | 55 | — | 70 | — | ns | |
| Address Access Time | t _{AVQV} | t _{AA} | — | 45 | — | 50 | — | 60 | ns | |
| \bar{E} Access Time | t _{ELQV} | t _{ACS} | — | 45 | — | 55 | — | 70 | ns | |
| \bar{E} Low to Output Active | t _{ELOX} | t _{LZ} | 10 | — | 10 | — | 10 | — | ns | 2, 3 |
| \bar{E} High to Output High-Z | t _{EHQZ} | t _{HZ} | 0 | 15 | 0 | 20 | 0 | 25 | ns | 2, 3 |
| Output Hold from Address Change | t _{AXQX} | t _{OH} | 5 | — | 5 | — | 5 | — | ns | |
| Power Up Time | t _{ELICCH} | t _{PU} | 0 | — | 0 | — | 0 | — | ns | |
| Power Down Time | t _{EHICCL} | t _{PD} | — | 45 | — | 55 | — | 70 | ns | |

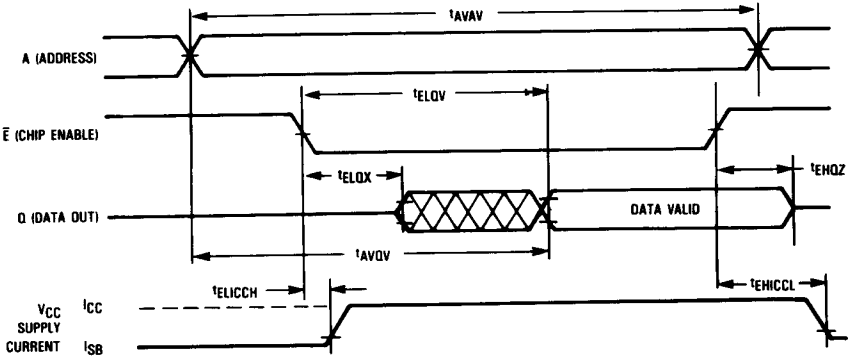
NOTES:

1. \bar{W} is high for read cycle.
2. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
3. This parameter is sampled and not 100% tested.
4. Device is continuously selected (\bar{E} = V_{IL}).
5. Addresses valid prior to or coincident with \bar{E} going low.

READ CYCLE 1 (See Note 4 Above)



READ CYCLE 2 (See Note 5 Above)

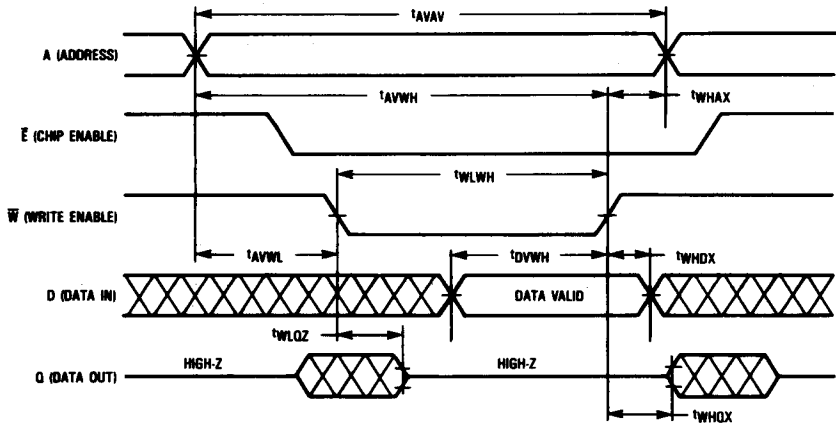


WRITE CYCLE 1 (\overline{W} Controlled; See Note 1)

| Parameter | Symbol | | MCM6168-45 | | MCM6168-55 | | MCM6168-70 | | Unit | Notes |
|-------------------------------|------------|-----------|------------|-----|------------|-----|------------|-----|------|-------|
| | Standard | Alternate | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | t_{AVAV} | t_{WC} | 40 | — | 50 | — | 60 | — | ns | |
| Address Setup Time | t_{AVWL} | t_{AS} | 0 | — | 0 | — | 0 | — | ns | |
| Address Valid to End of Write | t_{AVWH} | t_{AW} | 35 | — | 45 | — | 55 | — | ns | |
| Write Pulse Width | t_{WLWH} | t_{WP} | 35 | — | 45 | — | 55 | — | ns | |
| Data Valid to End of Write | t_{DVWH} | t_{DW} | 15 | — | 20 | — | 25 | — | ns | |
| Data Hold Time | t_{WHDX} | t_{DH} | 3 | — | 3 | — | 3 | — | ns | |
| Write Low to Output High-Z | t_{WLOZ} | t_{WZ} | — | 20 | — | 25 | — | 30 | ns | 2, 3 |
| Write High to Output Active | t_{WHQX} | t_{QW} | 5 | — | 5 | — | 5 | — | ns | 2, 3 |
| Write Recovery Time | t_{WHAX} | t_{WR} | 5 | — | 5 | — | 5 | — | ns | |

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. Transition is measured ± 500 mV from steady-state voltage with load in Figure 1B.
3. Parameter is sampled and not 100% tested.



AC TEST LOADS

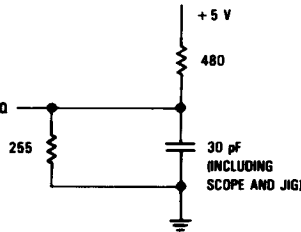


Figure 1A

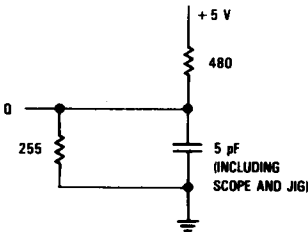


Figure 1B

TIMING LIMITS

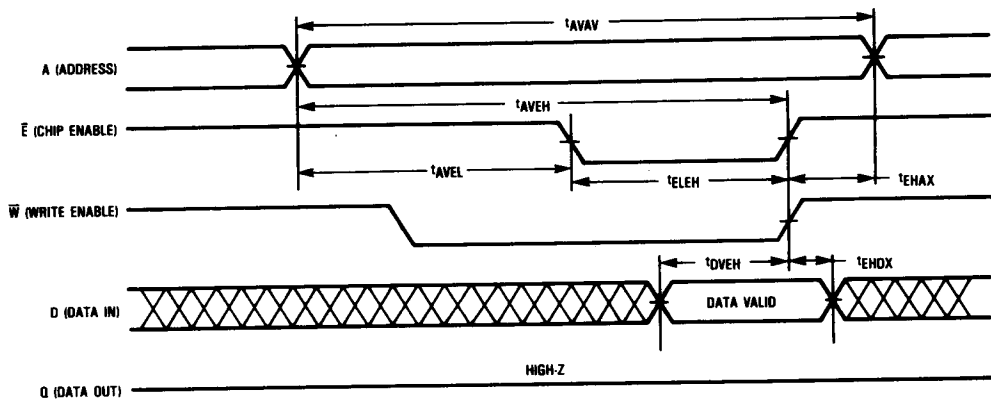
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 (\bar{E} Controlled; See Note 1)

| Parameter | Symbol | | MCM6168-45 | | MCM6168-55 | | MCM6168-70 | | Unit | Notes |
|-------------------------------|------------|-----------|------------|-----|------------|-----|------------|-----|------|-------|
| | Standard | Alternate | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | t_{AVAV} | t_{WC} | 40 | — | 50 | — | 60 | — | ns | |
| Address Setup Time | t_{AVEL} | t_{AS} | 0 | — | 0 | — | 0 | — | ns | |
| Address Valid to End of Write | t_{AVEH} | t_{AW} | 35 | — | 45 | — | 55 | — | ns | |
| Write Pulse Width | t_{ELEH} | t_{CW} | 35 | — | 45 | — | 55 | — | ns | 2, 3 |
| Data Valid to End of Write | t_{DVEH} | t_{DW} | 15 | — | 20 | — | 25 | — | ns | |
| Data Hold Time | t_{EHDX} | t_{DH} | 3 | — | 3 | — | 3 | — | ns | |
| Write Recovery Time | t_{EHAX} | t_{WR} | 5 | — | 5 | — | 5 | — | ns | |

NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high impedance condition.
3. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high impedance condition.

ORDERING INFORMATION
(Order by Full Part Number)