

128 K x 8 / 3.3 V Very Low Power CMOS SRAM

Introduction

The L65608 is a very low power CMOS static RAM organized as 131072×8 bits. It is manufactured using the TEMIC high performance CMOS technology named SCMOS.

The L65608 provides fast access time of 45 ns for a 3 Volts power supply.

Utilizing an array of six transistors (6T) memory cells, the L65608 combines an extremely low standby supply current (Typical value = $0.1 \mu\text{A}$) with a fast access time

at 45 ns over the full commercial and military temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

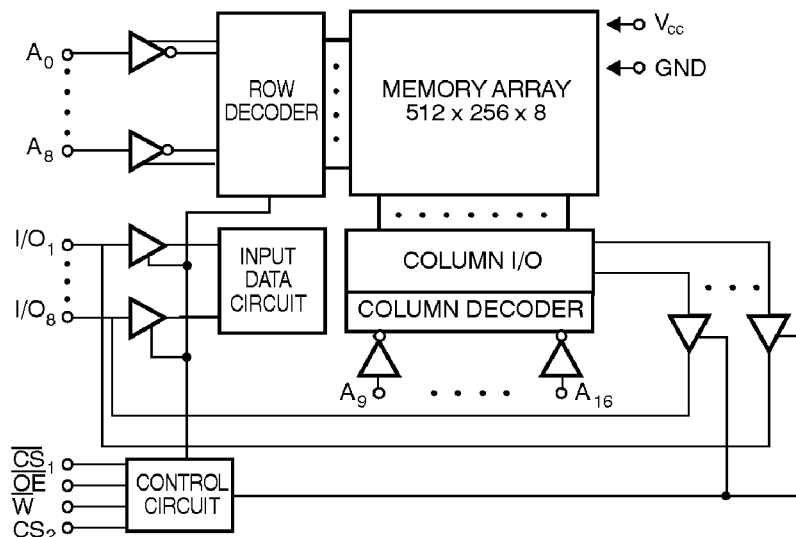
For military/space applications that demand superior levels of performance and reliability the L65608 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

Features

- Single 3.3 ± 0.3 volts supply
- Access time : commercial : 45/55/70 ns
industrial and military : 45/55/70 ns
- Very low power consumption
active : 150 mW (Typ)
standby : $0.3 \mu\text{W}$ (Typ)
data retention : $0.2 \mu\text{W}$ (Typ)
- Wide temperature Range : -55 To $+125^\circ\text{C}$
- 400 Mils width package
- TTL compatible inputs and outputs
- Asynchronous
- Equal cycle and access time
- Gated inputs :
no pull-up/down
resistors are required

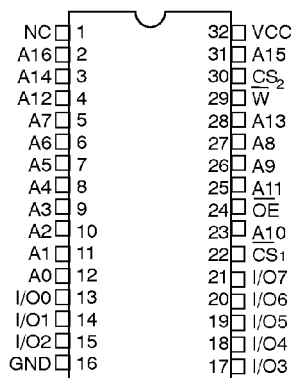
Interface

Block Diagram



Pin Configuration

32 pins DLCC ceramic 400 MILS
 32 pins DIL side-brazed 400 MILS
 32 pins Flatpack 400 MILS
 32 pins PDIL 400 MILS
 32 pins SOIC and SOJ 400 MILS



Pin Names

A0–A16	Address inputs
I/O0–I/O7	Data Input/Output
$\overline{CS}_1$	Chip select 1
CS_2	Chip select 2
$\overline{W}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

Truth Table

$\overline{CS}_1$	CS_2	$\overline{W}$	$\overline{OE}$	INPUTS/ OUTPUTS	MODE
H	X	X	X	Z	Deselect/ Power-down
X	L	X	X	Z	Deselect/ Power Down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Output Disable

L = low, H = high, X = H or L, Z = high impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : - 0.5 V + 7.0 V

DC input voltage : GND – 0,3 V to VCC + 0,3

DC output voltage high Z state : GND – 0,3 V to VCC + 0,3

Storage temperature : –65 °C to + 150 °C

Output current into outputs (low) : 20 mA

Electro statics discharge voltage : > 2 001 V
(MIL STD 883D method 3015.3)

Operating Range

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	3.3 V ± 0.3 V	– 55 °C to + 125 °C
Industrial	3.3 V ± 0.3 V	– 40 °C to + 85 °C
Commercial	3.3 V ± 0.3 V	0 °C to + 70 °C

Recommended DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	3	3.3	3.6	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	GND – 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC + 0.3	V

Capacitance

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (1)	Input low voltage	–	–	8	pF
Cout (1)	Output high volt	–	–	8	pF

Note : 1. Guaranteed but not tested.

DC Parameters

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 1	–	1	μA
IOZ (2)	Output leakage current	– 1	–	1	μA
VOL (3)	Output low voltage	–	–	0.4	V
VOH (4)	Output high voltage	2.4	–	–	

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output Disabled.

3. Vcc min. IOL = 6 mA.

4. Vcc min. IOH = –2.0 mA.

Consumption for Commercial

SYMBOL	DESCRIPTION	65608L/V – 45	65608L/V – 55	65608L/V – 70	UNIT	VALUE
ICCSB (5)	Standby supply current	3/1	3/1	3/1	mA	max
ICCSB ₁ (6)	Standby supply current	400/40	400/40	400/40	μA	max
ICCOP (7)	Dynamic operating current	70/50	65/45	60/40	mA	max

Consumption for Industrial

SYMBOL	DESCRIPTION	65608L/V – 45	65608L/V – 55	65608L/V – 70	UNIT	VALUE
ICCSB (5)	Standby supply current	3/1	3/1	3/1	mA	max
ICCSB ₁ (6)	Standby supply current	600/80	600/80	600/80	μA	max
ICCOP (7)	Dynamic operating current	70/50	65/45	60/40	mA	max

Consumption for Military

SYMBOL	DESCRIPTION	65608L/V – 45	65608L/V – 55	65608L/V – 70	UNIT	VALUE
ICCSB (5)	Standby supply current	3/1.5	3/1.5	3/1.5	mA	max
ICCSB ₁ (6)	Standby supply current	800/250	800/250	800/250	μA	max
ICCOP (7)	Dynamic operating current	70/50	65/45	60/40	mA	max

- Notes :**
5. $\overline{CS}_1 \geq V_{IH}$ or $CS_2 \leq V_{IL}$ and $\overline{CS}_1 \leq V_{IL}$.
 6. $\overline{CS}_1 \geq V_{cc} - 0.3 \text{ V}$ or, $CS_2 < Gnd + 0.3 \text{ V}$ and $\overline{CS}_1 \leq 0.2 \text{ V}$
 7. $F = 1/T_{AVAV}$, $I_{out} = 0 \text{ mA}$, $\overline{W} = \overline{OE} = V_{IH}$, $V_{in} = Gnd/V_{cc}$, V_{cc} max.

AC Parameters

Input pulse levels : Gnd to 3.0 V

Input rise : 5 ns

Input timing reference levels : 1.5 V

Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

AC Test Loads Waveforms

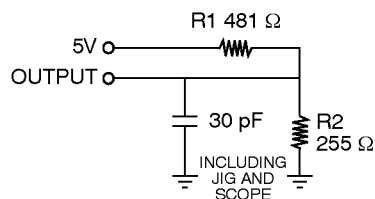


Figure 1a

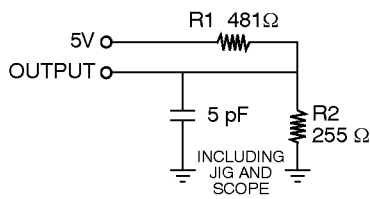


Figure 1b

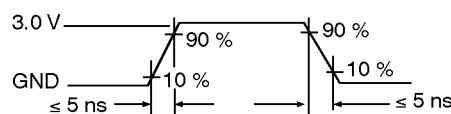
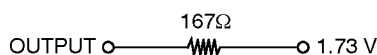


Figure 2

Equivalent to : THEVENIN EQUIVALENT



Data Retention Mode

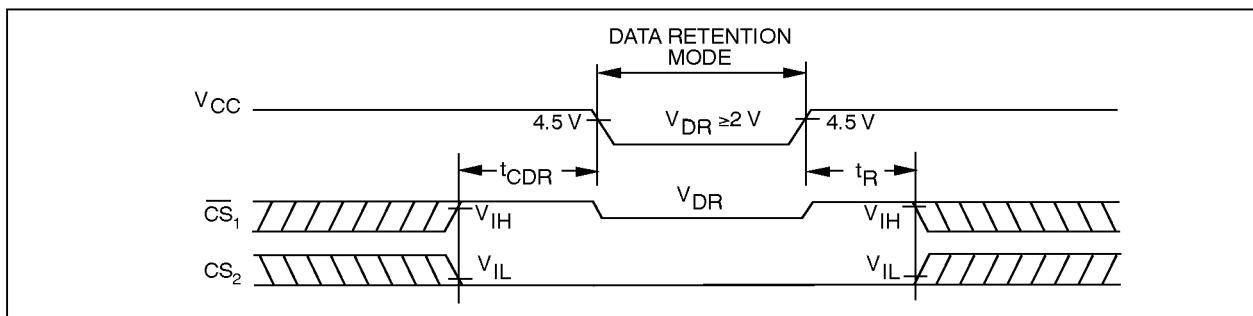
MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. . During data retention chip select $\overline{CS}_1$ must be held high within VCC to VCC -0.2 V or, chip select CS₂

must be held low within GND to GND + 0.2 V.

2. During power up and power down transitions $\overline{CS}_1$ must be kept between VCC + 0.3 V and 70 % of VCC, or with CS₂ between GND and GND - 0.3 V.
3. The RAM can begin operation > 45 ns after Vcc reaches the minimum operation voltages (4.5 V).

Timing



Data Retention Characteristics

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL $T_A = 25^\circ\text{C}$	MAXIMUM			UNIT
VCCDR	Vcc for data retention	2.0	—	—			V
TCDR	Chip deselect to data retention time	0.0	—	—			ns
TR	Operation recovery time	TAVAV (9)	—	—			ns
ICCDR1 (10)	Data retention current @ 2.0 V : L-65608-V L-65608-L	—	0.1 0.1	COM	IND	MIL	μA
				20	40	150	
				200	300	500	

Notes : 9. TAVAV = Read cycle time.

10. $\overline{CS}_1 = \text{Vcc}$ or $\text{CS}_2 = \overline{\text{CS}}_1 = \text{GND}$, $\text{Vin} = \text{Gnd/Vcc}$.

Write Cycle

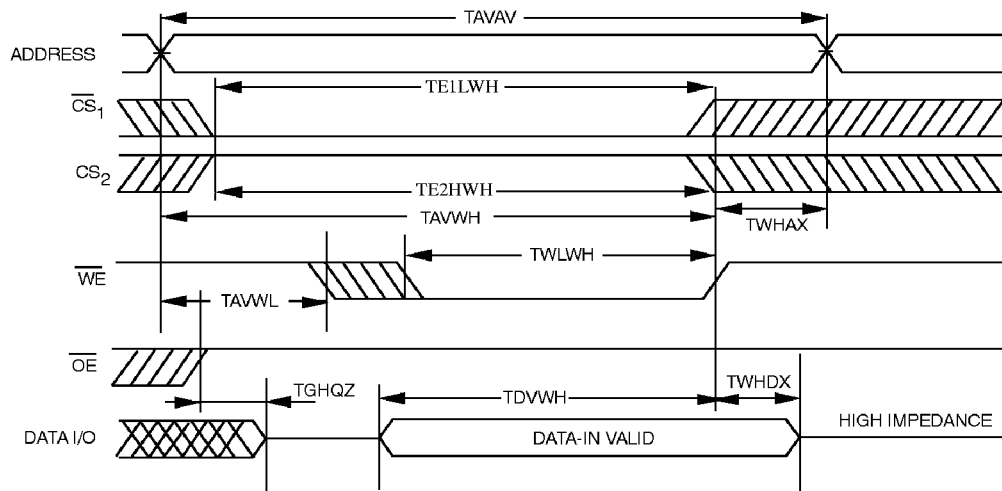
SYMBOL	PARAMETER	65608L/V – 45	65608L/V – 55	65608L/V – 70	UNIT	VALUE
TAVAW	Write cycle time	45	55	70	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	35	45	60	ns	min
TDVWH	Data set-up time	25	35	50	ns	min
TE ₁ LWH	$\overline{CS}_1$ low to write end	35	45	60	ns	min
TE ₂ HWH	CS ₂ high to write end	35	45	60	ns	min
TWLQZ	Write low to high Z (11)	15	15	20	ns	max
TWLWH	Write pulse width	35	45	60	ns	min
TWHAX	Address hold from to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX	Write high to low Z (11)	0	0	0	ns	min

Read Cycle

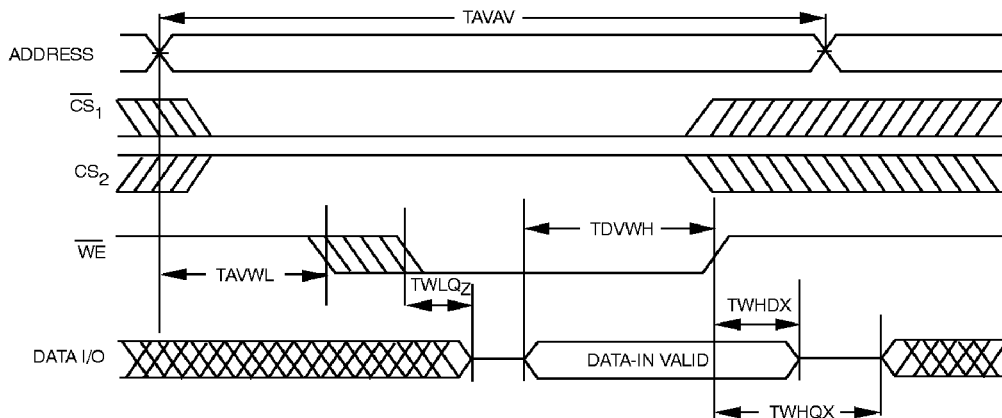
SYMBOL	PARAMETER	65608L/V – 45	65608L/V – 55	65608L/V – 70	UNIT	VALUE
TAVAV	Read cycle time	45	55	70	ns	min
TAVQV	Address access time	45	55	70	ns	max
TAVQX	Address valid to low Z	10	10	10	ns	min
TE ₁ LQV	Chip-select ₁ access time	45	55	70	ns	max
TE ₁ LQX	$\overline{CS}_1$ low to low Z (11)	10	10	10	ns	min
TE ₁ HQZ	$\overline{CS}_1$ high to high Z (11)	20	20	25	ns	max
TE ₂ HQV	Chip-select ₂ access time	45	55	70	ns	max
TE ₂ HQX	CS ₂ high to low Z (11)	10	10	10	ns	min
TE ₂ LQZ	CS ₂ low to high Z (11)	20	20	25	ns	max
TGLQV	Output Enable access time	20	25	30	ns	max
TGLQX	$\overline{OE}$ low to low Z (11)	10	10	10	ns	min
TGHQZ	$\overline{OE}$ high to high Z (11)	15	15	20	ns	max

Notes : 11. Parameters guaranteed, not tested, with output loading 5 pF. (see fig. 1.b.).

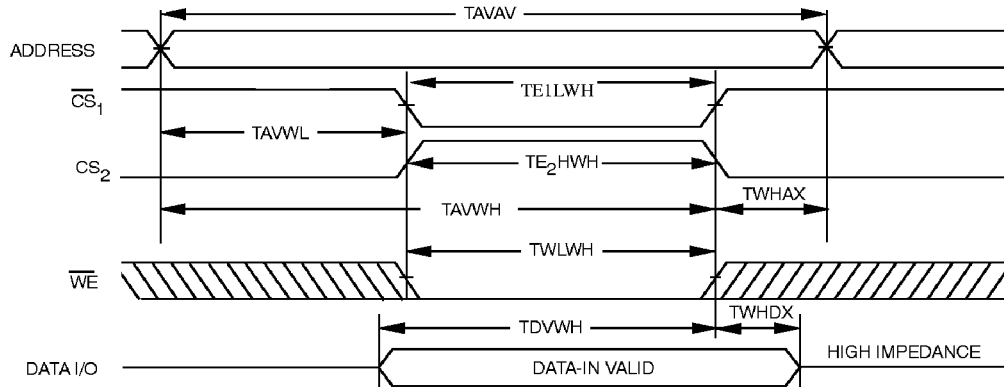
Write Cycle 1. $\overline{W}$ Controlled. $\overline{OE}$ High During Write



Write Cycle 2. $\overline{W}$ Controlled. $\overline{OE}$ Low

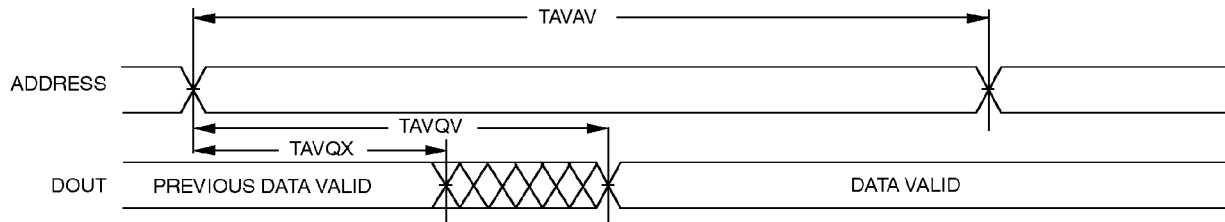


Write Cycle 3. $\overline{CS}_1$ or CS_2 Controlled.

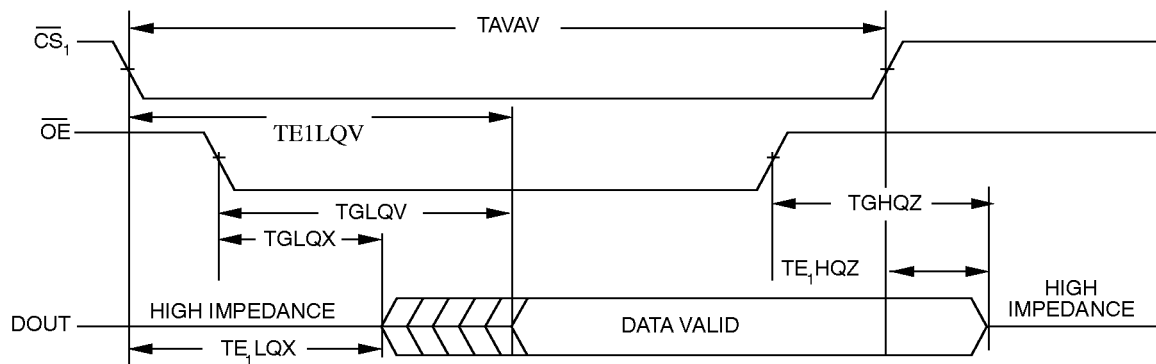


Note : 12. The internal write time of the memory is defined by the overlap of $\overline{CS}_1$ Low and CS_2 HIGH and $\overline{WE}$ LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in activated. The data input setup and hold timing should be referenced to the activated edge of the signal that terminates the write. Data out is high impedance if $\overline{OE} = V_{IH}$.

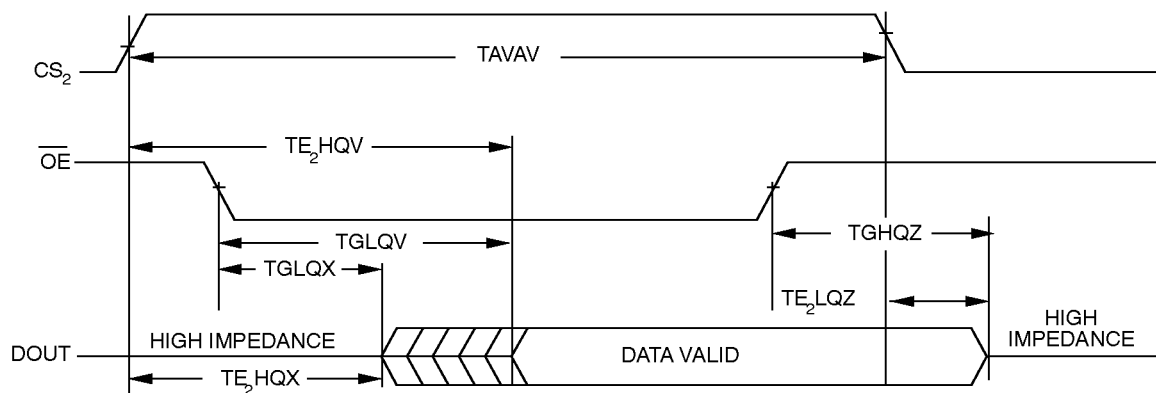
Read Cycle nb 1



Read Cycle nb 2



Read Cycle nb 3



Ordering Information

TEMPERATURE RANGE		PACKAGE	DEVICE	GRADE	SPEED	FLOW
M	L	C9	- 65608	V	- 45	
C = Commercial 0° to +70°C I = Industrial -40° to +85°C M = Military -55° to +125°C			128K × 8 STATIC RAM	L = Low power V = Very low power	45 ns 55 ns 70ns	
		C9 = Side Brazed 32 pins 400 mils DJ = Flat Package 32 pins 400 mils 4J = Dual LCC 32 pins 39 = Plastic DIL 32 pins 400 mils T1 = 32 pins SOIC 400 mils U1 = 32 pins SOJ 400 mils 0 = die			blank = MHS standards /883 = MIL STD 883 Class B or S P883 = MIL STD 883 + PIND test SB/SC = SCC 9000 level B/C SHXXX = Special customer request FHXXX = Flight models (space) EHXXX = Engineering models (space) MHXXX = Mechanical parts (space) LHXXX = Life test parts (space) : R = Tape and reel : RD = Tape and reel dry pack : D = Dry pack	

Military and Space Versions

The following table gives package/consumption/access time/process flow available combinations

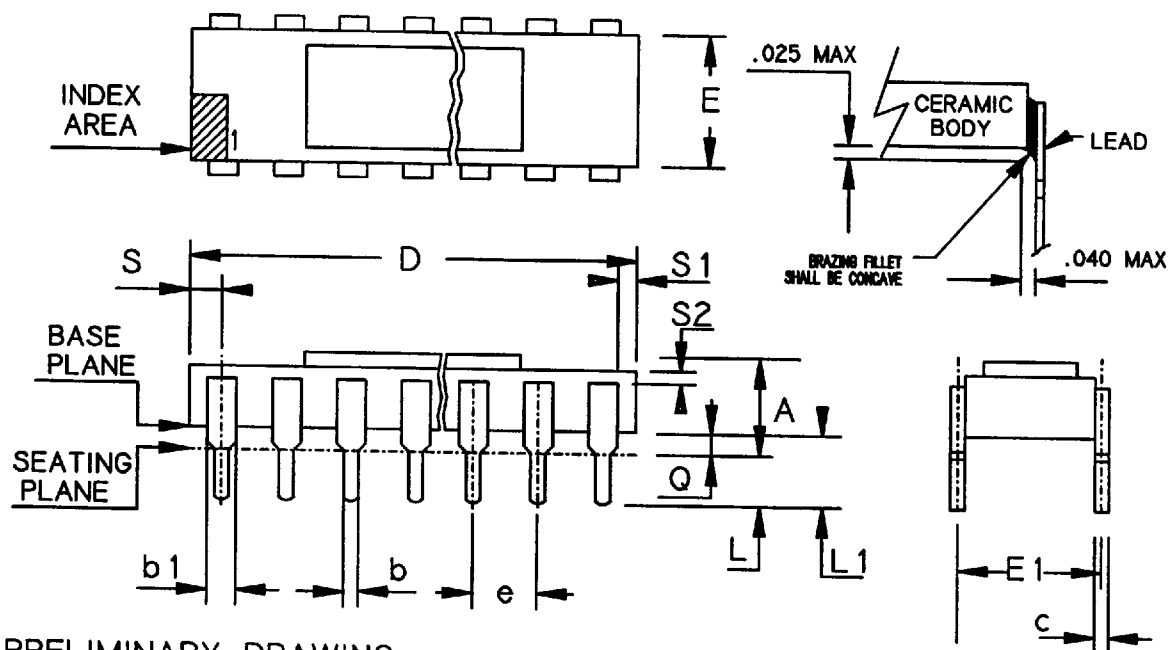
Temp range	Packages	Consumption		Access Time (ns)		Std process 65608	RT process 65608E	
		V	L	55	70	Mil flows (including SMD5962-89598)	Mil flows	Space flows
M	C9 DJ 4J 0	● X X X	● X X ●	● X X ●	● X X ●	● X X ●		
S	C9 DJ 4J 0	● X X X	● ● ● ●	● X X ●	● X X ●		● X X ●	● X X ●

● = product in production

X = call sales office for availability

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32 LEAD SIDE BRAZE .400



PRELIMINARY DRAWING

	MM		INCH	
A	3.22	4.30	.013	.170
b	0.40	0.51	.016	.020
b1	1.27 TYP		0.05 TYP	
c	0.23	0.30	.009	.012
D	40.26	41.02	1.585	1.615
E	9.78	10.29	.385	.405
E1	9.90	10.41	.390	.410
e	2.54	BSC	.100	BSC
L	1.66	4.06	.065	.160
L1	3.18	5.08	.125	.200
Q	1.02	1.52	.040	.050
S	-	1.65	-	.065
S1	0.13	-	.005	-
S2	0.13	-	.005	-

DON'T EXIST IN MIL STD 1835

CODE : C9

REV : 0 DATE : 23-03-93