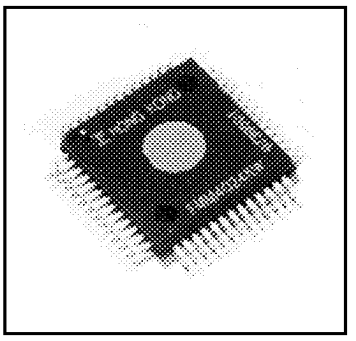
FMM4024KW

1.0625Gbps FIBRE CHANNEL REPEATER IC

FEATURES

- 1.0625Gbps Repeater IC for FIBRE CHANNEL (Hubs/Disk Arrays)
- Low Power Consumption: 0.5W
- Single Power Supply Voltage: +3.3V
- LVTTL and PECL Interface
- Thermally Enhanced, QFP52 Mold Package with Heat Sink



KW PACKAGE

DESCRIPTION

The FMM4024 is a one-chip monolithic repeater designed with 0.5µm GaAs MESFET technology for 1.0625Gbps Fibre Channel applications. Small Computer Systems Interface (SCSI) is the common interface medium for large computer systems and peripherals today. Advances in multimedia have significantly increased the demand for high speed data transmission interfaces. Fibre Channel products are the next generation of serial interface which are capable of Gbps data transmission rates.

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta = 25°C)

Parameter		Symbol	Values	Unit
Supply Voltage		V_{DD}	-0.5 ~ +4.0	V
Output Current	PECL	I_{OUT}	-50 ~ +50	mA
	LVTTL	I_{OUT}	-25 ~ +25	mA
Input Voltage	PECL	V_{IN}	-0.5 ~ VDD+0.5	V
	LVTTL	V_{IN}	-0.5 ~ 0.5	V
Maximum Input ESD (MIL-STD-883C)		V_{ESD}	1500	V
Storage Temperature		T_{STG}	-65 ~ +150	°C
Case Temperature		T_C	-55 ~ +120	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values	Unit
Supply Voltage	V_{DD}	+3.3 ±5%	V
AC Coupled Differential PECL Output Load	R_L	50	Ω
Ambient Temperature	T_A	0 ~ +70	°C
Junction Temperature	T_J	0 ~ +100	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS for PECL (V_{DD}=3.3V, T_A=25°C)

Parameter	Symbol	Test Conditions	Limit		Unit
			Min.	Max.	
Single Ended Output Voltage Swing	V_{OUT}	50Ω to V_{DD} -2.0V	600	1300	mV
Differential Output Voltage Swing	V_{OUTD}	50Ω to V_{DD} -2.0V	1200	2400	mV
Differential Input Voltage Swing	V_{IND}	–	200	2600	mV

DC CHARACTERISTICS FOR LVTTL (V_{DD}=3.3V, T_A=25°C)

Parameter	Symbol	Test Conditions	Value		Unit
			Min.	Max.	
Output HIGH Voltage	V_{OH}	I_{OH}=-1.0mA	2.4	V_{DD}	V
Output LOW Voltage	V_{OL}	I_{OL}=+1.0mA	0	0.6	V
Input HIGH Voltage	V_{IH}	–	2.0	5.5	V
Input LOW Voltage	V_{IL}	–	0	0.8	V
Input HIGH Current	I_{IH}	V_{IN}=V_{DD} -0.5V	-	50	µA
Input LOW Current	I_{IL}	V_{IN}=0.5V	-500	-	µA

SUPPLY CURRENT (V_{DD}=3.3V, T_A=25°C)

Parameter	Symbol	Test Conditions	Limit		Unit
			Min.	Max.	
Supply Current	I_{DD1}	50Ω to V_{DD} -2.0V Repeater mode	–	170	mA
Supply Current	I_{DD2}	50Ω to V_{DD} -2.0V Hub mode	–	210	mA

AC CHARACTERISTICS (V_{DD}=3.3V, T_A=25°C)

Parameter	Symbol	Test Conditions	Value		Unit
			Min.	Max.	
Serial Baud Rate	B_R	–	1062.5	1062.5	Mbps
TBC Clock Rate	F_{tbc}	–	106.25	106.25	MHz
Frequency Offset	F_{off}	Frequency offset between RX data frequency and TBC	-100	+100	ppm
PECL Output Rise and Fall Time	T_{tr}, T_{tf}	20% to 80% 50Ω single ended load	-	300	pS
TTL Output Rise and Fall time	T_{ttr}, T_{ttf}	0.8 to 2.0V with 10pF load	-	2.4	nS
Frequency Lock Time	T_{FL}	–	-	500	µS
Bit Lock Time	T_{BL}	–	-	2500	bit
Random Jitter	J_{RC}	SO K28.7 Pattern Random Jitter (rms value)	-	10	pS
Deterministic Jitter	J_{DC}	SO K28.5 Pattern Deterministic Jitter (p-p)	-	100	pS

Block Diagram

The functional block diagram of the FMM4024 is shown in Figure 1. The RX/RXN pins are high speed serial input terminals. The PLL clock recovery unit recovers the high speed clock from RX/RXN input signal and re-times the RX/RXN signal. The SI/SIN pins are also high speed input terminals but are not re-timed. The RX/RXN is connected to SO/SON output terminals by PBCENI control signal. The SI/SIN signals are connected to the TX/TXN output terminals by TXEN1 or TXEN2 signal.

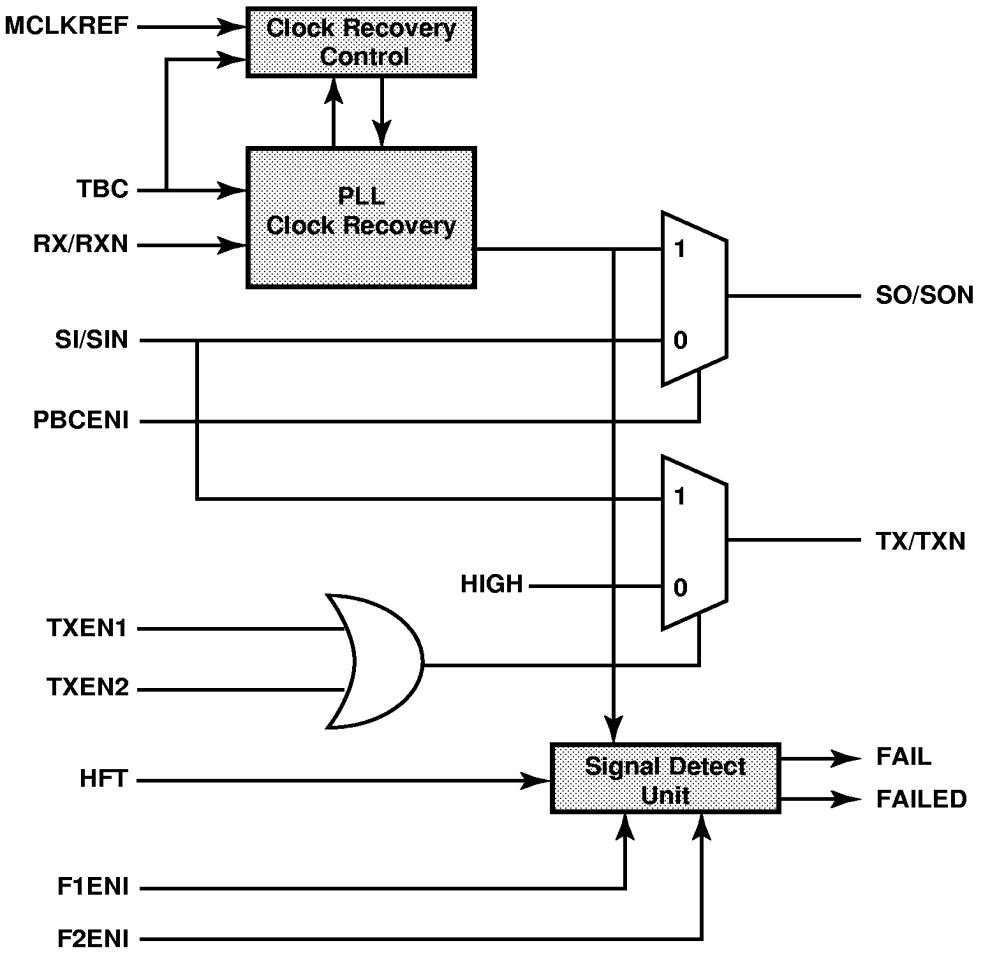


Figure 1: Functional Block Diagram of FMM4024KW

The functional block diagram of the Signal Detect Unit (SDU) is shown in Figure 2. The SDU checks the input format and detects the following words:

(1) 7-bit fixed low signal or 7-bit fixed high signal
(2) Comma word detection

The output of these two signals are available on the FAIL and FAILED terminals.

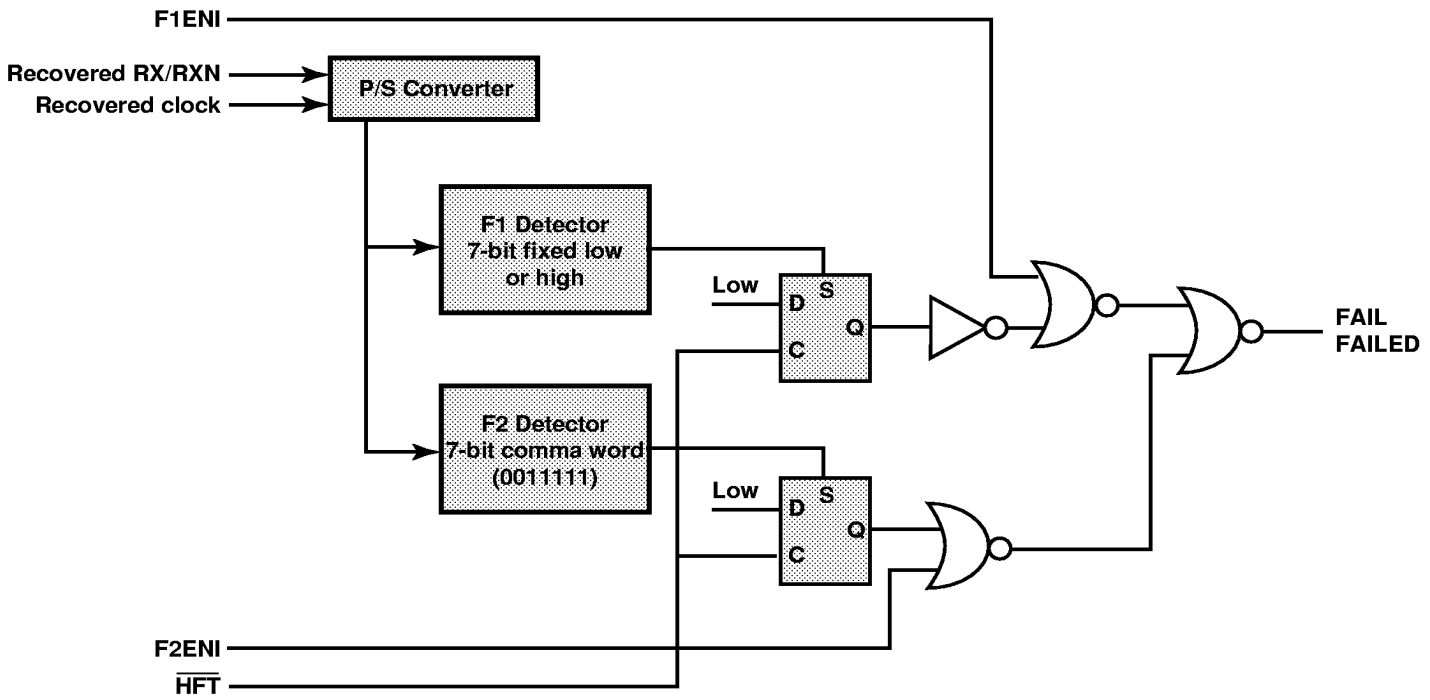


Figure 2: Functional Block Diagram of Signal Detect Unit (SDU)

The FMM4024 has two operational modes: Repeater mode and Hub mode.

Repeater Mode

Figure 3 shows the FMM4024 in repeater mode which re-times RX/RXN signals with outputs on SO/SON terminals. The PLL clock recovery unit (CRU) recovers clock signal from high speed input serial data. The CRU uses two methods to extract clock signal from the serial data. The first is manual clock recovery using the MCLKREF signal. The second method is auto clock recovery. The manual clock recovery technique is as follows:

(1) The MCLKREF signal must be low for more than 500µS in order to lock to TBC

(2) After 500µS, MCLKREF is set high to lock to input serial data

When MCLKREF is low, the CRU functions as a clock multiplier. TBC is used as the reference clock. When MCLKREF is high, the CRU functions as a phase aligner. The PLL aligns the phase to that of the input serial data.

When MCLKREF is high, the auto clock recovery compares the frequency between TBC and recovered clock. The fibre channel specification defines the allowable frequency offset (±100ppm) of the high speed signals. When the offset frequency between the recovered clock and 10 times TBC clock exceeds ±0.1%, the auto clock recovery circuit behaves as MCLKREF low.

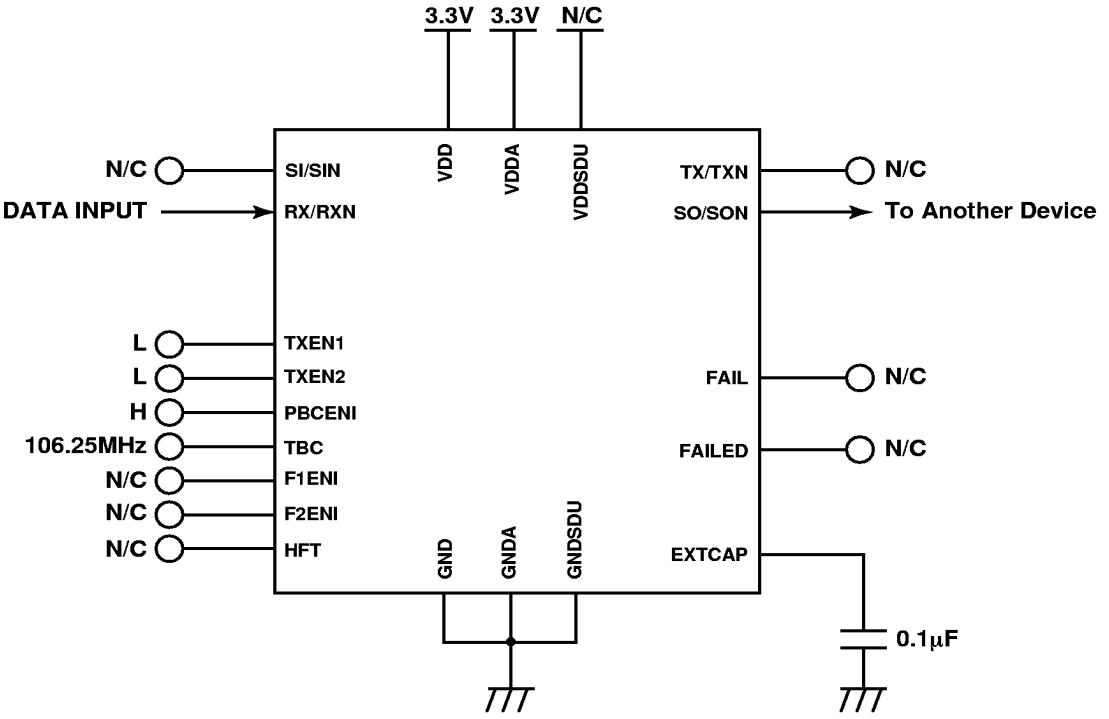


Figure 3: Repeater Mode Operation

Hub Mode

Figure 4 shows the FMM4024 in a Hub mode. The RX/RXN and SI/SIN signals are selected by PBCENI signal typically from an external Hub controller. When PBCENI is high, re-timed RX/RXN is connected to SO/SON. When PBCENI is low, SI/SIN is connected to TX/TXN. If RX/RXN signal has invalid Fibre channel data format, the SI/SIN signal is bypassed to SO/SON.

The external Hub controller monitors the FAIL signal at the rising edge of HFT. The FMM4024 resets the FAIL signal at the falling edge of HFT. If FAIL signal is low, an invalid signal was received by RX/RXN. The FAILED signal is the same as FAIL signal.

The FAIL signal will become low when the received signal from RX/RXN has the following conditions:

(1) Received signal contains 7-bit fixed low or 7-bit fixed high bit stream.

(2) Received signal does not contain 7-bit comma word during HFT cycle.

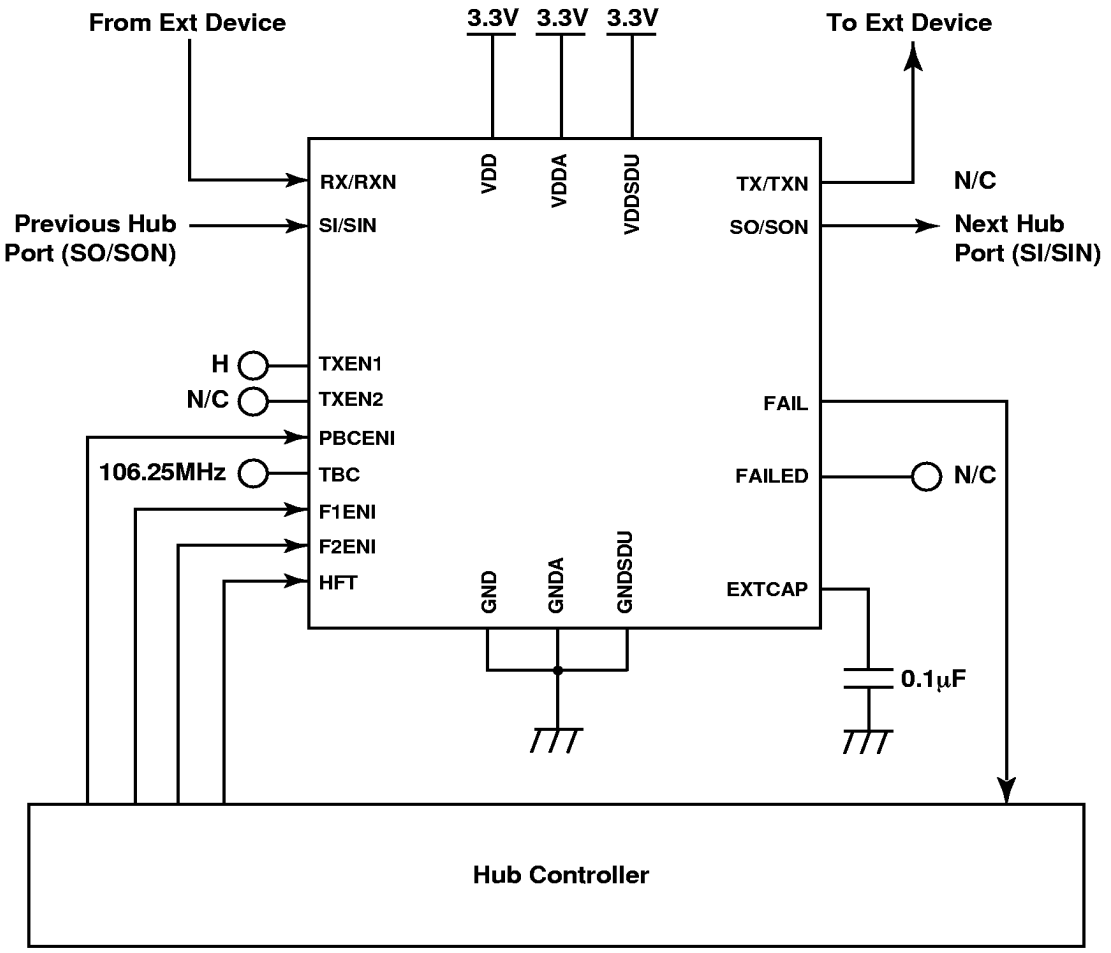


Figure 4: Hub Mode Operation

Package Information

The FMM4024 uses a standard, 10mm-size, thermally enhanced HQFP package. This package has a copper heat spreader for die attach to reduce the thermal resistance from the chip junction to the package surface.

Figure 5: Package Pin Assignment

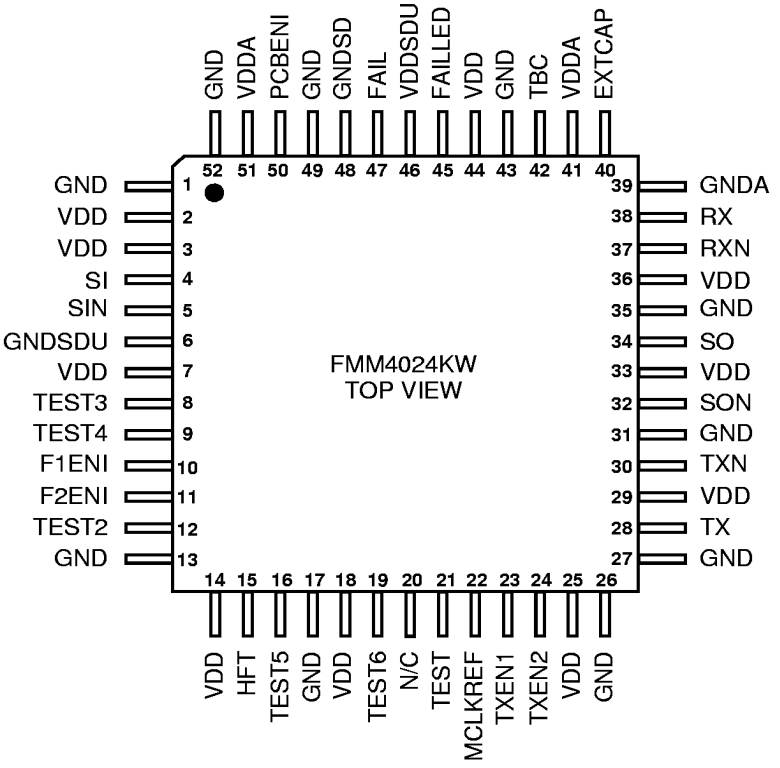


Table 1: Pin Description of Power Supply

Pin Name	Pin No.	Description
GND	1, 13, 17, 26, 27, 31, 35, 43, 52	**Ground for Logic Gates: 0V**
GNDSDU	6, 48	**Ground for Signal Detect Unit: 0V**
GNDA	39, 49	**Analog Ground: 0V**
VDD	2, 3, 7, 14, 18, 25, 29, 33, 36, 44	**Power Supply for Logic Gate: 3.3V**
VDDSDU	46	**Power Supply for Signal Detect Unit: 3.3V Leave open when in repeater mode.**
VDDA	41, 51	**Analog Power Supply: 3.3V**
N/C	20	**No connection**

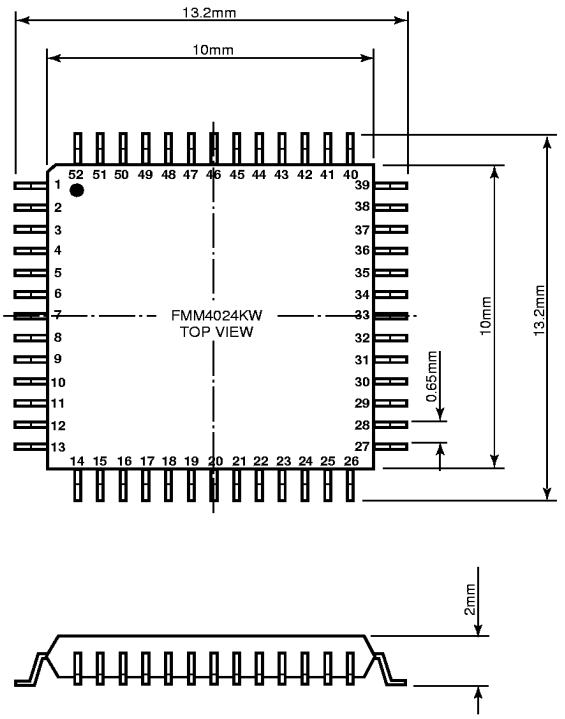
Table 2: Pin Description

Pin Name	Pin No.	I/O	Description
RX/RXN	38, 37	I-PECL	High Speed Serial Data Input to PLL clock recovery. These pins are internally biased to VDD/2 by internal resistors.
SI/SIN	4, 5	I-PECL	High Speed Serial Data Input to TX/TXN and port bypass circuit. These pins are internally biased to VDD/2 by internal resistors.
TBC	42	I-TTL	Transmit Byte Clock. This is the 106.25MHz reference clock. The clock recovery circuit and clock recovery control circuit use this clock as its reference clock. This clock signal must have good signal integrity.
HFT	15	I-TTL	Fault Detection Clock. The falling edge of HFT resets the F1 register (7-bit fixed high or low detection register) and F2 register (Comma word detection register).
PBCENI	50	I-TTL	Port Bypass Control. When PBCENI is high, recovered RX/RXN is connected to SO/SON. When PBCENI is low, SI/SIN is connected to SO/SON.
TXEN1 TXEN2	23 24	I-TTL	TX/TXN Output Control. When TXEN1 and TXEN2 are both low, TX level is fixed to high and TXN level is fixed to low. When TXEN1 or TXEN2 is high, SI/SIN is connected to TX/TXN. TXEN1 is internally pulled up and TXEN2 is internally pulled down.
F1ENI	10	I-TTL	F1 Register Output Control. When F1ENI is low, it enables the F1 register output.
F2ENI	11	I-TTL	F2 Register Output Control
SO/SON	34, 32	O-PECL	High Speed Serial Data Output. When PBCENI is high, recovered RX/RXN is connected to SO/SON.
TX/TXN	28, 30	O-PECL	High Speed Serial Data Output. These signals are controlled by TXEN1 and TXEN2.
FAIL FAILLED	47 45	O-TTL	Fault Detection Output. These two signals have the same logic function. When these signals are low, invalid fibre channel data was received at RX/RXN input signal. The outputs of F1 and F2 fault detection registers are enabled by F1ENI and F2ENI respectively.
MCLKREF	22	I-TTL	Master Clock Reference. When MCLKREF is low, PLL locks to TBC. When MCLKREF is high, PLL locks to recovered data. This pin is internally pulled up. For normal operation, leave it open.
TEST1 TEST2 TEST3 TEST4 TEST5 TEST6	21 12 8 9 16 19	I-TTL	Factory Test Pins. These signals used for factory test only. For normal operation, leave it open or tie to GND except for pin 12 which must be connected to high.
EXTCAP	40	EXT	External Capacitor to Ground (0.1μF)

I-TTL: INPUT, O-TTL: OUTPUT, I-PECL: PECL INPUT, O-PECL: PECL OUTPUT
EXT: EXTERNAL TERMINAL

Notes

Case Style KW



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