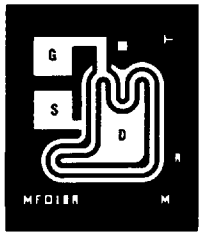
P-CHANNEL ENHANCEMENT MOS FET

CHIP NUMBER

FMP1.1



Die Size. 21 x 23 (mils)
0.533 x 0.584(mm)
Pad Size: 4 x 4 (mils)
BODY-SUBSTRATE

CONTACT METALLIZATION

Top Contact: > 12,000 Å Aluminum

Backside Contact: 3,000 Å Gold

ASSEMBLY RECOMMENDATIONS

It is advisable that:

a) the die be eutectically mounted with gold silicon preform 98/2%.

b) 1 mil (0.0254mm) aluminum wire be ultrasonically attached to the top contact.

TYPICAL ELECTRICAL CHARACTERISTICS

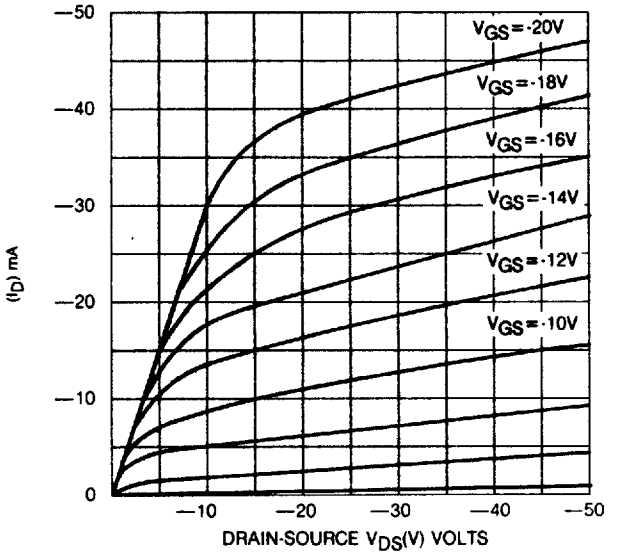
PARAMETER	MIN.	TYP	MAX.	UNIT	TEST CONDITIONS
BV_{GSS}	-35	-40	-60	V	I_D = 10, μA, V_{GS} = 0, V_{BS} = 0
I_{DSS}		20	500	pA	V_{DS} = -15V, V_{GS} = 0, V_{BS} = 0
g_{fs}	1000	2500	4000	μmho	V_{DS} = -15V, I_D, = 10mA, f = 1KHz
$I_{D(on)}$	-3.0		-30	mA	V_{DS} = -15V, V_{GS} = -10V, V_{GS} = 0
r_{DS}		200	350	Ω	V_{GS} = -20V, I_D = -100μA, V_{BS} = 0
$V_{GS(th)}$	-2.0		-5.0	V	V_{DS} = -15V, I_D = -10μA, V_{BS} = 0
C_{rss}			1.0	pF	V_{DS} = -15V, I_D = -10mA, f = 1MHz
C_{iss}			3.5	pF	V_{DS} = -15V, I_D = -10mA, f = 1MHz
$\bar{e}_n$		50		nV/√Hz	V_{DS} = -15V, I_D = -10mA, f = 1KHz

TYPICAL DEVICE TYPES: 2N4065, 3N163, 3N164, UC1700, UC1702

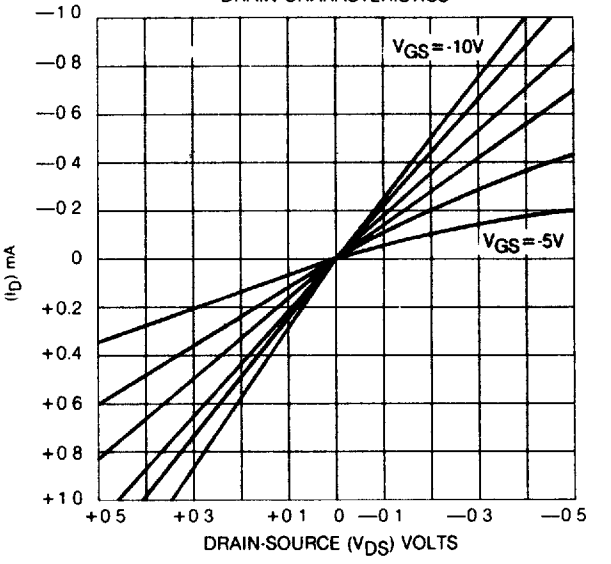
P-CHANNEL ENHANCEMENT MOS FET

CHIP TYPE FMP1.1

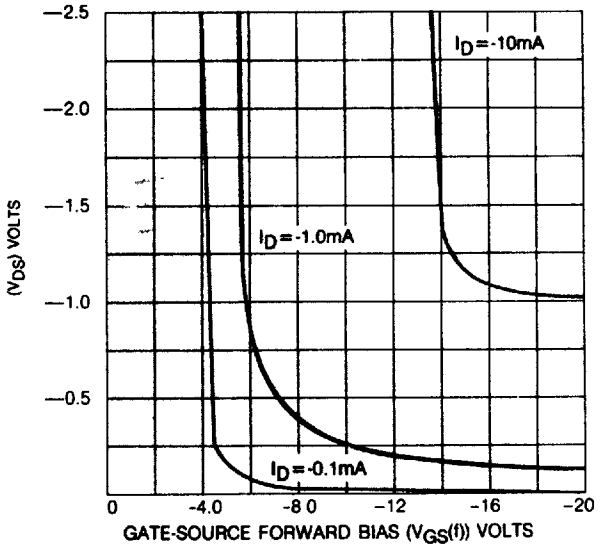
DRAIN CHARACTERISTICS—
COMMON-SOURCE



LOW LEVEL
DRAIN CHARACTERISTICS



LOW-LEVEL "ON" DRAIN SOURCE VOLTAGE
VS GATE-SOURCE FORWARD BIAS VOLTAGE



STATIC DRAIN-SOURCE ON RESISTANCE
VS GATE-SOURCE FORWARD BIAS