

CMOS Logic MN4000B Series
MN4000B/MN4000BS

6932852 PANASONIC INDL/ELECTRONIC

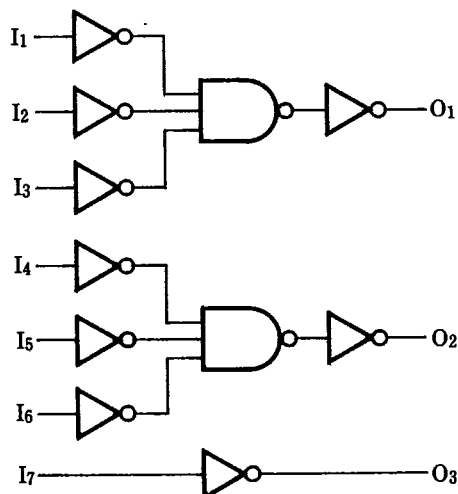
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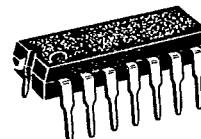
Dual 3-Input NOR Gates and Inverters

Description

The MN4000B/S are dual 3-input NOR gate and inverters. Their primary use is where low power dissipation and/or high noise immunity is desired.

Logic Diagram


P-1

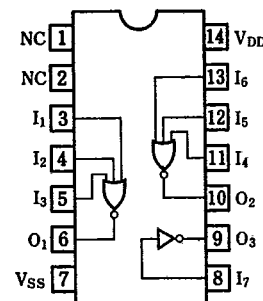


14-Pin • Plastic DIL Package

P-2



14-Pin • Panaflet Package (SO-14D)

Pin Configuration

Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.5 ~ +18	V
Input Voltage	V_I	-0.5 ~ $V_{DD} + 0.5^*$	V
Output Voltage	V_O	-0.5 ~ $V_{DD} + 0.5^*$	V
Peak Input • Output Current	$\pm I_I$	max. 10	mA
Power Dissipation (per package)	$T_a = -40 \sim +60^\circ\text{C}$	max. 400	mW
	$T_a = +60 \sim +85^\circ\text{C}$	Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)	P_D	max. 100	mW
Operating Ambient Temperature	T_{opr}	-40 ~ +85	°C
Storage Temperature	T_{stg}	-65 ~ +150	°C

* $V_{DD} + 0.5V$ should be under 18V

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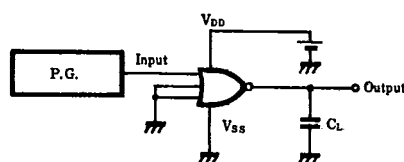
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■ DC Characteristics ($V_{SS}=0V$)

Item	V_{DD} (V)	Sym- bol	Conditions	$T_a=-40^\circ C$		$T_a=25^\circ C$		$T_a=85^\circ C$		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I_{DD}	$V_i=V_{SS}$ or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	$V_i=V_{SS}$ or V_{DD} $ I_o < 1\mu A$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_i=V_{SS}$ or V_{DD} $ I_o < 1\mu A$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$ I_o < 1\mu A$ $V_o=0.5V$ or $4.5V$ $V_o=1V$ or $9V$ $V_o=1.5V$ or $13.5V$	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$ I_o < 1\mu A$ $V_o=0.5V$ or $4.5V$ $V_o=1V$ or $9V$ $V_o=1.5V$ or $13.5V$	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	$V_o=0.4V$, $V_i=0V$ or $5V$	0.52	—	0.44	—	0.36	—	mA
	10		$V_o=0.5V$, $V_i=0V$ or $10V$	1.3	—	1.1	—	0.9	—	
	15		$V_o=1.5V$, $V_i=0V$ or $15V$	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_o=4.6V$, $V_i=0V$ or $5V$	0.52	—	0.44	—	0.36	—	mA
	10		$V_o=9.5V$, $V_i=0V$ or $10V$	1.3	—	1.1	—	0.9	—	
	15		$V_o=13.5V$, $V_i=0V$ or $15V$	3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	$V_o=2.5V$, $V_i=0V$ or $5V$	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_i$	$V_i=0V$ or $15V$	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics ($T_a=25^\circ C$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $I_1 \sim I_6 \rightarrow O_1, O_2$	5	t_{PHL}	—	70	210	ns
	10	t_{PLH}	—	35	105	
	15	t_{PLH}	—	30	90	
Propagation Delay Time $I_7 \rightarrow O_3$	5	t_{PHL}	—	45	135	ns
	10	t_{PLH}	—	25	75	
	15	t_{PLH}	—	20	60	
Input Capacitance		C_i	—	—	7.5	pF

1. Switching Time Test Circuit**2. Waveforms**