

Microtech
SEMICONDUCTORS

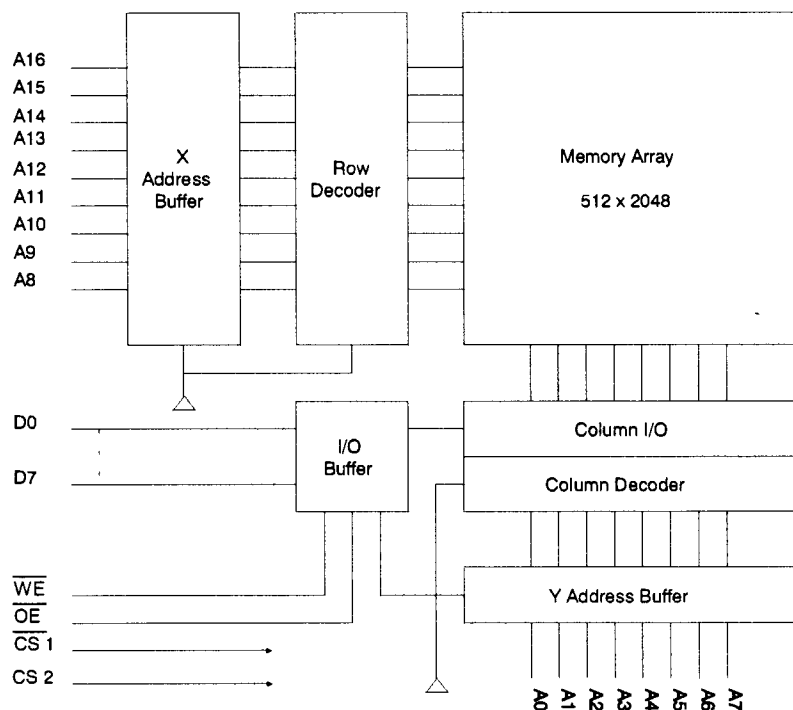
MS58128
- 35 / 45 / 55

1,048,576 bit High Speed CMOS Static RAM Module

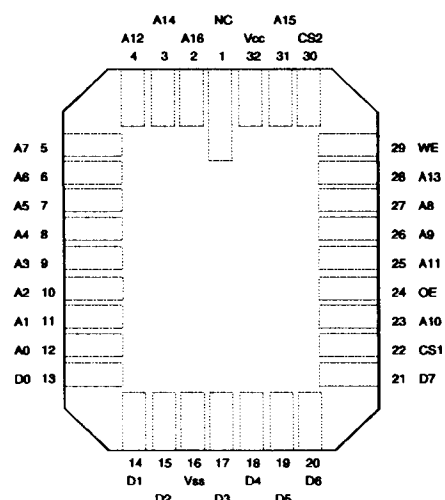
Features

- Full Military temperature range
- Very fast access times - 35/45/55ns
- Low power standby - 50 μ W (typical)
- Low power operation - 150mW (typical)
- Static operation - no clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible, all inputs and outputs

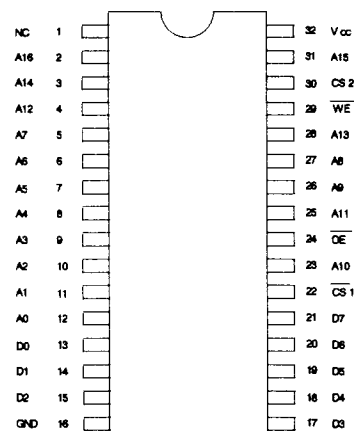
Block Diagram



Pin Assignments



32 pin LCC



32 pin DIL and 32 pin Flat-Pack

Pin Functions

A0-A16 Address inputs
D0-7 Data Input/Output
CS Chip Select
OE Output Enable
WE Write Enable
Vcc Power (+5V)
GND Ground

General Description

The MS58128 is a high speed 128K x 8 bit CMOS static RAM for use in high speed and low-power applications. The device operates from a single 5V supply, is fabricated using silicon-gate CMOS technology and is available in a variety of speeds and package styles.

Maximum ratings, absolute values ⁽¹⁾

		Min.	Max.	Unit
V _{CC}	Supply voltage ⁽²⁾	-0.5	+7.0	Volts
V _{IN}	Input voltage ⁽²⁾	-0.5	V _{CC} + 0.5	Volts
V _{IN/OUT}	Input/ Output voltage ⁽²⁾	-0.5	V _{CC} + 0.5	Volts
P _{tot}	Power dissipation		+1.0	Watts
T _{amb}	Operating temperature	-55	+125	°C
T _{stg}	Storage temperature	-65	+150	°C

Notes:

1. All voltage values are referenced to GND.
2. V_{CC}, V_{IN}, V_{IN/OUT} = - 3.5V minimum for pulse width ≤ 20ns.

Static Electrical Characteristics ⁽¹⁾

		Test Conditions	Min.	Max.	Units
V _{IL}	Low level, input voltage			0.8	Volts
V _{IH}	High level, input voltage		2.2		Volts
I _{IL}	Input leakage current	V _{IN} = GND to V _{CC}		2.0	μA
I _{LO}	Output leakage current	$\overline{\text{CS1}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$ or $\text{WE} = V_{IL}$ or $\text{CS2} = V_{IL}$ V _{I/O} = GND to V _{CC}		2.0	mA
I _{CC1}	Operating power supply current	$\overline{\text{CS1}} = V_{IL}$, $\text{CS2} = V_{IH}$ I _{I/O} = 0mA, V _{IN} = V _{IL} or V _{IH}		80	mA
I _{CC2}	Average operating supply current	Minimum cycle, duty = 100%, I _{I/O} = 0mA		120	mA
I _{SB1}	Standby power supply current	$\overline{\text{CS1}} \geq V_{CC} - 0.2V$ or $\text{CS2} \leq 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	2.0	mA	
I _{SB2}	Standby power supply current	$\overline{\text{CS1}} = V_{IH}$, $\text{CS2} = V_{IL}$ V _{IN} = V _{IL} or V _{IH}		15	mA
V _{OL}	Low level output voltage	I _{OL} = 8.0mA		0.4	Volts
V _{OH}	High level output voltage	-I _{OH} = 4.0mA	2.4		Volts

Note:

1. All limits over specified temperature and voltage range (unless otherwise stated)

Operating Conditions ⁽¹⁾

		Min.	Max.	Units
V _{CC}	Supply voltage	4.5	5.5	Volts
V _{IL}	Low-level input voltage ⁽²⁾	-0.3	0.8	Volts
V _{IH}	High-level input voltage	2.2	V _{CC} + 0.3	Volts
t _{AA}	Address access time (option -35)		35	nS
t _{AA}	Address access time (option -45)		45	nS
t _{AA}	Address access time (option -55)		55	nS
T _{amb}	Operating temperature ambient	-55	+125	°C

Notes:

1. The above are recommended conditions of use and the given values apply over the full operating temperature range. All voltages are referenced to the GND terminal.
2. V_{IL} = -3.0V minimum for pulse width ≤ 20nS.

Read Cycle ⁽¹⁾

		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	
t _{RC}	Read cycle time	35		45		55		nS
t _{AA}	Address access time		35		45		55	nS
t _{ACS}	Chip select access time		35		45		55	nS
t _{OE}	Output enable to output valid		20		25		30	nS
t _{OH}	Output hold from address change	5		5		5		nS
t _{CLZ}	Chip select to output low Z	5		5		5		nS
t _{OLZ}	Output select to output low Z	0		0		0		nS
t _{CHZ}	Chip deselection to output high Z	0	15	0	20	0	25	nS
t _{PU}	Chip enable to power up time	0		0		0		nS
t _{SPD}	Chip enable to power down time	35		45		55		nS

Note:

1. All limits over specified temperature and voltage range (unless otherwise stated).

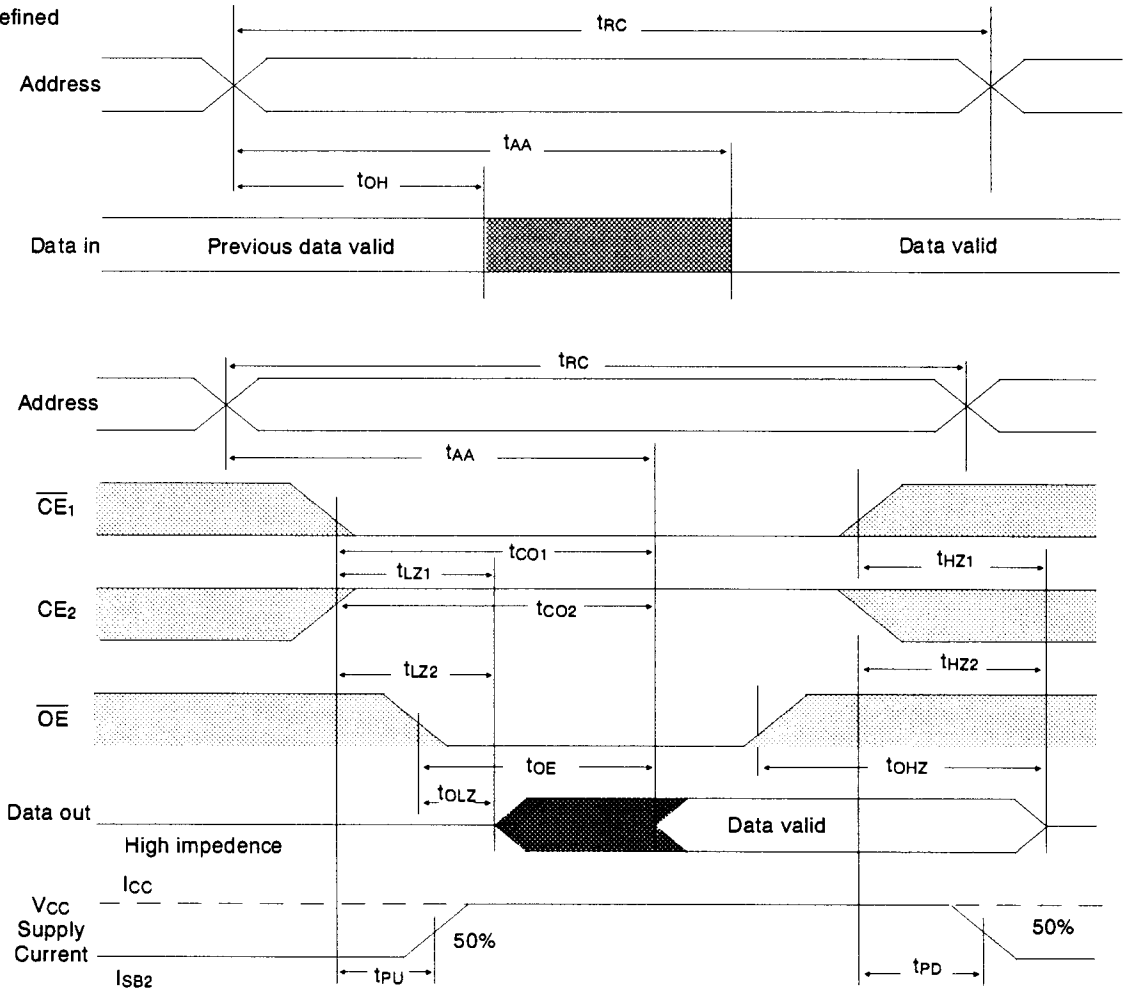
Key



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Write Cycle ⁽¹⁾

		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	
t _{WC}	Write cycle time	35		45		55		nS
t _{AW}	Address valid to end of write	30		40		45		nS
t _{CW}	Chip enable to end of write	30		40		45		nS
t _{DW}	Data to write time overlap	18		20		25		nS
t _{DH}	Data hold from write time	0		0		0		nS
t _{WP}	Write pulse width	30		35		40		nS
t _{AS}	Address set up time	0		0		0		nS
t _{WR1}	Write recovery time from $\overline{WE}$ or $\overline{CS1}$	3		3		3		nS
t _{WR2}	Write recovery time ($\overline{CS2}$)	5		5		5		nS
t _{OW}	Output active from end of write	5		5		5		nS
t _{WHZ}	Write to output in high Z	0	15	0	15	0	15	nS

Note:

1. All limits over specified temperature and voltage range (unless otherwise stated)

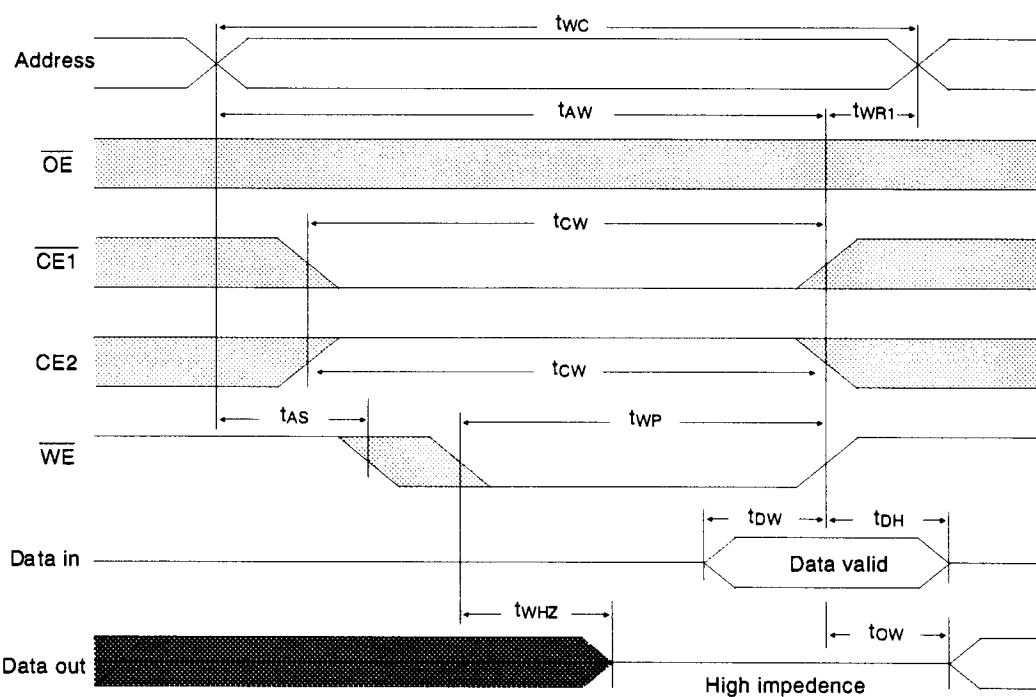
Key

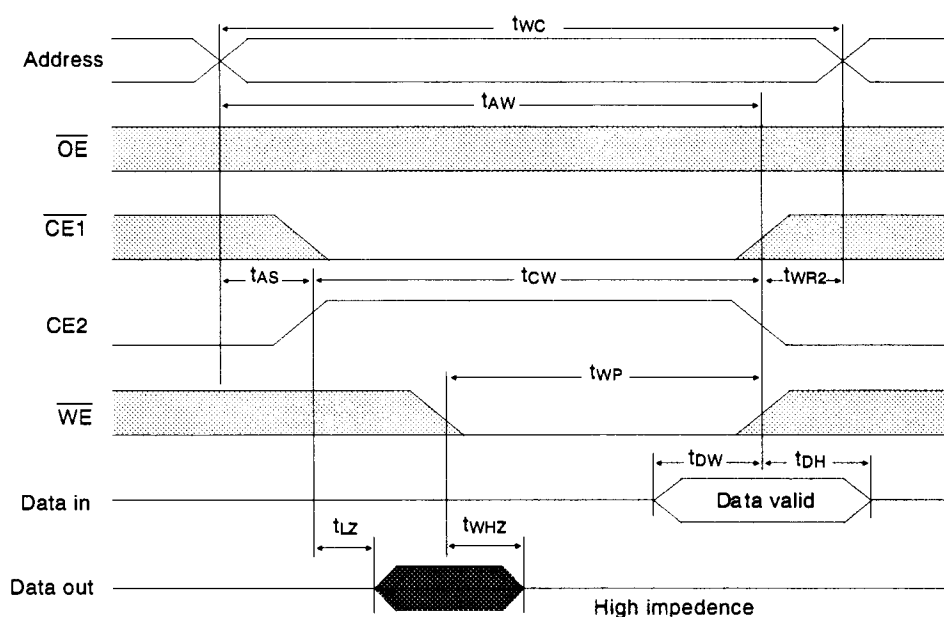
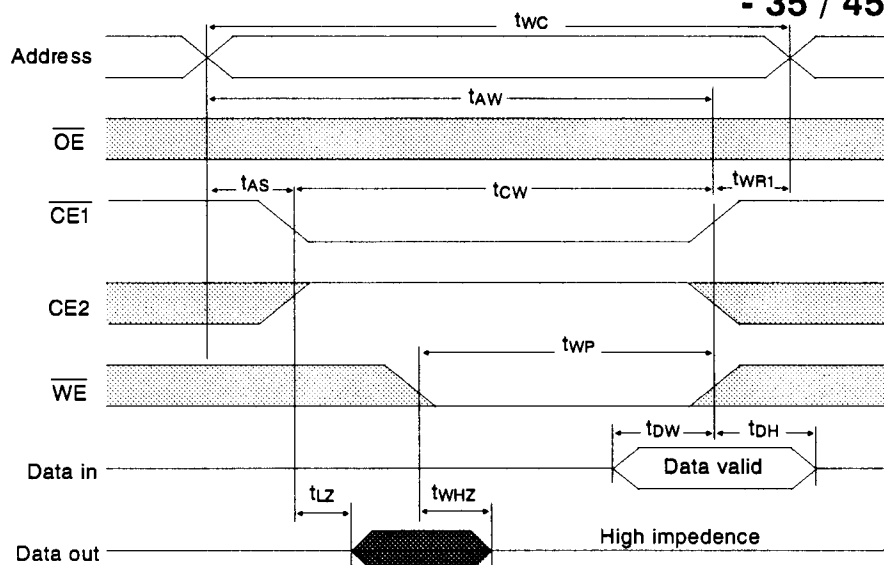


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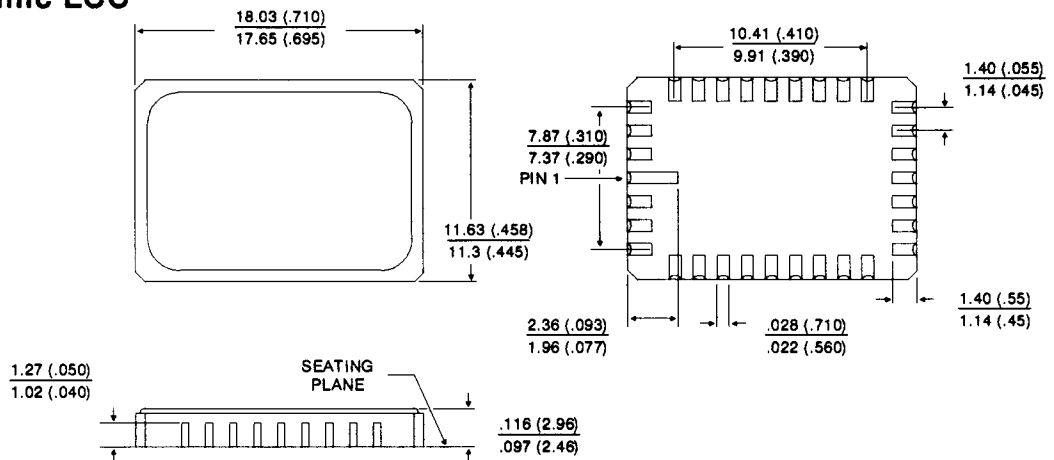
Truth table

Mode	$\overline{OE}$	$\overline{CS1}$	$CS2$	$\overline{WE}$	Outputs	Vcc Current
Not Selected	X	H	X	X	High Z	I_{SB1} , I_{SB2}
Not Selected	X	X	L	X	High Z	I_{SB1} , I_{SB2}
Output Disabled	H	L	H	H	High Z	I_{CC1} , I_{CC2}
Read	L	L	H	H	DOUT	I_{CC1} , I_{CC2}
Write	X	L	H	L	DIN	I_{CC1} , I_{CC2}
Note: H = High, L = Low, X = H or L						

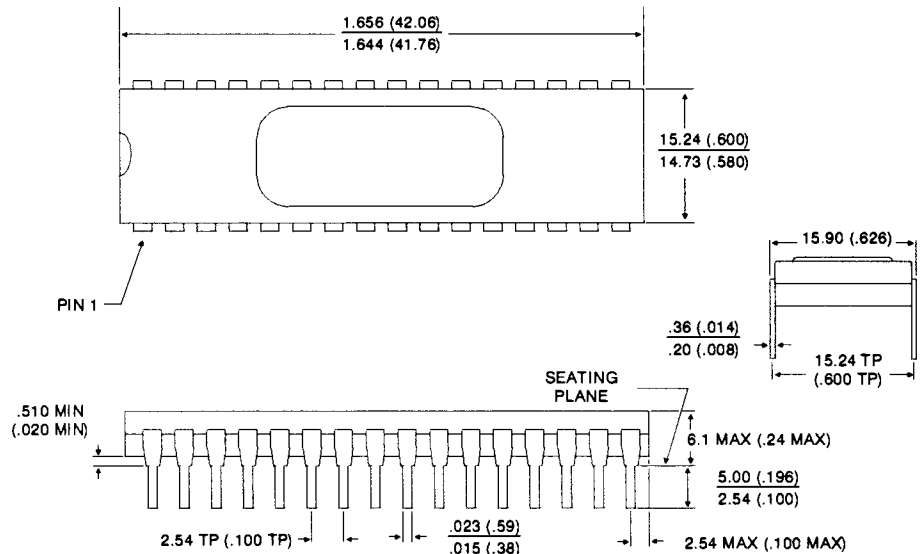
I/O Capacitance

	Min.	Max.	Units
C_{IN} Input capacitance @ $T_{amb} = 25^{\circ}C$, $f = 1MHz$		7	pF
$C_{I/O}$ I/O capacitance		7	pF

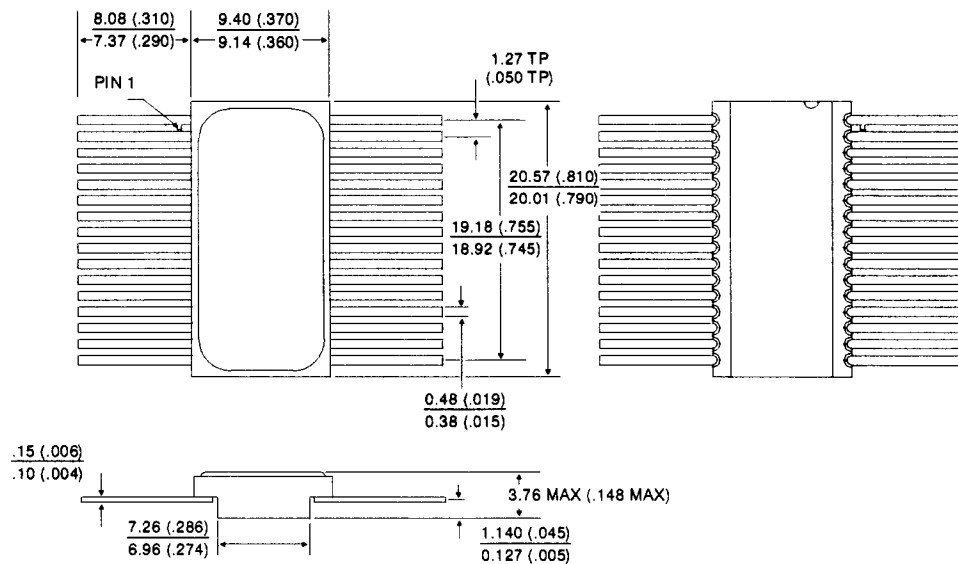
32-Lead Ceramic LCC



32-Lead 600mil Sidebrazed DIL



32-Lead Flat Pack





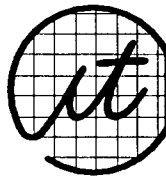
55

Speed : - 35ns
- 45ns
- 55ns

Package Style :
J = 32 pin ceramic DIL
W = 32 pin ceramic LCC
F = 32 pin ceramic Flat-Pack

128K X 8

CMOS Ultra Fast Static RAM



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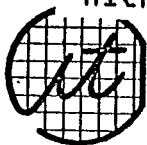
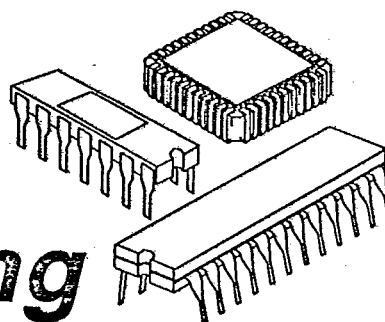
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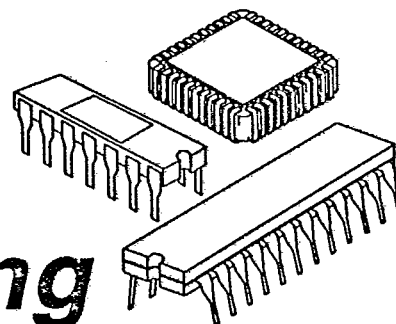
Microtech Semiconductors are leaders in Custom assembly, with our considerable expertise in production and test, we can satisfy the most complex requirement.

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**MICROTECH**

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Custom Packaging

Approved to CECC and BS9000, hallmarks of European quality, MICROTECH Semiconductors is totally committed to total quality. Dedicated to supporting the high-reliability equipment manufacturer, our integrated circuits are produced in Class 1000 cleanroom conditions. Final optical inspection takes place under better than Class 100 laminar flow and our impressive range of environmental and electrical test equipment ensures that we release high performance components with no compromise on reliability.

CUSTOM PACKAGING