DRAM MODULE

1, 2, 4 MEG x 32

4, 8, 16 MEGABYTE, 5V, BURST EDO

NEW DRAM SIMM

FEATURES

- 72-pin, single-in-line memory module (SIMM)
- Burst order, interleave or linear, programmed by executing WCBR cycle after initialization
- High-performance CMOS silicon-gate process
- Single +5V ±5% power supply
- All inputs and outputs are TTL-compatible
- Refresh modes: $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) or $\overline{\text{RAS}}$ ONLY
- 1,024-cycle refresh (10 row-, 10 column-addresses) [MT2D(T)132 B]
  2,048-cycle refresh (11 row-, 10 column-addresses) (MT4D232 B)
  2,048-cycle refresh (11 row-, 11 column-addresses) (MT8D432 B)
- Four-cycle Extended Data-Out (EDO) burst accesses

OPTIONS — MARKING

- Timing
  52ns access; 15ns cycle — -52
  60ns access; 16.6ns cycle — -60
- Components
  SOJ — D
  TSOP (1 Meg x 32 only) — DT
- Packages
  72-pin SIMM — M
  72-pin SIMM (gold) — G

KEY TIMING PARAMETERS

SPEED	^tRAC	^tPC	^tCAC	^tCOH	^tDS	^tDH
-52	52ns	15ns	10ns	3ns	0ns	5ns
-60	60ns	16.6ns	11ns	3ns	0ns	5ns

PART NUMBERS

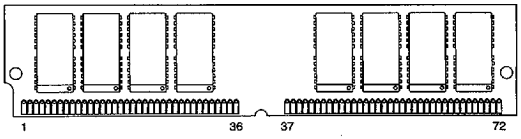
PART NUMBER	DESCRIPTION
MT2D132G-xx B	1 Meg x 32 Burst EDO, Gold, SOJ
MT2DT132G-xx B	1 Meg x 32 Burst EDO, Gold, TSOP
MT4D232G-xx B	2 Meg x 32 Burst EDO, Gold, SOJ
MT8D432G-xx B	4 Meg x 32 Burst EDO, Gold, SOJ
MT2D132M-xx B	1 Meg x 32 Burst EDO, Tin/Lead, SOJ
MT2DT132M-xx B	1 Meg x 32 Burst EDO, Tin/Lead, TSOP
MT4D232M-xx B	2 Meg x 32 Burst EDO, Tin/Lead, SOJ
MT8D432M-xx B	4 Meg x 32 Burst EDO, Tin/Lead, SOJ

xx = speed

PIN ASSIGNMENT (Front View)

72-Pin SIMM

(DD-11) 1 Meg x 32 TSOP version
(DD-9) 1 Meg x 32 SOJ version
(DD-8) 2 Meg x 32
(DD-3) 4 Meg x 32 (shown)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{\text{CAS0}}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{\text{CAS2}}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{\text{CAS3}}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{\text{RAS0}}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

GENERAL DESCRIPTION

The MT2D(T)132 B, MT4D232 B and MT8D432 B are randomly accessed 4MB, 8MB and 16MB solid-state memories organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20/21/22 address bits, which are entered 10/11 bits (A0-A10) at $\overline{\text{RAS}}$ time and 10/11 bits (A0-A10) at $\overline{\text{CAS}}$ time.

These SIMMs are burst access DRAM modules in which all READ and WRITE cycles occur in bursts of four. The bursts wrap around on a 4-half-byte boundary. This means only the two least significant bits of the $\overline{\text{CAS}}$ address are modified internally to produce each address of the burst sequence. The burst type, interleave or linear, is determined by executing a WCBR cycle (CBR cycle with $\overline{\text{WE}}$ LOW), with address A0 set to either HIGH or LOW. A0 LOW will

GENERAL DESCRIPTION (continued)

program the module to execute linear bursts, A0 HIGH will program the bursts to be interleave. For future compatability it is strongly recommended that the information (0010 000x) where x=A0 is supplied on addresses A7-A0 during the WCBR cycle. The WCBR cycle must be followed by a $\overline{RAS}$-ONLY or CBR REFRESH cycle to exit this programming mode.

A READ or WRITE cycle is selected with the $\overline{WE}$ input during the first $\overline{CAS}$ LOW pulse of the burst. During the burst cycle the $\overline{WE}$ input must remain constant for the burst to continue. Transition of the $\overline{WE}$ input during a burst causes the burst to terminate and place the outputs in a High-Z state. After a terminated burst, the next falling edge of $\overline{CAS}$ will start a new burst access at the address present on the external address bus.

During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must be LOW prior to $\overline{CAS}$ going LOW. This places the input/output pins in the High-Z state allowing the data-in (D) to be driven on the bus. $\overline{WE}$ must remain LOW during the burst operation for it to complete. $\overline{WE}$ going HIGH after ^{t}WCH from $\overline{CAS}$ LOW and before ^{t}WCS of the next $\overline{CAS}$ LOW terminates the burst operation and places the DQ pins in the High-Z state.

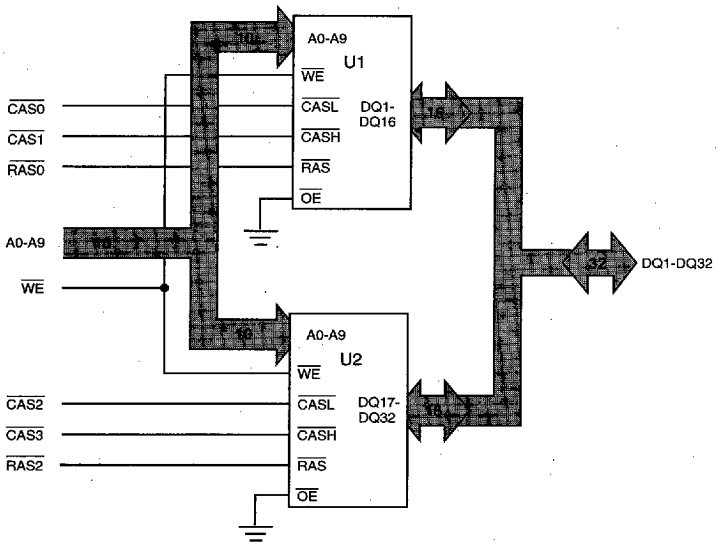
During a READ cycle $\overline{WE}$ must be HIGH prior to $\overline{CAS}$ going LOW. $\overline{WE}$ must remain HIGH during the burst operation for the burst to complete. $\overline{WE}$ going LOW after ^{t}RCH from $\overline{CAS}$ LOW and before ^{t}RCS of the next $\overline{CAS}$ LOW terminates the burst operation and places the DQ pins in the High-Z state.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates burst operations in the selected row, resets the burst counter, closes that row and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next access during the $\overline{RAS}$ HIGH time.

WORD AND BYTE WRITEs

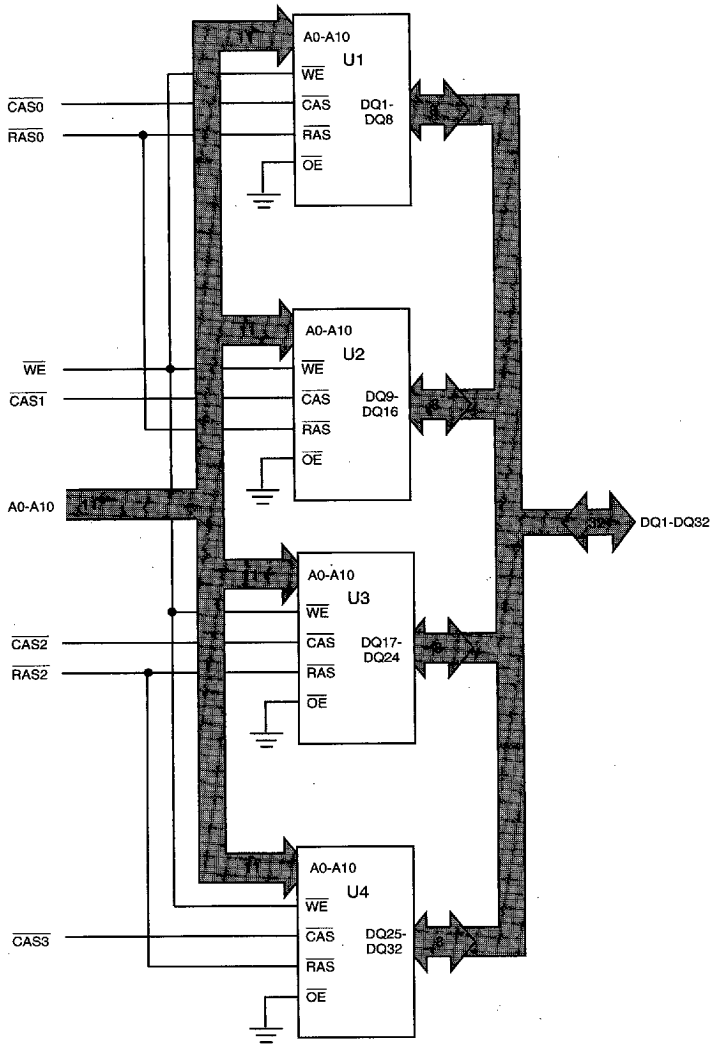
WORD WRITEs on the x16 Burst EDO DRAM based module [MT2D(T)132] require $\overline{CAS0}$ with $\overline{CAS1}$ and $\overline{CAS2}$ with $\overline{CAS3}$ skew considerations that are not required on modules employing x4 and x8 Burst EDO DRAMs. BYTE WRITEs on the x16 based MT2D(T)132 require special considerations when bursts are attempted. Refer to the MT4LC1M16H5 1 Meg x 16 Burst EDO DRAM data sheet for information on $\overline{CAS}$ to $\overline{CAS}$ skew requirements during WORD WRITE cycles and bursting BYTE WRITEs.

FUNCTIONAL BLOCK DIAGRAM
MT2(T)D132 B (4MB)



BURST EDO
U1-U2 = 1 Meg x 16 Burst EDO DRAMs

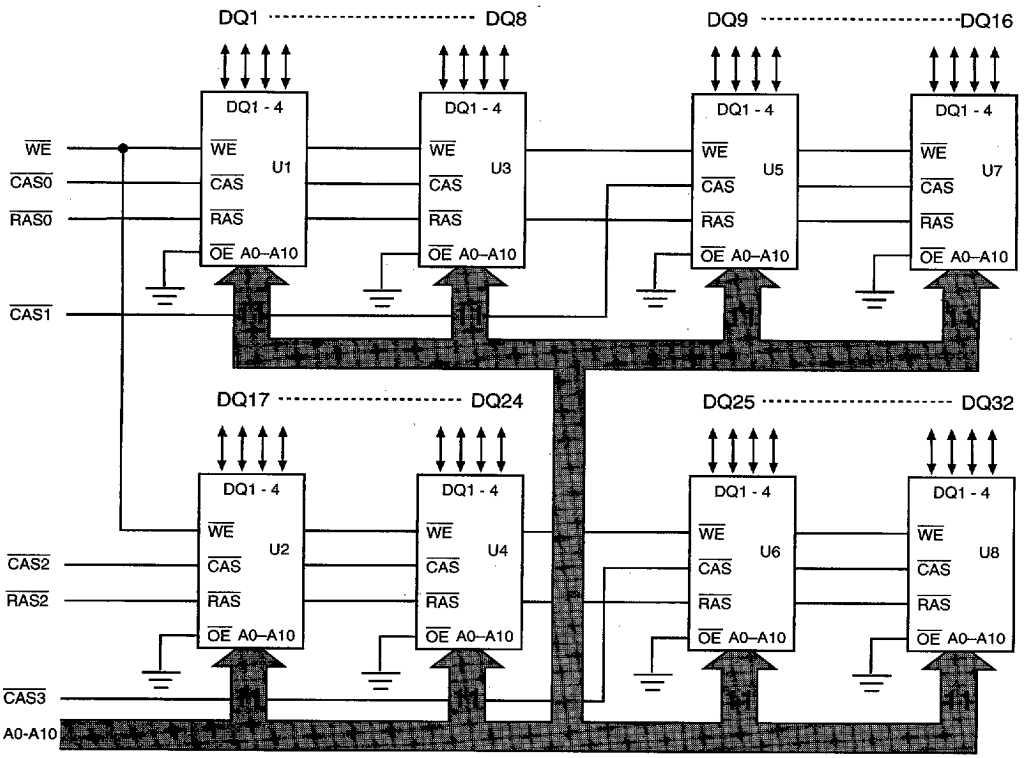
FUNCTIONAL BLOCK DIAGRAM
MT4D232 B (8MB)



BURST EDO
U1-U4 =2 Meg x 8 Burst EDO DRAMs

NEW DRAM SIMM

FUNCTIONAL BLOCK DIAGRAM
MT8D432 B (16MB)



BURST EDO
U1-U8 = 4 Meg x 4 Burst EDO DRAMs

EDO BURST MODE TRUTH TABLE

PRESENT STATE	RESULTING STATE	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA
						Row	Column	DQ1-32
Any	Idle	L→H	H	X	X	X	X	High-Z
Idle	Row Open	H→L	H	X	X	ROW	X	High-Z
Idle	CBR REFRESH	H→L	L	H	X	X	X	High-Z
Row Open	$\overline{RAS}$-ONLY REFRESH	L	H	X	X	ROW	X	High-Z
Row Open	READ burst	L	H→L	H	L	X	COL	Data-Out
Row Open	WRITE burst	L	H→L	L	X	X	COL	Data-In
READ burst	TERMINATE READ burst	L	H	H→L	X	X	X	High-Z
WRITE burst	TERMINATE WRITE burst	L	H	L→H	X	X	X	High-Z
Idle	PROGRAM burst type	H→L	L	L	X	A0[1]	X	High-Z
PROGRAM	EXIT PROGRAM MODE using CBR REFRESH	H→L	L	H	X	X	X	High-Z
PROGRAM	EXIT PROGRAM MODE using $\overline{RAS}$-ONLY REFRESH	L	H	X	X	ROW	X	High-Z

NOTE: 1. A WCBR cycle determines the burst sequence. A0=LOW sets the burst sequence to linear, A0=HIGH set the burst sequence to interleave. A8 through A10 are "don't cares." A7-A0 should contain the sequence (0010 000x where x=A0) to ensure future compatability. A refresh cycle ($\overline{RAS}$ ONLY or CBR) must follow the WCBR cycle to exit the programming mode.

NEW DRAM SIMM

INTERLEAVE BURST SEQUENCE TABLE

	ADDRESSES USED		
OPERATION	**A10 - A2**	**A1**	**A0**
First access, register external CAS address	A10 - A2	A1	A0
Second access, (first burst address)	registered A10 - A2	registered A1	registered $\overline{A0}$
Third access (second burst address)	registered A10 - A2	registered $\overline{A1}$	registered A0
Fourth access (third burst address)	registered A10 - A2	registered $\overline{A1}$	registered $\overline{A0}$

INTERLEAVE BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X00	X..X11	X..X10
X..X10	X..X11	X..X00	X..X01
X..X11	X..X10	X..X01	X..X00

LINEAR BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X10	X..X11	X..X00
X..X10	X..X11	X..X00	X..X01
X..X11	X..X00	X..X01	X..X10

CAPACITANCE

PARAMETER	SYMBOL	MAX 4MB	MAX 8MB	MAX 16MB	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	16	26	46	pF	3
Input Capacitance: $\overline{WE}$	C_{I2}	16	26	46	pF	3
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}	10	16	28	pF	3
Input Capacitance: $\overline{CAS0}$ - $\overline{CAS3}$	C_{I4}	8	8	12	pF	3
Input/Output Capacitance: DQ1-DQ32	C_{IO}	10	10	10	pF	3

NEW DRAM SIMM

PRESENCE-DETECT - MT2(T)D132 B (4MB)

SYMBOL	PIN #	-52	-60
PRD1	67	Vss	Vss
PRD2	68	Vss	Vss
PRD3	69	Vss	NC
PRD4	70	Vss	NC

PRESENCE-DETECT - MT4D232 B (8MB)

SYMBOL	PIN #	-52	-60
PRD1	67	NC	NC
PRD2	68	NC	NC
PRD3	69	Vss	NC
PRD4	70	Vss	NC

PRESENCE-DETECT - MT8D432 B (16MB)

SYMBOL	PIN #	-52	-60
PRD1	67	Vss	Vss
PRD2	68	NC	NC
PRD3	69	Vss	NC
PRD4	70	Vss	NC

NEW DRAM SIMM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss ..... -1V to +7V
Voltage on Inputs, NC or I/O pins
Relative to Vss ..... -1V to +5.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 4.8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1) (Vcc = +5V ±5%)

PARAMETER/CONDITION		SYM	SIZE	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	ALL	4.75	5.25	V	
Input High (Logic 1) Voltage, all inputs		VIH	ALL	2.4	5.25	V	2
Input Low (Logic 0) Voltage, all inputs		VIL	ALL	-1.0	0.8	V	2
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V)	$\overline{CAS0}$-$\overline{CAS3}$	II1	4MB 8MB 16MB	-2 -2 -4	2 2 4	µA µA µA	
	A0-A10, $\overline{WE}$, $\overline{RAS0}$, $\overline{RAS2}$	II2	4MB 8MB 16MB	-4 -8 -16	4 8 16	µA µA µA	18
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ32	IOZ	ALL	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	ALL	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL	ALL		0.4	V	

PARAMETER/CONDITION	SYM	SIZE	MAX -52	MAX -60	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	4MB 8MB 16MB	14 18 26	14 18 26	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	4MB 8MB 16MB	11 12 14	11 12 14	mA	
OPERATING CURRENT: Closed Row Burst READ/WRITE Average power supply current; (^tPC = ^tPC [MIN]; 50% duty cycle on $\overline{RAS}$; open row, four-cycle burst, close row)	ICC3	4MB 8MB 16MB	320 440 880	300 400 800	mA	4, 5
OPERATING CURRENT: Open Row Burst READ/WRITE Average power supply current (alternating four-cycle burst followed by four cycles of inactivity; ^tPC = ^tPC [MIN])	ICC4	4MB 8MB 16MB	180 280 520	170 260 480	mA	4, 5
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current (address cycling; $\overline{RAS}$ cycling $\overline{CAS}$ = VIH; ^tRAS = ^tRAS [MIN]; ^tRP = ^tRP [MIN])	ICC5	4MB 8MB 16MB	380 560 1,040	320 520 960	mA	4, 5
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling: ^tRAS = ^tRAS [MIN]; ^tRP = ^tRP [MIN])	ICC6	4MB 8MB 16MB	340 560 1,040	300 520 960	mA	5, 6

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 13) (Vcc = +5V ±5%)

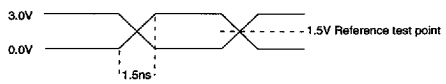
AC CHARACTERISTICS		-52		-60			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from $\overline{CAS}$	^tAA		25		28.2	ns	11
Column-address setup time	^tASC	1.5		1.5		ns	
Row-address setup time	^tASR	1.5		1.5		ns	
Burst terminate hold time	^tBTH	3		3		ns	
Output disable from burst terminate	^tBTHZ	7	13	7	13	ns	14
Access time from $\overline{CAS}$	^tCAC		10		11	ns	
Column-address hold time	^tCAH	8.5		8.5		ns	
$\overline{CAS}$ pulse width	^tCAS	5	10,000	5	10,000	ns	
$\overline{CAS0}$ and $\overline{CAS1}$ or $\overline{CAS2}$ and $\overline{CAS3}$ Coincident HIGH time	^tCCH	5		5		ns	15
$\overline{CAS}$ hold time (CBR or WCBR)	^tCHR	15		15		ns	6
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	
Data Hold time from $\overline{CAS}$ LOW	^tCOH	3		3		ns	
$\overline{CAS}$ precharge time	^tCP	5		5		ns	
$\overline{CAS}$ precharge time (CBR or WCBR)	^tCPN	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH (WRITE only)	^tCRW	15		16.6		ns	
Skew between $\overline{CAS0}$ and $\overline{CAS1}$ or $\overline{CAS2}$ and $\overline{CAS3}$ (WRITE only)	^tCSK		2		2	ns	16
$\overline{CAS}$ setup time (CBR or WCBR)	^tCSR	10		10		ns	6
Data-in hold time	^tDH	5		5		ns	
Data-in setup time	^tDS	0		0		ns	17
Output buffer turn-off delay	^tOFF	4	13	4	13	ns	
Burst EDO cycle time	^tPC	15		16.6		ns	
Access time from $\overline{RAS}$	^tRAC		52		60	ns	
Row-address hold time	^tRAH	8.5		8.5		ns	
$\overline{RAS}$ pulse width	^tRAS	52	125,000	60	125,000	ns	
Random Read or Write cycle time	^tRC	90				ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$^tRCD1$	20		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$^tRCD2$	40		45		ns	
Read command hold time	^tRCH	5		5		ns	
Read command setup time	^tRCS	3		4		ns	
Refresh period (1,024 cycles)	^tREF		16		16	ms	
Refresh period (2,048 cycles)	^tREF		32		32	ms	
$\overline{RAS}$ precharge time	^tRP	30		40		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	5		5		ns	
$\overline{RAS}$ hold time	^tRSH	0		0		ns	
Transition time (rise or fall)	^tT	1.5	50	1.5	50	ns	
Burst Terminate pulse width	^tTP	6		6		ns	12
Write command hold time	^tWCH	5		5		ns	
$\overline{WE}$ command setup time	^tWCS	3		4		ns	
Ouput Disable from $\overline{WE}$ LOW	^tWHZ	4	10	4	10	ns	14
$\overline{WE}$ hold time (CBR or WCBR)	^tWRH	10		10		ns	
$\overline{WE}$ setup time (CBR or WCBR)	^tWRP	10		10		ns	

NEW DRAM SIMM

NEW

DRAM SIMM

Input timing waveform:



Output timing waveform:

Figure 1
TIMING SPECIFICATIONS

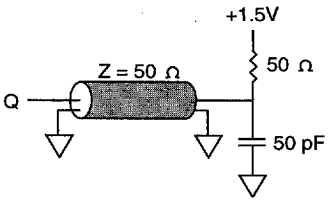
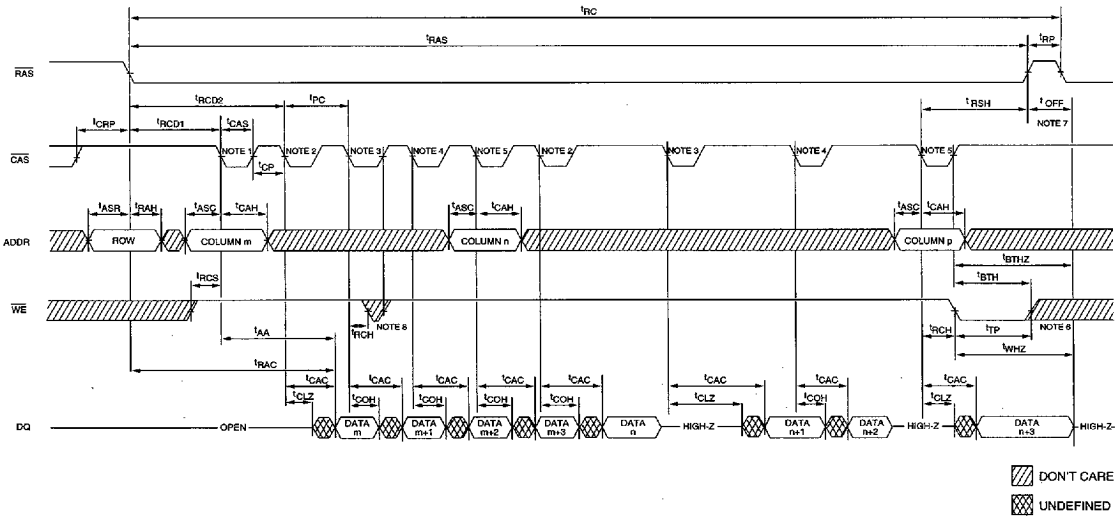


Figure 2
AC TIMING OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to V_{SS}.
2. Input Power-up: $V_{IH} \leq +5.5V$ and $V_{CC} \leq +5.5V$ for $t \leq 200ms$
3. This parameter is sampled. $V_{CC} = 5V \pm 5\%$; $f = 1$ MHz.
4. Address transitions once per burst access.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum ^tPC and 50 percent duty cycle. The outputs are open.
6. Enables on-chip refresh and address counters.
7. Initialization consists of an initial pause of 100µs after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH). This sequence must be executed before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded. A WCBR cycle must be executed to initalize the burst type, interleave or linear followed by a $\overline{RAS}$ ONLY or CBR REFRESH cycle.
8. AC characteristics assume $^tT = 1.5ns$.
9. All output timings are referenced to 1.5V and all input timings are referenced to 1.5V, unless otherwise specified. Inputs must be driven to the appropriate voltage levels indicated by the corresponding timing diagrams when AC specifications are measured, as shown in Figure 1.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. ^tAA is a calculated specification which is the sum of ^tPC and ^tCAC.
12. Applies only during burst termination operation.
13. AC output loading is specified with $C_L = 50pF$ as in Figure 2. Transition is measured at the 1.5V reference level.
14. The DQs will continue to drive data out until both ^tBTHZ (MIN) and ^tWHZ (MIN) have been satisfied and will reach the High-Z state once ^tBTHZ (MAX) and ^tWHZ (MAX) have both been satisfied.
15. $\overline{CAS0}$ and $\overline{CAS1}$ or $\overline{CAS2}$ and $\overline{CAS3}$, etc. HIGH pulse widths must be concurrently HIGH for at least this limit [MT2D(T)132 B version only].
16. The skew between $\overline{CAS0}$ and $\overline{CAS1}$ or $\overline{CAS2}$ and $\overline{CAS3}$ is required for WRITE cycles and is required only on the MT2D(T)132 B SIMM since it utilizes 1 Meg x 16 Burst EDO DRAMs.
17. Valid data-in is referenced from when a valid logic level (V_{IH}, V_{IL}) is achieved.
18. $\overline{RAS0}$ and $\overline{RAS2}$ will be half of the values shown.

BURST EDO READ CYCLE



NOTE:

1. Latch column address; start READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start READ cycle.
6. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until $^{t}BTHZ$ (MIN) and ^{t}WHZ (MIN) have both been satisfied and will reach the High-Z state once $^{t}BTHZ$ (MAX) and ^{t}WHZ (MAX) have both been satisfied.
7. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQs in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{RAS}$ or $\overline{CAS}$) that transitions HIGH.
8. $\overline{WE}$ transitioning LOW and returning HIGH prior to $\overline{CAS}$ going HIGH will not terminate the burst.

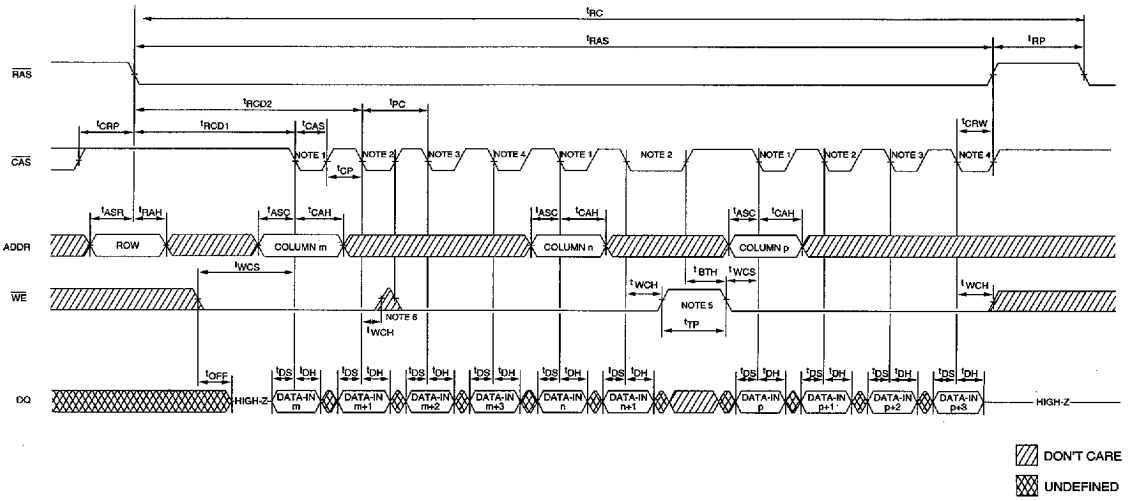
TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}AA		25		28.2	ns
^{t}ASC	1.5		1.5		ns
^{t}ASR	1.5		1.5		ns
^{t}BTH	3		3		ns
$^{t}BTHZ$	7	13	7	13	ns
^{t}CAC		10		11	ns
^{t}CAH	8.5		8.5		ns
^{t}CAS	5	10,000	5	10,000	ns
^{t}CLZ	3		3		ns
^{t}COH	3		3		ns
^{t}CP	5		5		ns
^{t}CRP	10		10		ns
^{t}OFF	4	10	4	10	ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}PC	15		16.6		ns
^{t}RAC		52		60	ns
^{t}RAH	8.5		8.5		ns
^{t}RAS	52	125,000	60	125,000	ns
^{t}RC	90		110		ns
$^{t}RCD1$	20		20		ns
$^{t}RCD2$	40		45		ns
^{t}RCH	5		5		ns
^{t}RCS	3		4		ns
^{t}RP	30		40		ns
^{t}RSH	0		0		ns
^{t}TP	6		6		ns
^{t}WHZ	4	10	4	10	ns

NEW DRAM SIMM

BURST EDO WRITE CYCLE



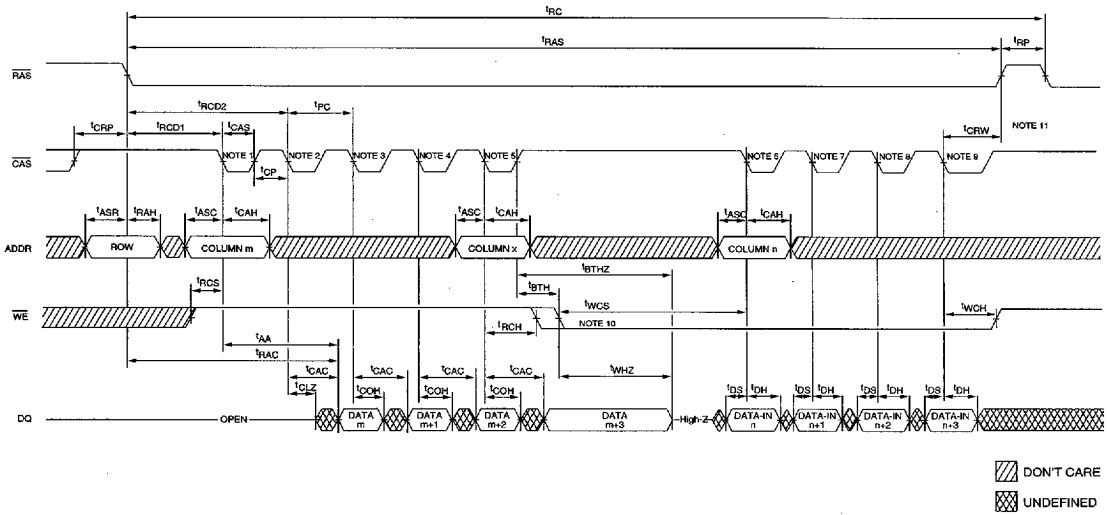
NOTE:
1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. $\overline{WE}$ transitioning HIGH will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied.
6. $\overline{WE}$ transitioning HIGH and returning LOW prior to $\overline{CAS}$ going HIGH will not terminate the burst.

TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}ASC	1.5		1.5		ns
^{t}ASR	1.5		1.5		ns
^{t}BTH	3		3		ns
^{t}CAH	8.5		8.5		ns
^{t}CAS	5	10,000	5	10,000	ns
^{t}CP	5		5		ns
^{t}CRP	10		10		ns
^{t}CRW	15		16.6		ns
^{t}DH	5		5		ns
^{t}DS	0		0		ns
^{t}OFF	4	13	4	13	ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}PC	15		16.6		ns
^{t}RAH	8.5		8.5		ns
^{t}RAS	52	125,000	60	125,000	ns
^{t}RC	90		110		ns
$^{t}RCD1$	20		20		ns
$^{t}RCD2$	40		45		ns
^{t}RP	30		40		ns
^{t}TP	6		6		ns
^{t}WCH	5		5		ns
^{t}WCS	3		4		ns

BURST EDO READ/WRITE CYCLE



NOTE:

1. Latch column address; start burst READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start burst READ cycle.
6. Latch column address; start burst WRITE cycle; write data 1.
7. Increment burst counter; write data 2.
8. Increment burst counter; write data 3.
9. Increment burst counter; write data 4.
10. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. ^{t}TP is met by the READ burst being terminated by a WRITE burst. The DQs will continue to drive data out until $^{t}BTHZ$ (MIN) and ^{t}WHZ (MIN) have both been satisfied and will reach the High-Z state once $^{t}BTHZ$ (MAX) and ^{t}WHZ (MAX) have both been satisfied.
11. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQ pins in the High-Z state.

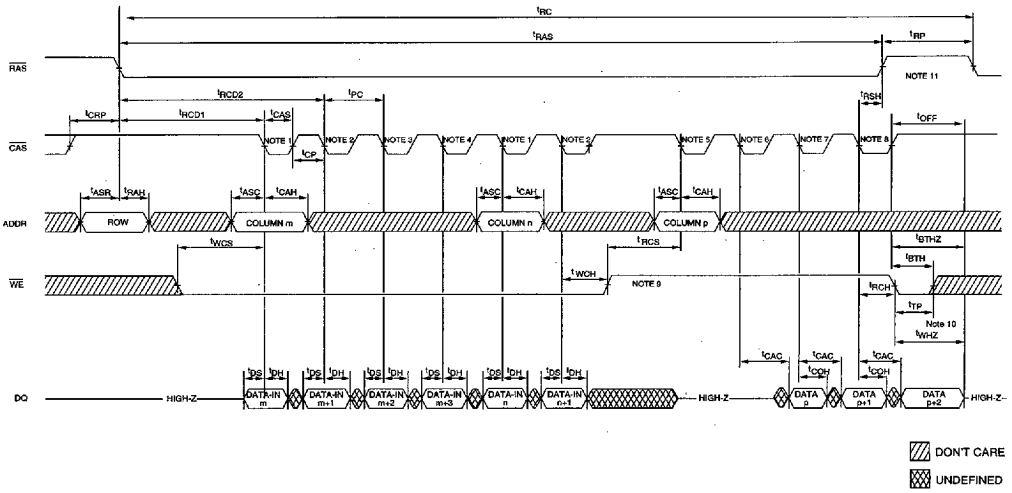
TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}AA		25		28.2	ns
^{t}ASC	1.5		1.5		ns
^{t}ASR	1.5		1.5		ns
^{t}BTH	3		3		ns
$^{t}BTHZ$	7	13	7	13	ns
^{t}CAC		10		11	ns
^{t}CAH	8.5		8.5		ns
^{t}CAS	5	10,000	5	10,000	ns
^{t}CLZ	3		3		ns
^{t}COH	3		3		ns
^{t}CP	5		5		ns
^{t}CRP	10		10		ns
^{t}CRW	15		16.6		ns
^{t}DH	5		5		ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}DS	0		0		ns
^{t}PC	15		16.6		ns
^{t}RAC		52		60	ns
^{t}RAH	8.5		8.5		ns
^{t}RAS	52	125,000	60	125,000	ns
^{t}RC	90		110		ns
$^{t}RCD1$	20		20		ns
$^{t}RCD2$	40		45		ns
^{t}RCH	5		5		ns
^{t}RCS	3		4		ns
^{t}RP	30		40		ns
^{t}WCH	5		5		ns
^{t}WCS	3		4		ns
^{t}WHZ	4	10	4	10	ns

NEW DRAM SIMM

BURST EDO WRITE/READ CYCLE



NOTE:

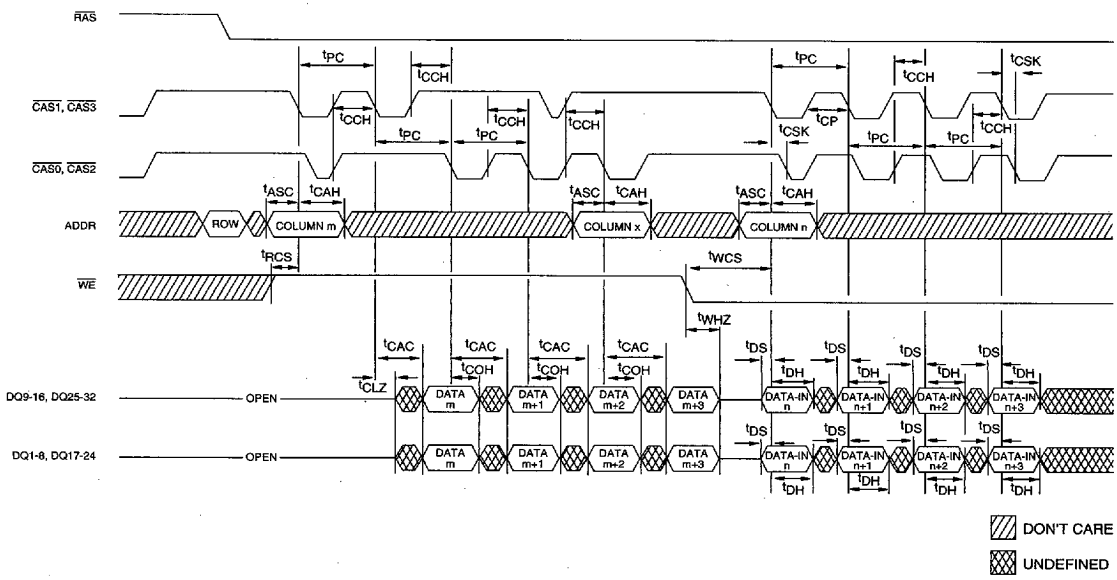
1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. Latch column address; start burst READ cycle.
6. Output data 1; increment column address.
7. Output data 2; increment column address.
8. Output data 3; increment column address.
9. $\overline{WE}$ transitioning HIGH will terminate the burst and reset the burst counter. The ^{t}BTH time is not required as it is satisfied by ^{t}RCS; ^{t}TP is met by the WRITE burst being terminated by a READ burst.
10. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until ^{t}BTHZ (MIN) and ^{t}WHZ (MIN) have both been satisfied and will reach the High-Z state once ^{t}BTHZ (MAX) and ^{t}WHZ (MAX) have both been satisfied.
11. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQ pins in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{RAS}$ or $\overline{CAS}$) that transitions HIGH.

TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}ASC	1.5		1.5		ns
^{t}ASR	1.5		1.5		ns
^{t}BTH	3		3		ns
^{t}BTHZ	7	13	7	13	ns
^{t}CAC		10		11	ns
^{t}CAH	8.5		8.5		ns
^{t}CAS	5	10,000	5	10,000	ns
^{t}COH	3		3		ns
^{t}CP	5		5		ns
^{t}CRP	10		10		ns
^{t}DH	5		5		ns
^{t}DS	0		0		ns
^{t}OFF	4	10	4	10	ns
^{t}PC	15		16.6		ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}RAH	8.5		8.5		ns
^{t}RAS	52	125,000	60	125,000	ns
^{t}RC	90		110		ns
^{t}RCD1	20		20		ns
^{t}RCD2	40		45		ns
^{t}RCH	5		5		ns
^{t}RCS	3		4		ns
^{t}RP	30		40		ns
^{t}RSH	0		0		ns
^{t}TP	6		6		ns
^{t}WCH	5		5		ns
^{t}WCS	3		4		ns
^{t}WHZ	4	10	4	10	ns

BURST EDO READ/WORD-WRITE CYCLE



NOTE: 1. The $\overline{CAS}$ to $\overline{CAS}$ skew requirements apply to $\overline{CAS0}$ with $\overline{CAS1}$ and $\overline{CAS2}$ with $\overline{CAS3}$ on the MT2D(T)132 B only.

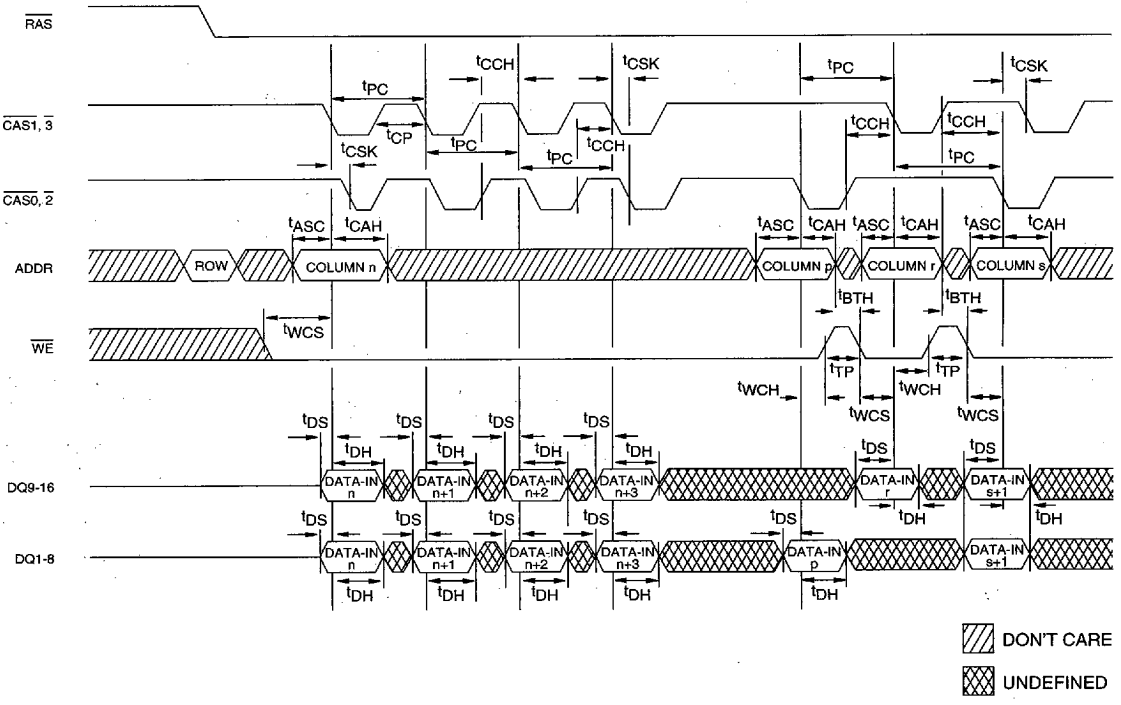
TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tASC	1.5		1.5		ns
tCAC		10		11	ns
tCAH	8.5		8.5		ns
tCCH	5		5		ns
tCLZ	3		3		ns
tCOH	3		3		ns
tCP	5		5		ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tCSK		2		2	ns
tDH	5		5		ns
tDS	0		0		ns
tPC	15		16.6		ns
tRCS	3		4		ns
tWCS	3		4		ns
tWHZ	4	10	4	10	ns

NEW DRAM SIMM

BURST EDO
WORD-WRITE/BYTE-WRITE CYCLE



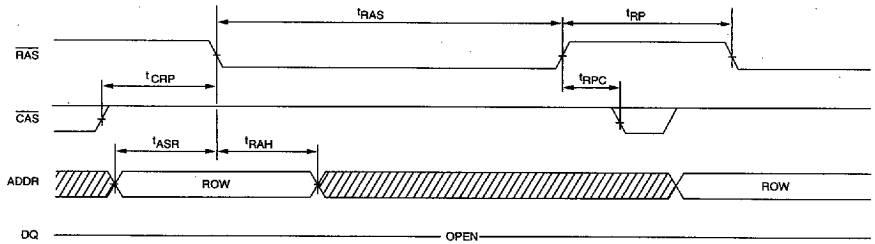
NOTE: 1. Applies to MT2D(T)132 B module only.

TIMING PARAMETERS

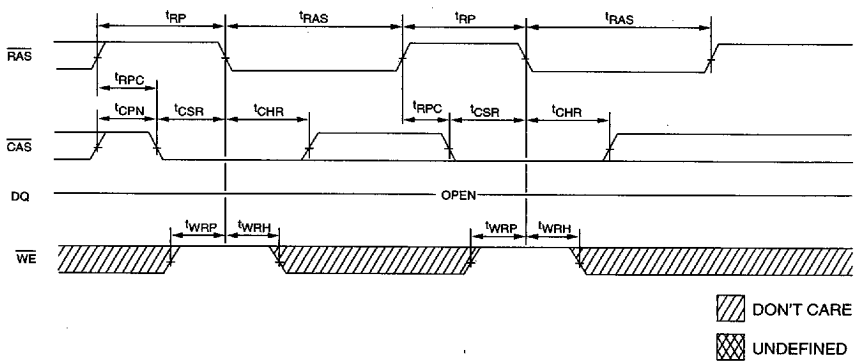
	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tASC	1.5		1.5		ns
tBTH	3		3		ns
tCAH	8.5		8.5		ns
tCCH	5		5		ns
tCP	5		5		ns
tCSK		2		2	ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tDH	5		5		ns
tDS	0		0		ns
tPC	15		16.6		ns
tTP	6		6		ns
tWCH	5		5		ns
tWCS	3		4		ns

RAS-ONLY REFRESH CYCLE



CBR REFRESH CYCLE



NOTE: 1. CBR REFRESH is recommended for all new designs to ensure compatibility with future generation DRAMs. Micron and JEDEC recommend CBR REFRESH as the preferred method of refresh for the 64 Meg DRAM generation and beyond.

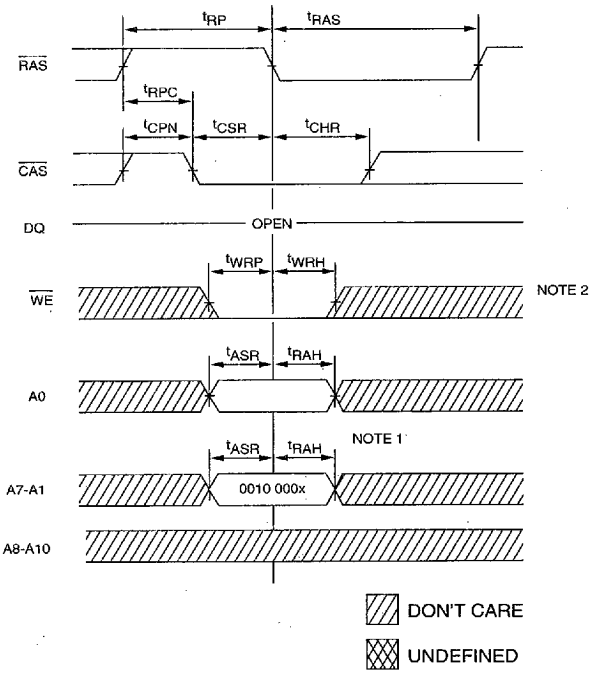
TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tASR	1.5		1.5		ns
tCHR	15		15		ns
tCPN	10		10		ns
tCRP	10		10		ns
tCSR	10		10		ns
tRAH	8.5		8.5		ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAS	52	125,000	60	125,000	ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	10		10		ns
tWRP	10		10		ns

NEW DRAM SIMM

WCBR PROGRAM CYCLE



NOTE:
1. A0 LOW sets the burst sequence to linear bursts. A0 HIGH sets the burst sequence to interleave bursts. Addresses A8 through A10 are "don't cares." Addresses A7-A0 should contain the state of (0010 000x where x=A0) to ensure future compatability. The burst sequence will remain set until the device power is interrupted or another WCBR cycle is executed.
2. A RAS-ONLY or CBR REFRESH cycle must be executed after the WCBR cycle to exit the programming mode.

TIMING PARAMETERS

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tASR	1.5		1.5		ns
tCHR	15		15		ns
tCPN	10		10		ns
tCSR	10		10		ns
tRAH	8.5		8.5		ns

	-52		-60		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAS	52	125,000	60	125,000	ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	10		10		ns
tWRP	10		10		ns