

SMALL-OUTLINE DRAM MODULE

1 MEG, 2 MEG x 64

8, 16 MEGABYTE, 3.3V, OPTIONAL
EXTENDED REFRESH, FAST PAGE OR EDO
PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 144-pin, small-outline, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V $\pm 0.3V$ power supply
- All device pins are TTL-compatible
- Low power, 24mW standby; 1,012mW active, typical (16MB)
- Refresh modes: RAS# ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN; optional Extended CBR
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE (FPM) operating mode or Extended Data-Out (EDO) PAGE MODE operating mode
- Serial Presence-Detect (SPD)

OPTIONS

- Timing
60ns access
70ns access
- Packages
144-pin Small-Outline DIMM (gold)
- Operating Modes
FAST PAGE MODE
EDO PAGE MODE
- Refresh
Standard/16ms
Extended Refresh/128ms

MARKING

-6
-7

G

Blank
X

Blank
L

KEY TIMING PARAMETERS

EDO Operating Mode

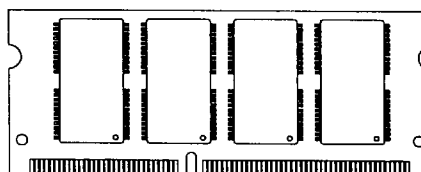
SPEED	RC	RAC	PC	AA	CAC	CAS
-6	105ns	60ns	25ns	30ns	15ns	12ns
-7	125ns	70ns	30ns	35ns	20ns	12ns

FPM Operating Mode

SPEED	RC	RAC	PC	AA	CAC	RP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)

144-Pin Small-Outline DIMM



PIN #	FRONT	PIN #	BACK	PIN #	FRONT	PIN #	BACK
1	Vss	2	Vss	73	OE#	74	RFU
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	RSVD	78	RSVD
7	DQ2	8	DQ34	79	RSVD	80	RSVD
9	DQ3	10	DQ35	81	Vcc	82	Vcc
11	Vcc	12	Vcc	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	CAS0#	24	CAS4#	95	DQ21	96	DQ53
25	CAS1#	26	CAS5#	97	DQ22	98	DQ54
27	Vcc	28	Vcc	99	DQ23	100	DQ55
29	A0	30	A3	101	Vcc	102	Vcc
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	RSVD
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	RSVD
39	DQ9	40	DQ41	111	A10	112	RSVD
41	DQ10	42	DQ42	113	Vcc	114	Vcc
43	DQ11	44	DQ43	115	CAS2#	116	CAS6#
45	Vcc	46	Vcc	117	CAS3#	118	CAS7#
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	RSVD	58	RSVD	129	Vcc	130	Vcc
59	RSVD	60	RSVD	131	DQ28	132	DQ60
61	RFU	62	RFU	133	DQ29	134	DQ61
63	Vcc	64	Vcc	135	DQ30	136	DQ62
65	RFU	66	RFU	137	DQ31	138	DQ63
67	WE#	68	RFU	139	Vss	140	Vss
69	RAS0#	70	RFU	141	SDA	142	SCL
71	RAS1#*	72	RFU	143	Vcc	144	Vcc

*16MB version only



ADVANCE MT4LDT164H(X)(L), MT8LDT264H(X)(L) 1 MEG, 2 MEG x 64 DRAM MODULES

PART NUMBERS

EDO Operating Mode

PART NUMBER	DESCRIPTION
MT4LDT164HG-xx X	1 Meg x 64, EDO
MT4LDT164HG-xx XL	1 Meg x 64, EDO, Extended Refresh
MT8LDT264HG-xx X	2 Meg x 64, EDO
MT8LDT264HG-xx XL	2 Meg x 64, EDO, Extended Refresh

xx = speed

FPM Operating Mode

PART NUMBER	DESCRIPTION
MT4LDT164HG-xx	1 Meg x 64
MT4LDT164HG-xx L	1 Meg x 64, Extended Refresh
MT8LDT264HG-xx	2 Meg x 64
MT8LDT264HG-xx L	2 Meg x 64, Extended Refresh

xx = speed

GENERAL DESCRIPTION

The MT4LDT164H(X)(L) and MT8LDT264H(X)(L) are randomly accessed 8MB and 16MB solid-state memories organized in a small outline x64 configuration. They are specially processed to operate from +3.0V to 3.6V for low voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. RAS# is used to latch the first 10 bits and CAS# the latter 10 bits.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode, while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS#, followed by a column-address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column-addresses, thus executing faster memory

cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" option, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (t_{CP}) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH (reference MT4LC1M16E5 DRAM data sheet for additional information on EDO functionality).

REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS# ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (A0-A9) are executed at least every t_{REF}, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

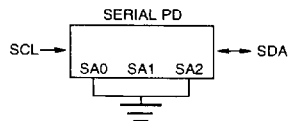
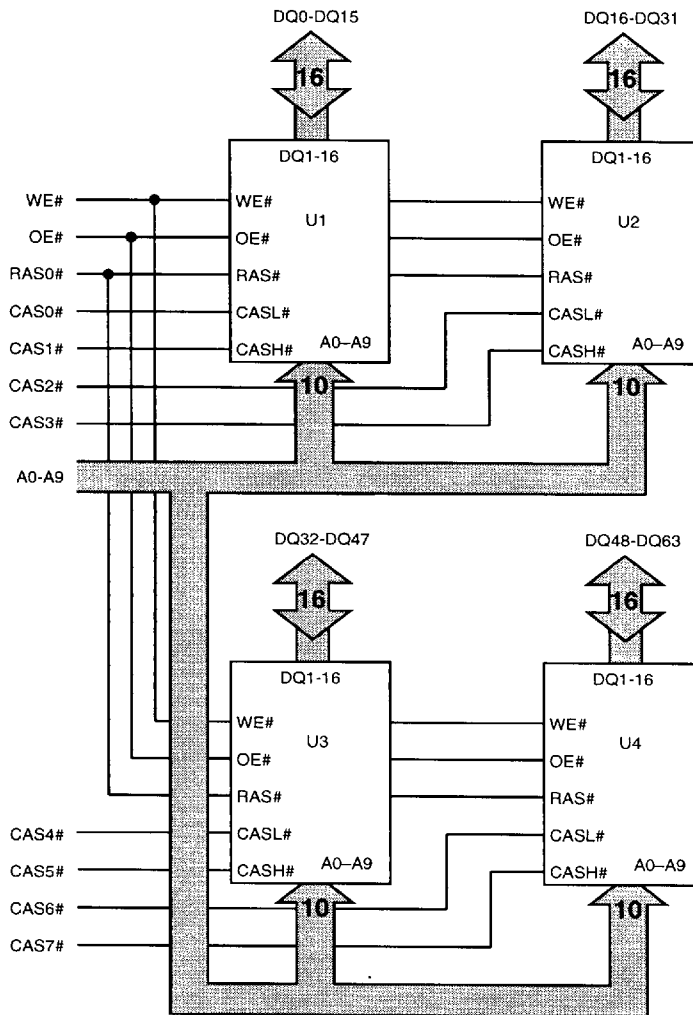
STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time.

SERIAL PRESENCE-DETECT EEPROM

This module incorporates Serial Presence Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM. This nonvolatile storage device contains data programmed by Micron that identifies the module type and various DRAM organization and timing parameters. System READ/WRITE operations to the EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals. The EEPROM device operates with a V_{cc} of 3.3V ±0.3V.

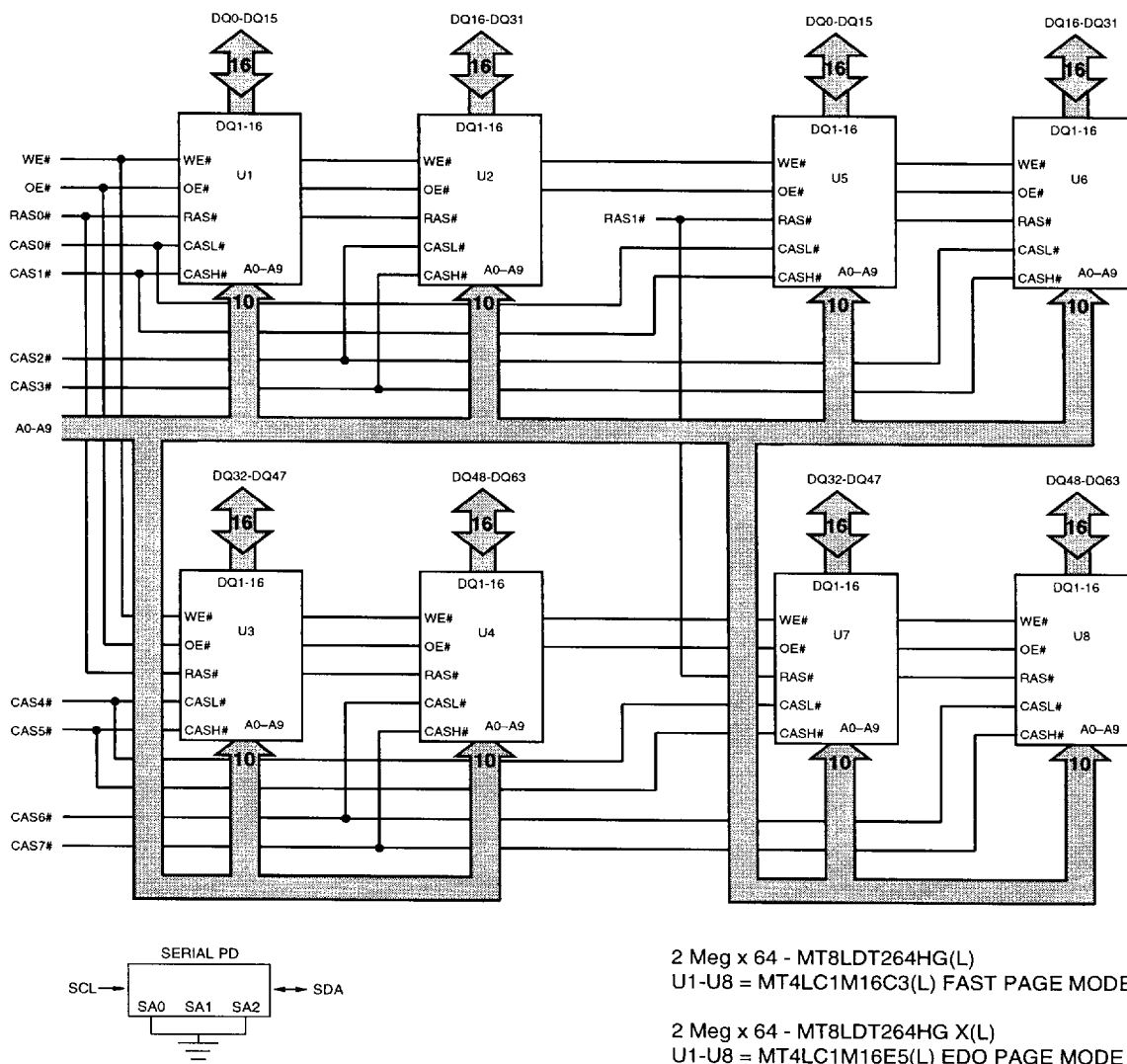
FUNCTIONAL BLOCK DIAGRAM
MT4LDT164H (8MB)



1 Meg x 64 - MT4LDT164HG(L)
U1-U4 = MT4LC1M16C3(L) FAST PAGE MODE

1 Meg x 64 - MT4LDT164HG X(L)
U1-U4 = MT4LC1M16E5(L) EDO PAGE MODE

FUNCTIONAL BLOCK DIAGRAM
MT8LDT264H (16MB)





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MT4LDT164H(X)(L), MT8LDT264H(X)(L)
1 MEG, 2 MEG x 64 DRAM MODULES

SERIAL PRESENCE-DETECT EEPROM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1) ($V_{CC} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	$V_{CC} \times .7$	$V_{CC} \times .5$	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	$V_{CC} \times .3$	V	
OUTPUT LOW VOLTAGE, $I_{OUT} = 3mA$	V_{OL}		0.4	V	
INPUT LEAKAGE CURRENT, $V_{IN} = GND$ to V_{CC}	I_{LI}		10	μA	
OUTPUT LEAKAGE CURRENT, $V_{OUT} = GND$ to V_{CC}	I_{LO}		10	μA	
STANDBY CURRENT SCL = SDA = $V_{CC} - 0.3V$, All other inputs = GND or $V_{CC} 3.3V + 10\%$	I_{SB}		30	μA	
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I_{CC}		2	mA	

SERIAL PRESENCE-DETECT EEPROM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 1) ($V_{CC} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS					
PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	t_{AA}	0.3	3.5	μs	
Time the bus must be free before a new transition can start	t_{BUF}	4.7		μs	
Data-out hold time	t_{DH}	300		ns	
SDA and SCL fall time	t_F		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		μs	
Start condition hold time	$t_{HD:STA}$	4		μs	
Clock HIGH period	t_{HIGH}	4		μs	
Noise suppression time constant at SCL, SDA inputs	t_I		100	ns	
Clock LOW period	t_{LOW}	4.7		μs	
SDA and SCL rise time	t_R		1	μs	
SCL clock frequency	f_{SCL}		100	KHz	
Data-in setup time	$t_{SU:DAT}$	250		ns	
Start condition setup time	$t_{SU:STA}$	4.7		μs	
Stop condition setup time	$t_{SU:STO}$	4.7		μs	
WRITE cycle time	t_{WR}		10	ms	32



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SERIAL PRESENCE-DETECT MATRIX

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BYTE 0: NUMBER OF BYTES USED BY MICRON								
128	1	0	0	0	0	0	0	0
BYTE 1: TOTAL NUMBER OF SPD MEMORY BYTES								
256	0	0	0	0	1	0	0	0
BYTE 2: MEMORY TYPE								
FAST PAGE MODE	0	0	0	0	0	0	0	1
EDO PAGE MODE	0	0	0	0	0	0	1	0
BYTE 3: NUMBER OF ROW ADDRESSES								
10	0	0	0	0	1	0	1	0
BYTE 4: NUMBER OF COLUMN ADDRESSES								
10	0	0	0	0	1	0	1	0
BYTE 5: NUMBER OF BANKS								
1 (1 Meg x 64)	0	0	0	0	0	0	0	1
2 (2 Meg x 64)	0	0	0	0	0	0	1	0
BYTE 6: DATA WIDTH								
x64	0	1	0	0	0	0	0	0
BYTE 7: DATA WIDTH (continued)								
NONE	0	0	0	0	0	0	0	0
BYTE 8: VOLTAGE INTERFACE								
LVTTTL	0	0	0	0	0	0	0	1
BYTE 9: RAS# ACCESS TIME								
60ns	0	0	1	1	1	1	0	0
70ns	0	1	0	0	0	1	1	0
BYTE 10: CAS# ACCESS TIME								
10ns	0	0	0	0	1	0	1	0
12ns	0	0	0	0	1	1	0	0
BYTE 11: MODULE CONFIGURATION TYPE								
NON-PARITY	0	0	0	0	0	0	0	0
BYTE 12: REFRESH RATES								
NORMAL (15.625µs)	0	0	0	0	0	0	0	0
EXTENDED (8X - 125µs)	0	0	0	0	0	1	0	1

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH" / "driven to LOW."



ADVANCE
MT4LDT164H(X)(L), MT8LDT264H(X)(L)
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TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	ADDRESSES		DATA-IN/OUT
					'R	'C	DQ0-DQ63
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
EDO/FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS#-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
Extended CBR REFRESH (L version)		H→L	L	H	X	X	High-Z



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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} -1V to +4.6V
Voltage on Inputs or I/O pins
relative to V_{SS} -1V to +5.5V
Operating Temperature, T_A (ambient) 0°C to +70°C
Storage Temperature (plastic) -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V _{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V _{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		V _{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ 5.5V (All other pins not under test = 0V) for each package input	RAS0#-1#	I _{I1}	-8	8	μA	
	A0-A9, WE#, OE#	I _{I2}	-16	16	μA	25
	CAS0#-CAS7#	I _{I3}	-4	4	μA	25
	DQ0-DQ63	I _{O2}	-20	20	μA	25
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V) for each package input						
OUTPUT LEVELS						
Output High Voltage (I _{OUT} = -2mA)		V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 2mA)		V _{OL}		0.4	V	



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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 5, 6) ($V_{CC} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX		UNITS	NOTES
			-6	-7		
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I _{cc1}	8MB 16MB	8 16	8 16	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = $V_{CC} - 0.2V$)	I _{cc2}	8MB 16MB	2 4	2 4	mA	28
	I _{cc2} (L only)	8MB 16MB	0.6 1.2	0.6 1.2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, Address Cycling: $t_{RC} = t_{RC} [MIN]$)	I _{cc3}	8MB 16MB	680 688	620 628	mA	3, 24
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL} , CAS#, Address Cycling: $t_{PC} = t_{PC} [MIN]$; t_{CP} , $t_{ASC} = 10ns$)	I _{cc4}	8MB 16MB	400 408	360 368	mA	3, 24
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL} , CAS#, Address Cycling: $t_{PC} = t_{PC} [MIN]$)	I _{cc5} (X only)	8MB 16MB	480 488	440 448	mA	3, 24
REFRESH CURRENT: RAS# ONLY Average power supply current (RAS# Cycling, CAS# = V_{IH} ; $t_{RC} = t_{RC} [MIN]$)	I _{cc6}	8MB 16MB	640 648	580 588	mA	3, 24
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, Address Cycling: $t_{RC} = t_{RC} [MIN]$)	I _{cc7}	8MB 16MB	600 608	560 568	mA	3, 4
REFRESH CURRENT: Extended (L-version only) Average power supply current during Extended Refresh: CAS# = 0.2V or CBR cycling; RAS# = $t_{RAS} [MIN]$; WE# = $V_{CC} - 0.2V$; A0-A9 and $D_{IN} = V_{CC} - 0.2V$ or 0.2V (D_{IN} may be left open); $t_{RC} = 125\mu s$ (1024 rows at $125\mu s = 128ms$)	I _{cc8} (L only)	8MB 16MB	1.2 2.4	1.2 2.4	mA	3, 4



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CAPACITANCE

PARAMETER	SYMBOL	8MB	16MB	UNITS	NOTES
Input Capacitance: A0-A9	C _{I1}	24	46	pF	2
Input Capacitance: WE#, OE#	C _{I2}	32	62	pF	2
Input Capacitance: RAS0# - RAS1#	C _{I3}	32	32	pF	2
Input Capacitance: CAS0# - CAS7#	C _{I4}	10	20	pF	2
Input/Output Capacitance: DQ0-DQ63	C _{IO1}	10	18	pF	2
Input/Output Capacitance: SDA, SCL	C _{IO2}	10	10	pF	

FAST PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
Access time from column-address	t _{AA}		30		35	ns	
Column-address hold time (referenced to RAS#)	t _{AR}	50		55		ns	
Column-address setup time	t _{ASC}	0		0		ns	
Row-address setup time	t _{ASR}	0		0		ns	
Column-address to WE# delay time	t _{AWD}	55		60		ns	20
Access time from CAS#	t _{CAC}		15		20	ns	14
Column-address hold time	t _{CAH}	10		15		ns	
CAS# pulse width	t _{CAS}	15	10,000	20	10,000	ns	
CAS# hold time (CBR REFRESH)	t _{CHR}	15		15		ns	4
Last CAS# going LOW to first CAS# to return HIGH	t _{CLCH}	10		10		ns	33
CAS# to output in Low-Z	t _{CLZ}	3		3		ns	23
CAS# precharge time	t _{CP}	10		10		ns	15
Access time from CAS# precharge	t _{CPA}		35		40	ns	
CAS# to RAS# precharge time	t _{CRP}	5		5		ns	
CAS# hold time	t _{CSH}	60		70		ns	
CAS# setup time (CBR REFRESH)	t _{CSR}	5		5		ns	4
CAS# to WE# delay time	t _{CWD}	40		45		ns	20, 29
Write command to CAS# lead time	t _{CWL}	15		20		ns	
Data-in hold time	t _{DH}	10		15		ns	20
Data-in hold time (referenced to RAS#)	t _{DHR}	45		55		ns	
Data-in setup time	t _{DS}	0		0		ns	20
Output disable	t _{OD}	3	15	3	20	ns	27, 28, 39
Output enable	t _{OE}		15		20	ns	32
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t _{OEH}	15		20		ns	27
Output buffer turn-off delay	t _{OFF}	3	15	3	20	ns	19, 23
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t _{ORD}	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t _{PC}	35		40		ns	
Access time from RAS#	t _{RAC}		60		70	ns	13
RAS# to column-address delay time	t _{RAD}	15	30	15	35	ns	17
Row-address hold time	t _{RAH}	10		10		ns	
Column-address to RAS# lead time	t _{RAL}	30		35		ns	



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FAST PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{cc} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
RAS# pulse width	t_{RAS}	60	10,000	70	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	t_{RC}	110		130		ns	
RAS# to CAS# delay time	t_{RCD}	20	45	20	50	ns	16
Read command hold time (referenced to CAS#)	t_{RCH}	0		0		ns	18
Read command setup time	t_{RCS}	0		0		ns	
Refresh period (1,024 cycles)	t_{REF}		16		16	ms	
Refresh period (1,024 cycles) L version	t_{REF}		128		128	ms	
RAS# precharge time	t_{RP}	40		50		ns	
RAS# to CAS# precharge time	t_{RPC}	0		0		ns	
Read command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	18
RAS# hold time	t_{RSH}	15		20		ns	
READ WRITE cycle time	t_{RWC}	150		180		ns	
RAS# to WE# delay time	t_{RWD}	85		95		ns	20
Write command to RAS# lead time	t_{RWL}	15		20		ns	
Transition time (rise or fall)	t_T	3	50	3	50	ns	
Write command hold time	t_{WCH}	10		15		ns	
Write command hold time (referenced to RAS#)	t_{WCR}	45		55		ns	
WE# command setup time	t_{WCS}	0		0		ns	
Write command pulse width	t_{WP}	10		15		ns	
WE# hold time (CBR REFRESH)	t_{WRH}	10		10		ns	
WE# setup time (CBR REFRESH)	t_{WRP}	10		10		ns	



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EDO PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
Access time from column-address	t_{AA}		30		35	ns	
Column-address setup to CAS# precharge during WRITE	t_{ACH}	15		15		ns	
Column-address hold time (referenced to RAS#)	t_{AR}	45		55		ns	
Column-address setup time	t_{ASC}	0		0		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Column-address to WE# delay time	t_{AWD}	55		60		ns	13
Access time from CAS#	t_{CAC}		15		20	ns	14
Column-address hold time	t_{CAH}	10		12		ns	
CAS# pulse width	t_{CAS}	10	10,000	12	10,000	ns	
CAS# hold time (CBR REFRESH)	t_{CHR}	10		12		ns	4
Last CAS# going LOW to first CAS# to return HIGH	t_{CLCH}	10		10		ns	29
CAS# to output in Low-Z	t_{CLZ}	0		0		ns	
Data output hold after next CAS# LOW	t_{COH}	3		3		ns	
CAS# precharge time	t_{CP}	10		10		ns	15
Access time from CAS# precharge	t_{CPA}		35		40	ns	
CAS# to RAS# precharge time	t_{CRP}	5		5		ns	
CAS# hold time	t_{CSH}	50		55		ns	
CAS# setup time (CBR REFRESH)	t_{CSR}	5		5		ns	4
CAS# to WE# delay time	t_{CWD}	35		40		ns	13, 25
Write command to CAS# lead time	t_{CWL}	15		15		ns	
Data-in hold time	t_{DH}	10		12		ns	20
Data-in hold time (referenced to RAS#)	t_{DHR}	45		55		ns	
Data-in setup time	t_{DS}	0		0		ns	20
Output disable	t_{OD}	0	15	0	15	ns	
Output Enable	t_{OE}		15		20	ns	19, 23
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t_{OEHL}	12		12		ns	18
OE# HIGH hold from CAS# HIGH	t_{OEHL}	10		10		ns	18
OE# HIGH pulse width	t_{OEP}	10		10		ns	
OE# LOW to CAS# HIGH setup time	t_{OES}	5		5		ns	
Output buffer turn-off delay	t_{OFF}	3	15	3	15	ns	19, 23
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	75		85		ns	31
Access time from RAS#	t_{RAC}		60		70	ns	13
RAS# to column-address delay time	t_{RAD}	12	30	12	35	ns	17
Row-address hold time	t_{RAH}	10		10		ns	
Column-address to RAS# lead time	t_{RAL}	30		35		ns	
RAS# pulse width	t_{RAS}	60	10,000	70	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	t_{RASP}	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	110		130		ns	
RAS# to CAS# delay time	t_{RCD}	14	45	14	50	ns	16
Read command hold time (referenced to CAS#)	t_{RCH}	0		0		ns	18
Read command setup time	t_{RCS}	0		0		ns	



ADVANCE
MT4LDT164H(X)(L), MT8LDT264H(X)(L)
1 MEG, 2 MEG x 64 DRAM MODULES

EDO PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{cc} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
Refresh period (1,024 cycles)	t_{REF}		16		16	ms	
Refresh period (1,024 cycles) L version	t_{REF}		128		128	ms	
RAS# precharge time	t_{RP}	40		50		ns	
RAS# to CAS# precharge time	t_{RPC}	0		0		ns	
Read command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	18
RAS# hold time	t_{RSH}	10		12		ns	
READ WRITE cycle time	t_{RWC}	145		170		ns	
RAS# to WE# delay time	t_{RWD}	80		90		ns	13
Write command to RAS# lead time	t_{RWL}	15		15		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	
Write command hold time	t_{WCH}	10		12		ns	
Write command hold time (referenced to RAS#)	t_{WCR}	45		55		ns	
WE# command setup time	t_{WCS}	0		0		ns	
Output disable delay from WE# (CAS# HIGH)	t_{WHZ}	0	13	0	15	ns	
Write command pulse width	t_{WP}	10		12		ns	
WE# pulse width for output disable when CAS# HIGH	t_{WPZ}	10		12		ns	
WE# hold time (CBR REFRESH)	t_{WRH}	10		10		ns	
WE# setup time (CBR REFRESH)	t_{WRP}	10		10		ns	

NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = +3.3V \pm 0.3V$; $f = 1$ MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
6. An initial pause of 100 μ s is required after power-up, followed by eight RAS# refresh cycles (RAS# ONLY or CBR with WE# HIGH) before proper device operation is assured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5$ ns for FAST PAGE MODE and $t_T = 2.5$ ns for EDO PAGE MODE.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH} , data output is High-Z.
11. If CAS# = V_{IL} , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
13. Assumes that $t_{RCD} < t_{RCD} (MAX)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
14. Assumes that $t_{RCD} \geq t_{RCD} (MAX)$.
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP} .
16. Operation within the $t_{RCD} (MAX)$ limit ensures that $t_{RAC} (MAX)$ can be met. $t_{RCD} (MAX)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} (MAX)$ limit, then access time is controlled exclusively by t_{CAC} , provided t_{RAD} is not exceeded.
17. Operation within the $t_{RAD} (MAX)$ limit ensures that $t_{RAC} (MIN)$ and $t_{CAC} (MIN)$ can be met. $t_{RAD} (MAX)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD} (MAX)$ limit, then access time is controlled exclusively by t_{AA} , provided t_{RCD} is not exceeded.
18. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
19. $t_{OFF} (MAX)$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} . It is referenced from the rising edge of RAS# or CAS#, whichever occurs last.
20. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
21. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, WE# must be pulsed during CAS# HIGH time in order to place I/O buffers in High-Z.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
23. The 3ns minimum is a parameter guaranteed by design.
24. Column-address changed once each cycle.
25. 8MB module values will be half of those shown.
26. For FAST PAGE MODE option, t_{OFF} is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, t_{OFF} on an EDO option is determined by the latter of the RAS# and CAS# signal to transition HIGH.
27. Applies to both EDO and FAST PAGE MODE operating modes.
28. All other inputs at 0.2V or $V_{CC} - 0.2V$.
29. L version only.
30. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. t_{RWD} , t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If $t_{WCS} \geq t_{WCS} (MIN)$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{WCS} < t_{WCS} (MIN)$ and $t_{RWD} \geq t_{RWD} (MIN)$, $t_{AWD} \geq t_{AWD} (MIN)$ and $t_{CWD} \geq t_{CWD} (MIN)$, the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.

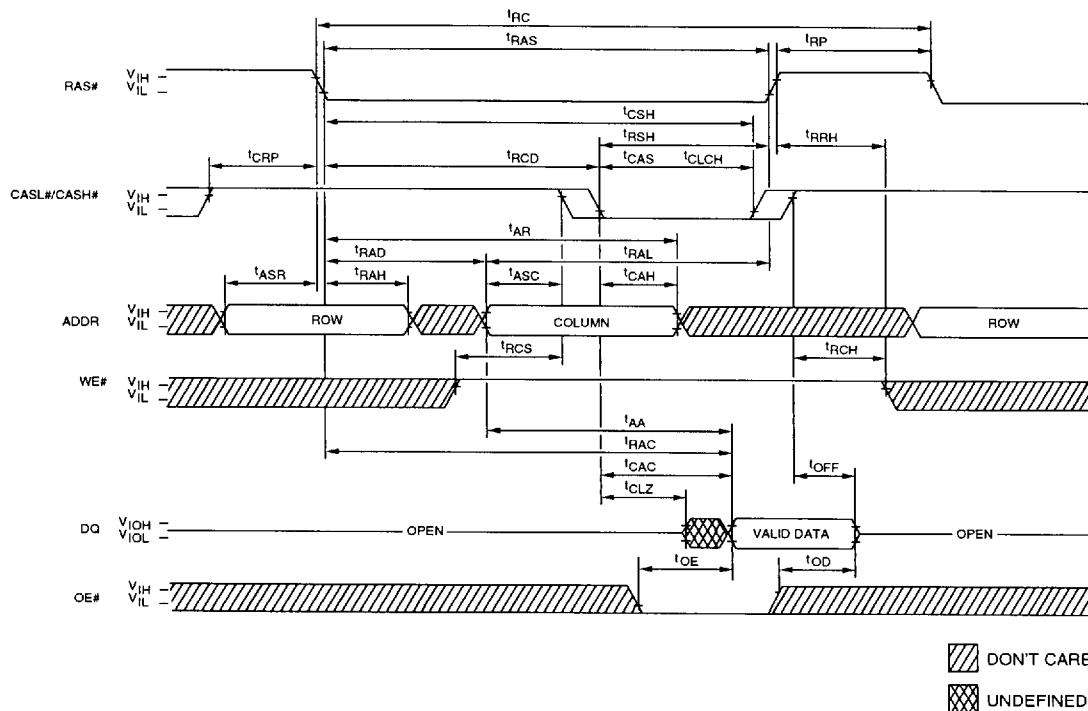


ADVANCE
MT4LDT164H(X)(L), MT8LDT264H(X)(L)
1 MEG, 2 MEG x 64 DRAM MODULES

NOTES (continued)

31. LATE WRITE and READ-MODIFY-WRITE cycles must have both 'OD and 'OE_H met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after 'OE_H is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
32. The SPD EEPROM WRITE cycle time (t_{WR}) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

READ CYCLE
(FAST PAGE MODE Module)

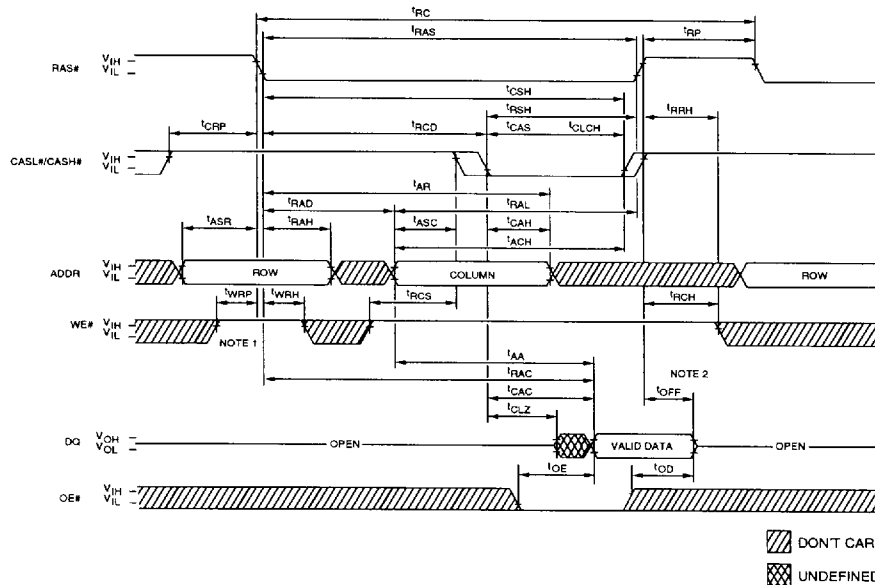


FAST PAGE MODE
TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t _{AA}		30		35	ns
t _{AR}	50		55		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		15		20	ns
t _{CAH}	10		15		ns
t _{CAS}	15	10,000	20	10,000	ns
t _{CLCH}	10		10		ns
t _{CLZ}	3		3		ns
t _{CRP}	5		5		ns
t _{CSH}	60		70		ns
t _{OD}	3	15	3	20	ns
t _{OE}		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t _{OFF}	3	15	3	20	ns
t _{RAC}		60		70	ns
t _{RAD}	15	30	15	35	ns
t _{RAH}	10		10		ns
t _{RAL}	30		35		ns
t _{RAS}	60	10,000	70	10,000	ns
t _{RC}	110		130		ns
t _{RCD}	20	45	20	50	ns
t _{RCH}	0		0		ns
t _{RCS}	0		0		ns
t _{RP}	40		50		ns
t _{RRH}	0		0		ns
t _{RSH}	15		20		ns

READ CYCLE
(EDO PAGE MODE Module)



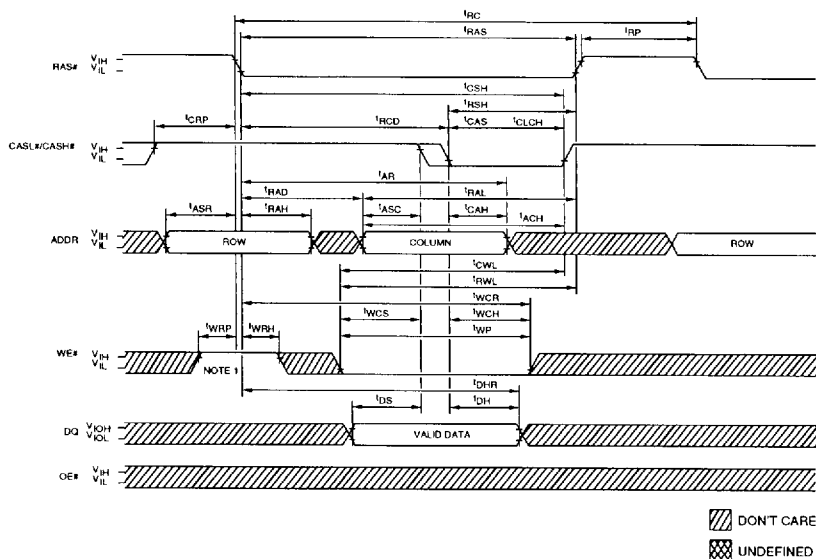
- NOTE:**
1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
 2. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EDO PAGE MODE
TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tACH	15		15		ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		12		ns
tCAS	12	10,000	13	10,000	ns
tCLCH	10		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	50		55		ns
tOD	0	15	0	15	ns
tOE		15		15	ns
tOFF	3	15	3	15	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAC		60		70	ns
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC	105		125		ns
tRCD	14	45	14	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	13		15		ns
tWRH	10		10		ns
tWRP	10		10		ns

EARLY WRITE CYCLE 27

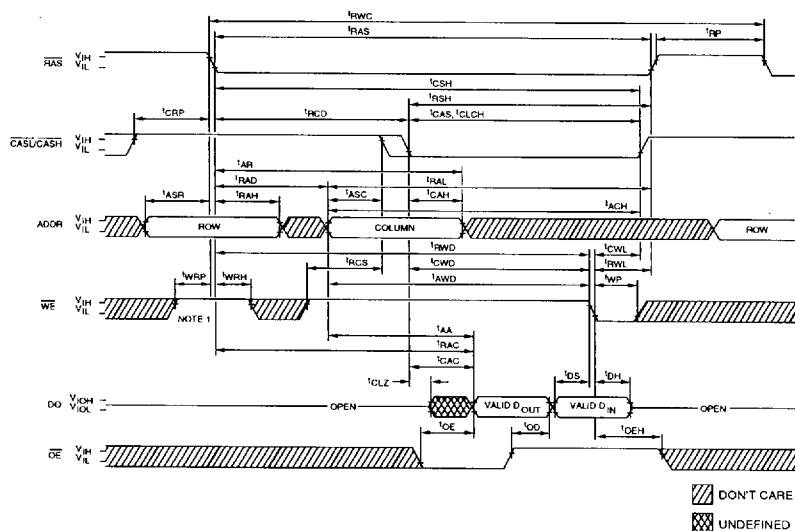


FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{ACH} (EDO)	15		15		ns
t _{AR} (FPM)	50		55		ns
t _{AR} (EDO)	45		50		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAH} (FPM)	10		15		ns
t _{CAH} (EDO)	10		12		ns
t _{CAS} (FPM)	15	10,000	20	10,000	ns
t _{CAS} (EDO)	12	10,000	13	10,000	ns
t _{CLCH}	10		10		ns
t _{CRP}	5		5		ns
t _{CSH} (FPM)	60		70		ns
t _{CSH} (EDO)	50		55		ns
t _{CWL} (FPM)	15		20		ns
t _{CWL} (EDO)	15		15		ns
t _{DH} (FPM)	10		15		ns
t _{DH} (EDO)	10		12		ns
t _{DHR}	45		55		ns
t _{DS}	0		0		ns
t _{RAD} (FPM)	15	30	15	35	ns
t _{RAD} (EDO)	12	30	12	35	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{RAH}	10		10		ns
t _{RAL}	30		35		ns
t _{RAS}	60	10,000	70	10,000	ns
t _{RC} (FPM)	110		130		ns
t _{RC} (EDO)	105		125		ns
t _{RCD} (FPM)	20	45	20	50	ns
t _{RCD} (EDO)	14	45	14	50	ns
t _{RP}	40		50		ns
t _{RSH} (FPM)	15		20		ns
t _{RSH} (EDO)	13		15		ns
t _{RWL} (FPM)	15		20		ns
t _{RWL} (EDO)	15		15		ns
t _{WCH} (FPM)	10		15		ns
t _{WCH} (EDO)	10		12		ns
t _{WCR}	45		55		ns
t _{WCS}	0		0		ns
t _{WP} (FPM)	10		15		ns
t _{WP} (EDO)	10		12		ns
t _{WRH}	10		10		ns
t _{WRP}	10		10		ns

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



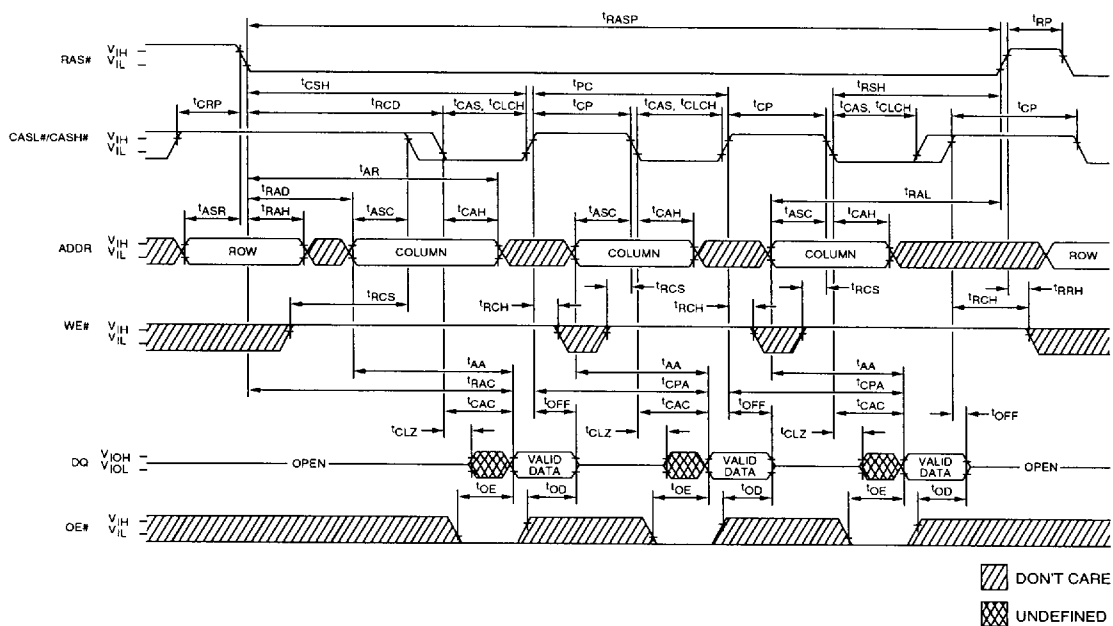
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE
TIMING PARAMETERS

SYM	-6		-7		UNITS
tAA	MIN	MAX	MIN	MAX	ns
tACH	15	30	15	35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	55		60		ns
tCAC		15		20	ns
tCAH	10		12		ns
tCAS	12	10,000	13	10,000	ns
tCLCH	10		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	50		55		ns
tCWD	35		40		ns
tCWL	15		15		ns
tDH	10		12		ns
tDS	0		0		ns
tOD	0	15	0	15	ns

SYM	-6		-7		UNITS
tOE	MIN	MAX	MIN	MAX	ns
tOEH	12	15	12	20	ns
tRAC		60		70	ns
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRCD	14	45	14	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	13		15		ns
tRWC	145		170		ns
tRWD	80		90		ns
tRWL	15		15		ns
tWP	10		12		ns
tWRH	10		10		ns
tWRP	10		10		ns

FAST-PAGE-MODE READ CYCLE

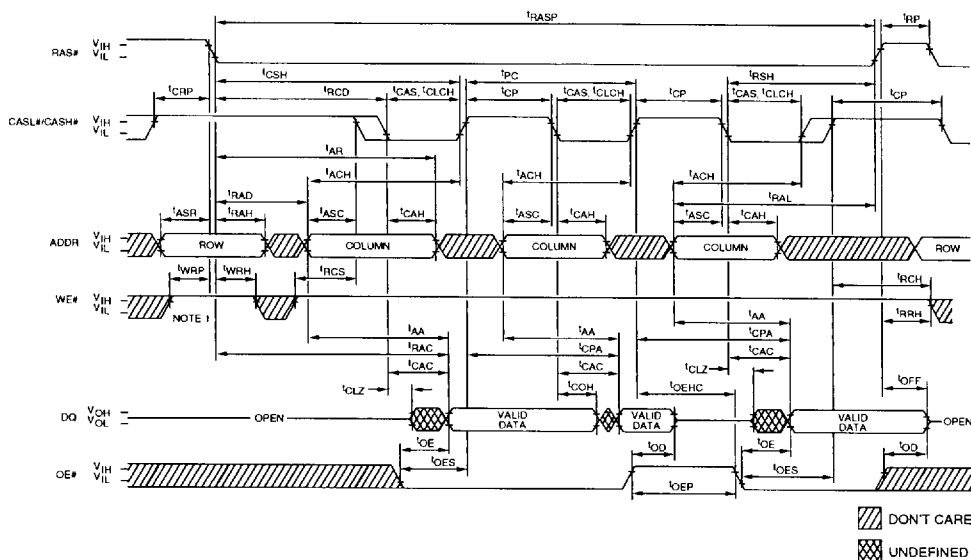


FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
1AA		30		35	ns
1AR	50		55		ns
1ASC	0		0		ns
1ASR	0		0		ns
1CAC		15		20	ns
1CAH	10		15		ns
1CAS	15	10,000	20	10,000	ns
1CLCH	10		10		ns
1CLZ	3		3		ns
1CP	10		10		ns
1CPA		35		40	ns
1CRP	5		5		ns
1CSH	60		70		ns
1OD	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
'OE		15		20	ns
'OFF	3	15	3	20	ns
'PC	35		40		ns
'RAC		60		70	ns
'RAD	15	30	15	35	ns
'RAH	10		10		ns
'RAL	30		35		ns
'RASP	60	100,000	70	100,000	ns
'RCD	20	45	20	50	ns
'RCH	0		0		ns
'RCS	0		0		ns
'RP	40		50		ns
'RRH	0		0		ns
'RSH	15		20		ns

EDO-PAGE-MODE READ CYCLE



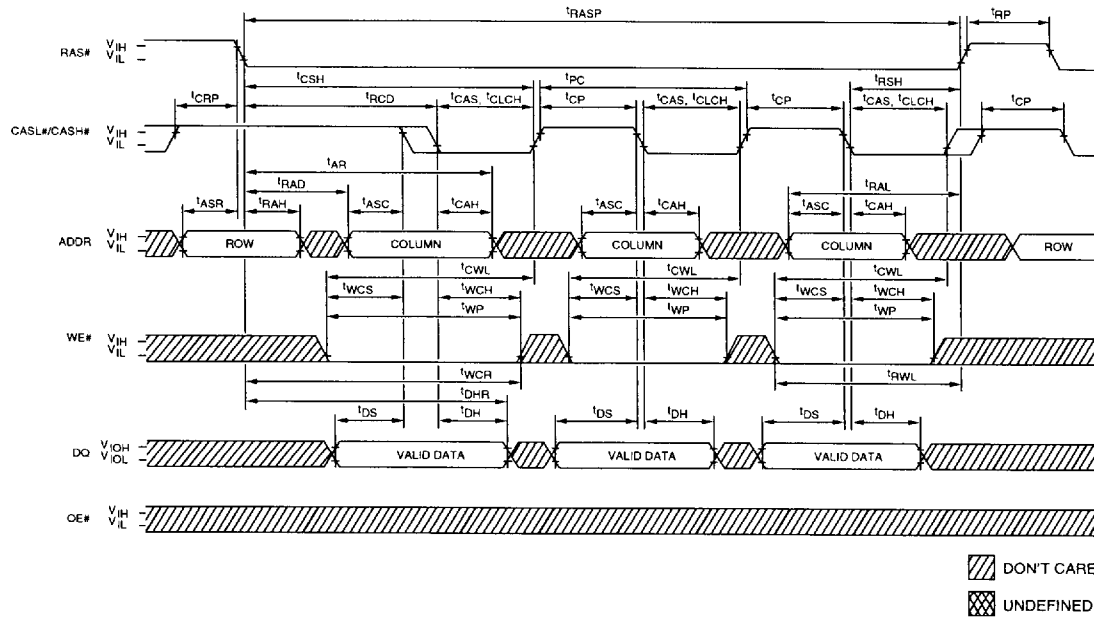
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMS.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
AA		30		35	ns
ACH	15		15		ns
AR	45		50		ns
ASC	0		0		ns
ASR	0		0		ns
CAC		15		20	ns
CAH	10		12		ns
CAS	12	10,000	13	10,000	ns
CLCH	10		10		ns
CLZ	0		0		ns
COH	3		3		ns
CP	10		10		ns
CPA		35		40	ns
CRP	5		5		ns
CSH	50		55		ns
OD	0	15	0	15	ns
OE		15		20	ns
OEHC	10		10		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ OEP	10		10		ns
¹ OES	5		5		ns
¹ OFF	3	15	3	15	ns
¹ PC	25		30		ns
¹ RAC		60		70	ns
¹ RAD	12	30	12	35	ns
¹ RAH	10		10		ns
¹ RAL	30		35		ns
¹ RASP	60	125,000	70	125,000	ns
¹ RCD	14	45	14	50	ns
¹ RCH	0		0		ns
¹ RCS	0		0		ns
¹ RP	40		50		ns
¹ RRH	0		0		ns
¹ RSH	13		15		ns
¹ WRH	10		10		ns
¹ WRP	10		10		ns

FAST-PAGE-MODE EARLY-WRITE CYCLE

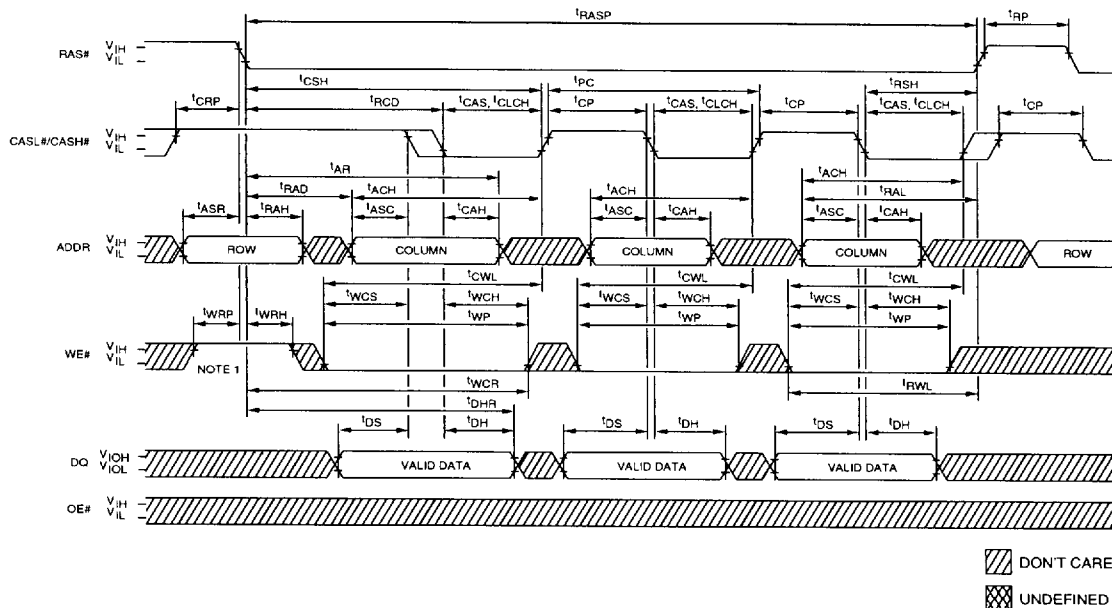


FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
'AR	50		55		ns
'ASC	0		0		ns
'ASR	0		0		ns
'CAH	10		15		ns
'CAS	15	10,000	20	10,000	ns
'CLCH	10		10		ns
'CP	10		10		ns
'CRP	5		5		ns
'CSH	60		70		ns
'CWL	15		20		ns
'DH	10		15		ns
'DHR	45		55		ns
'DS	0		0		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
'PC	35		40		ns
'RAD	15	30	15	35	ns
'RAH	10		10		ns
'RAL	30		35		ns
'RASP	60	100,000	70	100,000	ns
'RCD	20	45	20	50	ns
'RP	40		50		ns
'RSH	15		20		ns
'RWL	15		20		ns
'WCH	10		15		ns
'WCR	45		55		ns
'WCS	0		0		ns
'WP	10		15		ns

EDO-PAGE-MODE EARLY-WRITE CYCLE



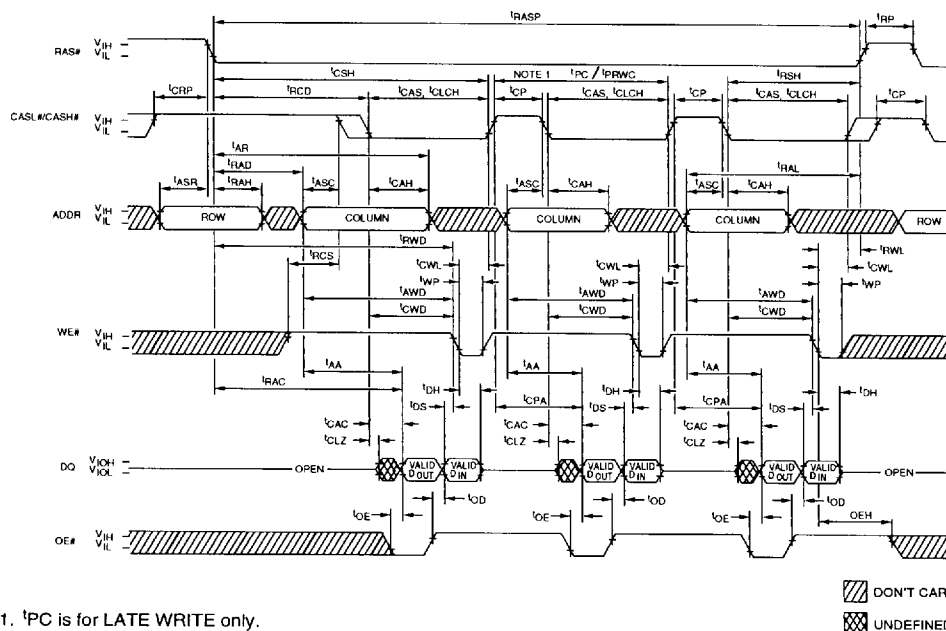
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for ¹WRP and ¹WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
ACH	15		15		ns
AR	45		50		ns
ASC	0		0		ns
ASR	0		0		ns
CAH	10		12		ns
CAS	12	10,000	13	10,000	ns
CLCH	10		10		ns
CP	10		10		ns
CRP	5		5		ns
CSH	50		55		ns
CWL	15		15		ns
DH	10		12		ns
DHR	45		55		ns
DS	0		0		ns
PC	25		30		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ RAD	12	30	12	35	ns
¹ RAH	10		10		ns
¹ RAL	30		35		ns
¹ RASP	60	125,000	70	125,000	ns
¹ RCD	14	45	14	50	ns
¹ RP	40		50		ns
¹ RSH	13		15		ns
¹ RWL	15		15		ns
¹ WCH	10		12		ns
¹ WCR	45		55		ns
¹ WCS	0		0		ns
¹ WP	10		12		ns
¹ WRH	10		10		ns
¹ WRP	10		10		ns

FAST-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)



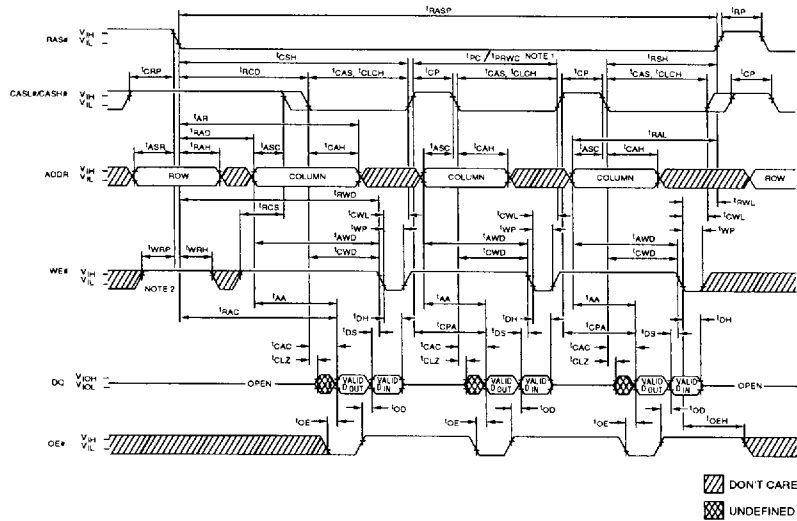
NOTE: 1. ^tPC is for LATE WRITE only.

TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
1AA		30		35	ns
1AR	50		55		ns
1ASC	0		0		ns
1ASR	0		0		ns
1AWD	55		60		ns
1CAC		15		20	ns
1CAH	10		15		ns
1CAS	15	10,000	20	10,000	ns
1CLCH	10		10		ns
1CLZ	3		3		ns
1CP	10		10		ns
1CPA		35		40	ns
1CRP	5		5		ns
1CSH	60		70		ns
1CWD	40		45		ns
1CWL	15		20		ns
1DH	10		15		ns
1DS	0		0		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
'OD	3	15	3	20	ns
'OE		15		20	ns
'OEH	15		20		ns
'PC	35		40		ns
'PRWC	85		95		ns
'RAC		60		70	ns
'RAD	15	30	15	35	ns
'RAH	10		10		ns
'RAL	30		35		ns
'RASP	60	100,000	70	100,000	ns
'RCD	20	45	20	50	ns
'RCS	0		0		ns
'RP	40		50		ns
'RSH	15		20		ns
'RWD	85		95		ns
'RWL	15		20		ns
'WP	10		15		ns

EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)



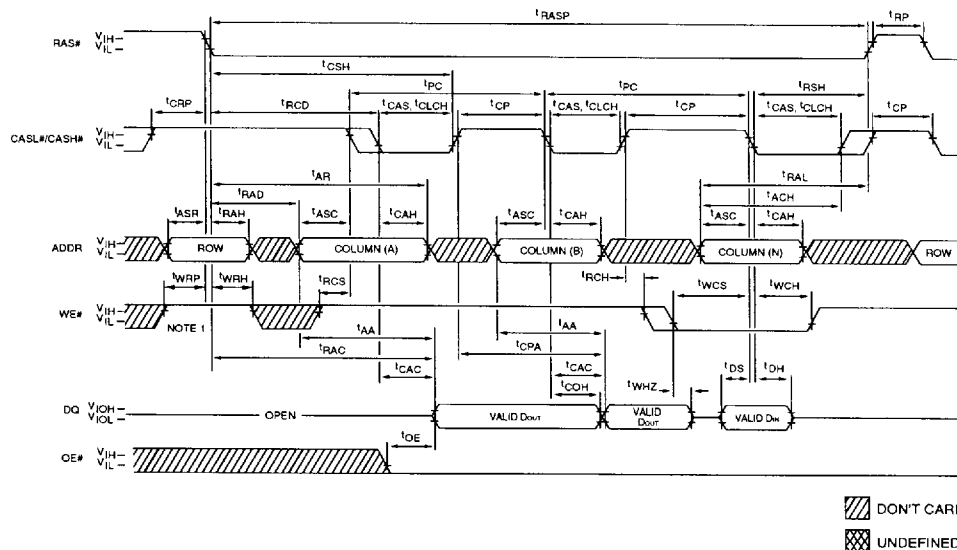
- NOTE:**
1. ¹PC is for LATE WRITE cycles only.
 2. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for ¹WRP and ¹WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
AA		30		35	ns
AR	45		50		ns
ASC	0		0		ns
ASR	0		0		ns
AWD	55		60		ns
CAC		15		20	ns
CAH	10		12		ns
CAS	12	10,000	13	10,000	ns
CLCH	10		10		ns
CLZ	0		0		ns
CP	10		10		ns
CPA		35		40	ns
CRP	5		5		ns
CSH	50		55		ns
CWD	35		40		ns
CWL	15		15		ns
DH	10		12		ns
DS	0		0		ns
OD	0	15	0	15	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
'OE		15		20	ns
'OEH	12		12		ns
'PC	25		30		ns
'PRWC	75		85		ns
'RAC		60		70	ns
'RAD	12	30	12	35	ns
'RAH	10		10		ns
'RAL	30		35		ns
'RASP	60	125,000	70	125,000	ns
'RCD	14	45	14	50	ns
'RCS	0		0		ns
'RP	40		50		ns
'RSH	13		15		ns
'RWD	80		90		ns
'RWL	15		15		ns
'WP	10		12		ns
'WRH	10		10		ns
'WRP	10		10		ns

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY-WRITE)



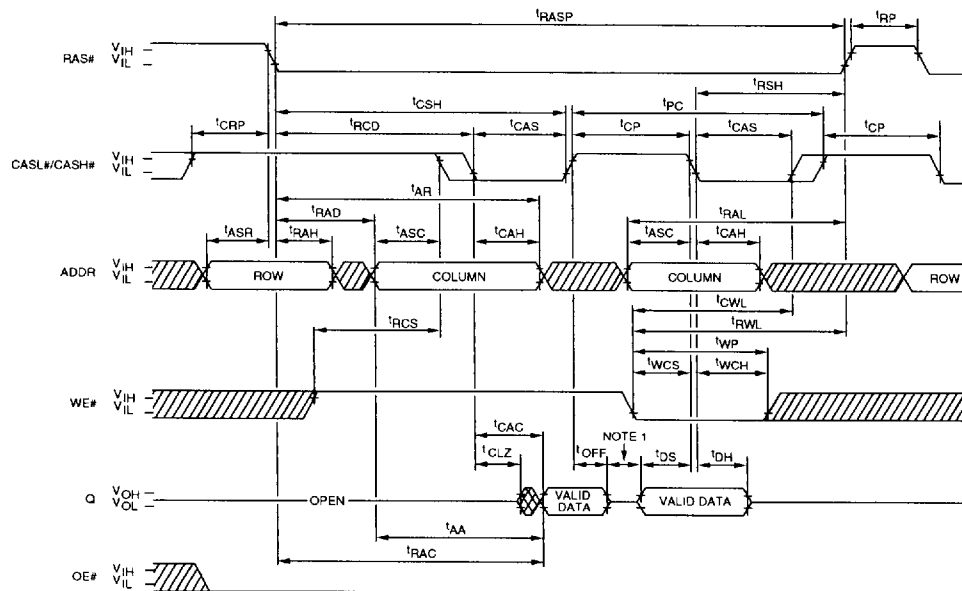
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for $\overline{\text{WRP}}$ and $\overline{\text{WRH}}$. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
1AA		30		35	ns
1ACH	15		15		ns
1AR	45		50		ns
1ASC	0		0		ns
1ASR	0		0		ns
1CAC		15		20	ns
1CAH	10		12		ns
1CAS	12	10,000	13	10,000	ns
1CLCH	10		10		ns
1COH	3		3		ns
1CP	10		10		ns
1CPA		35		40	ns
1CRP	5		5		ns
1CSH	50		55		ns
1DH	10		12		ns
1DS	0		0		ns
1OE		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ PC	25		30		ns
¹ RAC		60		70	ns
¹ RAD	12	30	12	35	ns
¹ RAH	10		10		ns
¹ RAL	30		35		ns
¹ RASP	60	125,000	70	125,000	ns
¹ RCD	14	45	14	50	ns
¹ RCH	0		0		ns
¹ RCS	0		0		ns
¹ RP	40		50		ns
¹ RSH	13		15		ns
¹ WCH	10		12		ns
¹ WCS	0		0		ns
¹ WHZ	0	13	0	15	ns
¹ WRH	10		10		ns
¹ WRP	10		10		ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY-WRITE)



 DON'T CARE

 UNDEFINED

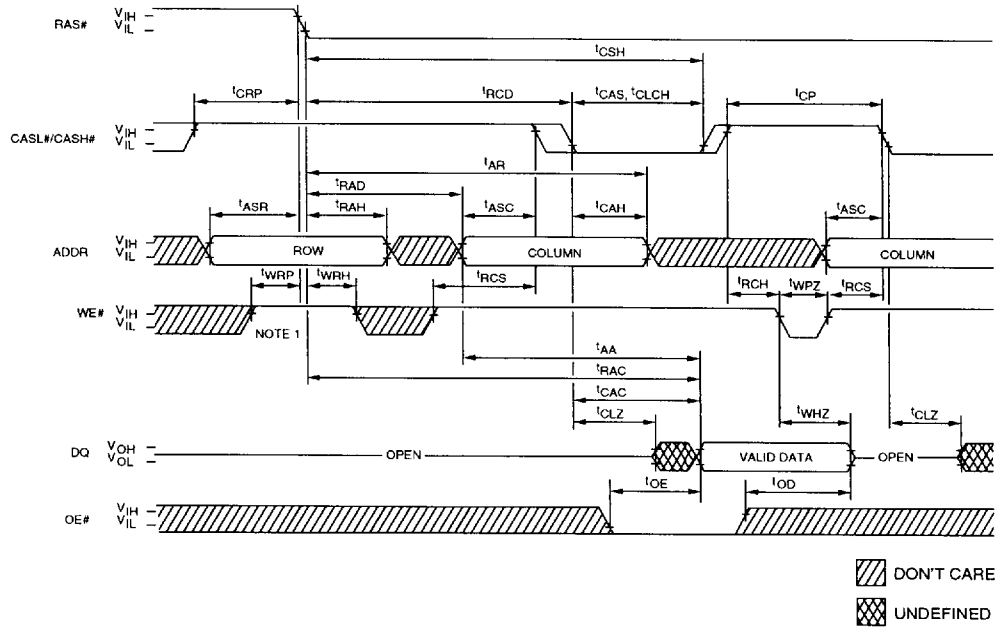
NOTE: 1. Do not drive data prior to tristate.

FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
AA		30		35	ns
AR	50		55		ns
ASC	0		0		ns
ASR	0		0		ns
CAC		15		20	ns
CAH	10		15		ns
CAS	15	10,000	20	10,000	ns
CLZ	3		3		ns
CP	10		10		ns
CRP	5		5		ns
CSH	60		70		ns
CWL	15		20		ns
DH	10		15		ns
DS	0		0		ns
OFF	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
'PC	35		40		ns
'RAC		60		70	ns
'RAD	15	30	15	35	ns
'RAH	10		10		ns
'RAL	30		35		ns
'RASP	60	100,000	70	100,000	ns
'RCD	20	45	20	50	ns
'RCS	0		0		ns
'RP	40		50		ns
'RSH	15		20		ns
'RWL	15		20		ns
'WCH	10		15		ns
'WCS	0		0		ns
'WP	10		15		ns

EDO READ CYCLE
(with WE#-controlled disable)



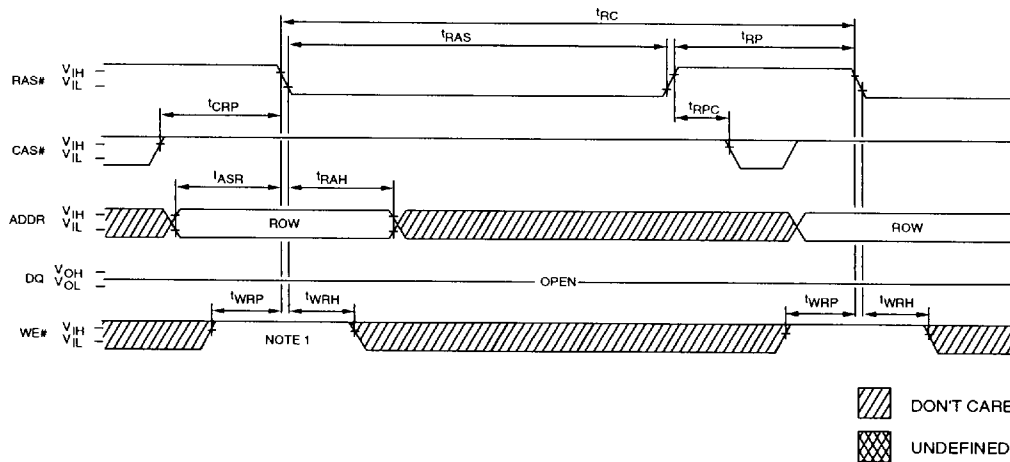
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE
TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		12		ns
tCAS	12	10,000	13	10,000	ns
tCLCH	10		10		ns
tCLZ	0		0		ns
tCP	10		10		ns
tCRP	5		5		ns
tCSH	50		55		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOD	0	15	0	15	ns
tOE		15		20	ns
tRAC		60		70	ns
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRCD	14	45	14	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ	0	13	0	15	ns
tWPZ	10		12		ns
tWRH	10		10		ns
tWRP	10		10		ns

RAS#-ONLY REFRESH CYCLE ²⁷



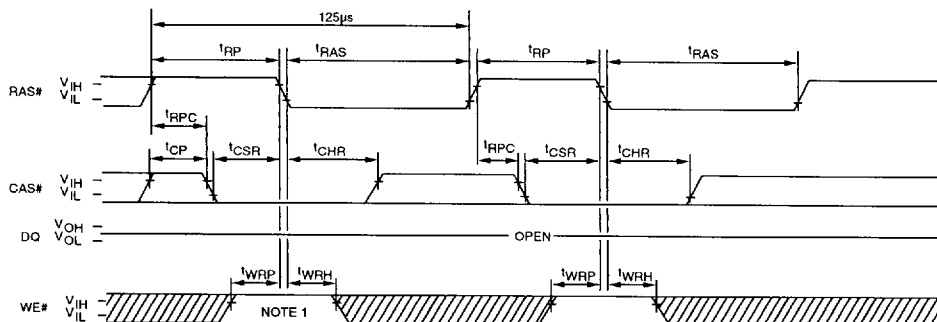
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for $t'WRP$ and $t'WRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

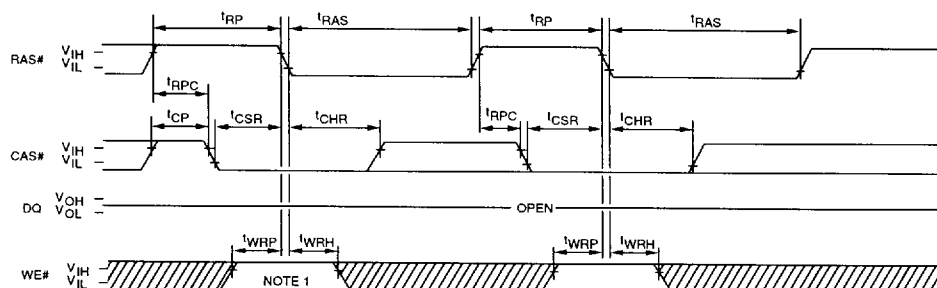
	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
$t'ASR$	0		0		ns
$t'CRP$	5		5		ns
$t'RAH$	10		10		ns
$t'RAS$	60	10,000	70	10,000	ns
$t'RC$	110		130		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
$t'RP$	40		50		ns
$t'RPC$ (FPM)	0		0		ns
$t'RPC$ (EDO)	5		5		ns
$t'WRH$	10		10		ns
$t'WRP$	10		10		ns

EXTENDED CBR REFRESH CYCLE 27, 29
(Addresses = DON'T CARE)



CBR REFRESH CYCLE 27
(Addresses = DON'T CARE)



▨ DON'T CARE
▩ UNDEFINED

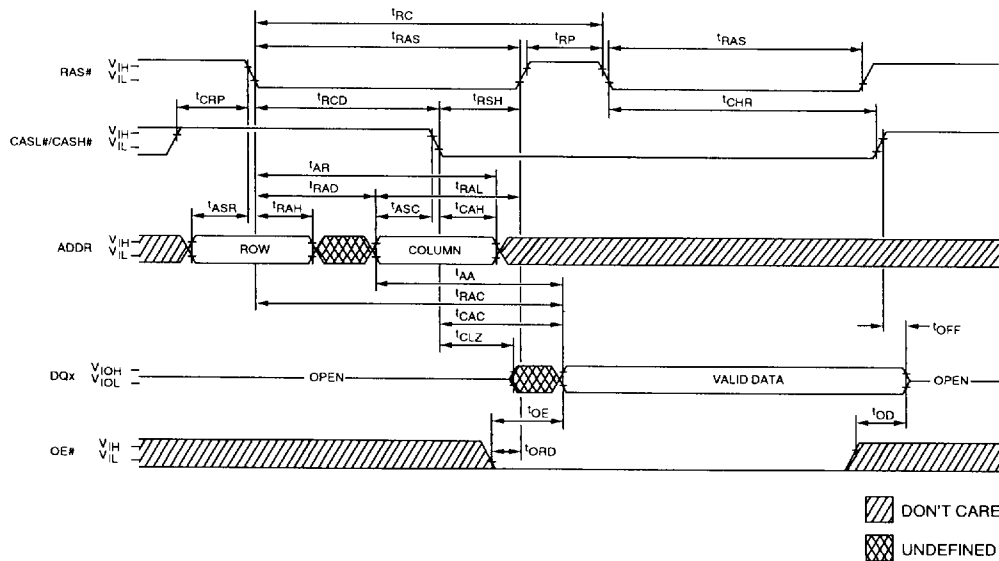
NOTE: 1. t_{WRP} and t_{WRH} are for system design reference only. The WE# signal is actually a "don't care" at RAS# time during a CBR REFRESH. However, WE# should be held HIGH at RAS# time during a CBR REFRESH to ensure compatibility with other DRAMs which require WE# HIGH at RAS# time during a CBR REFRESH.

FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t_{CHR}	15		15		ns
t_{CP}	10		10		ns
t_{CSR}	5		5		ns
t_{RAS}	60	10,000	70	10,000	ns
t_{RP}	40		50		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t_{RPC} (FPM)	0		0		ns
t_{RPC} (EDO)	5		5		ns
t_{WRH}	10		10		ns
t_{WRP}	10		10		ns

HIDDEN REFRESH CYCLE 22, 27
(WE# = HIGH)

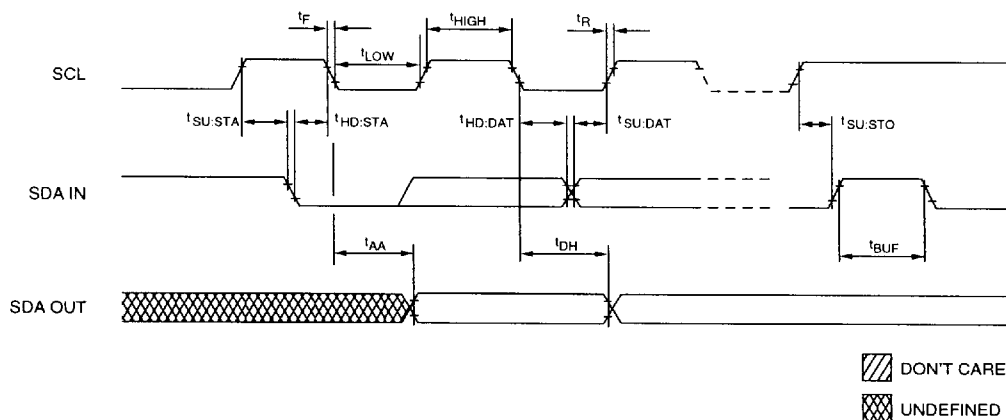


FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tAA		30		35	ns
tAR (FPM)	50		55		ns
tAR (EDO)	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH (FPM)	10		15		ns
tCAH (EDO)	10		12		ns
tCHR (FPM)	15		15		ns
tCHR (EDO)	10		12		ns
tCLZ (FPM)	3		3		ns
tCLZ (EDO)	0		0		ns
tCRP	5		5		ns
tOD	3	15	3	20	ns
tOE		15		20	ns
tOFF (FPM)	3	15	3	20	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tOFF (EDO)	3	15	3	15	ns
tORD	0		0		ns
tRAC		60		70	ns
tRAD (FPM)	15	30	15	35	ns
tRAD (EDO)	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC (FPM)	110		130		ns
tRC (EDO)	105		125		ns
tRCD (FPM)	20	45	20	50	ns
tRCD (EDO)	14	45	14	50	ns
tRP	40		50		ns
tRSH (FPM)	15		20		ns
tRSH (EDO)	10		12		ns

SPD EEPROM

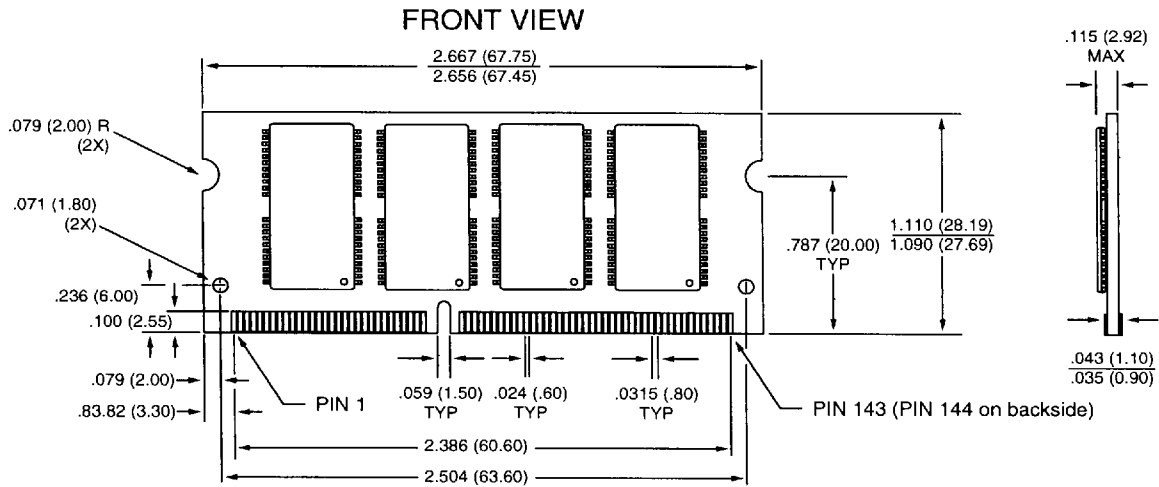


SERIAL PRESENCE-DETECT EEPROM
TIMING PARAMETERS

SYM	MIN	MAX	UNITS
t_{AA}	0.3	3.5	μ S
t_{BUF}	4.7		μ S
t_{DH}	300		ns
t_F		300	ns
$t_{HD:DAT}$	0		μ S
$t_{HD:STA}$	4		μ S
t_{HIGH}	4		μ S
t_I		100	ns

SYM	MIN	MAX	UNITS
t_{LOW}	4.7		μ S
t_R		1	μ S
f_{SCL}		100	KHz
$t_{SU:DAT}$	250		ns
$t_{SU:STA}$	4.7		μ S
$t_{SU:STO}$	4.7		μ S
t_{WR}		10	ms

144-Pin SO DIMM
(8 MB)



144-Pin SO DIMM
(16 MB)

