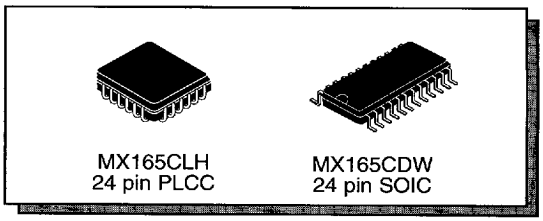
Advance Information

LOW VOLTAGE CTCSS ENCODER/DECODER
WITH TX/RX AUDIO FILTERS

FEATURES
- **MX•COM MiXed Signal CMOS**
- **47 CTCSS Tones + Notone**
- **TX/RX Audio Filters**
- **TX Tone Phase Reversals**
- **Serial or Parallel Programming**
- **Meets TIA/EIA-603 Land Mobile Standard***

BENEFITS
- **Scanning of any Channel**
- **Improved Sinad**
- **Squelch Tail Elimination**
- **Easy µP Interface**

APPLICATIONS
- **Mobile Radio Channel Sharing**
- **Wireless Intercom**
- **Serves 3-Cell Applications**



MX165CLH
24 pin PLCC

MX165CDW
24 pin SOIC

Description

Voice on shared radio channels is multiplexed with a subaudible CTCSS tone as a means of directing messages among user groups sharing the same RF frequency. Continuous Tone Controlled Sub-audible Squelch (CTCSS) modulates the transmitter with a discrete tone, taken from a field of 39 in the range of 67 to 250 Hz, according to TIA/EIA-603 Standard plus 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz. Groups of radio receivers, segregated by common interest and assigned tone, demodulate the voice/tone mixture for voice messages to be heard.

The MX165C CTCSS Encoder/Decoder enhances voice/tone multiplexing with an on-chip filter that attenuates TX speech 36dB at frequencies below 250Hz, while passing signals >300Hz with only ±1dB of ripple.

Early CTCSS designs did not filter TX speech, depending instead on the host transmitter's pre-emphasis network. At only 6dB/octave, their attenuation of speech components at the higher CTCSS tones was only a few dB, which resulted in "talk-off" (low frequency voice components unsquelching the receiver audio).

The MX165C features TX/RX selection and a LOAD/LATCH pin. A Notone program code has been included to permit scanning channels without CTCSS. A choice of serial or parallel tone programming is offered. Operation of the PTL signal during TX reverses the phase of the transmitted CTCSS tone by 180°. This is used in some radios to eliminate squelch tails.

The MX165C requires a single 3.75-volt supply and a 1 MHz clock or crystal.

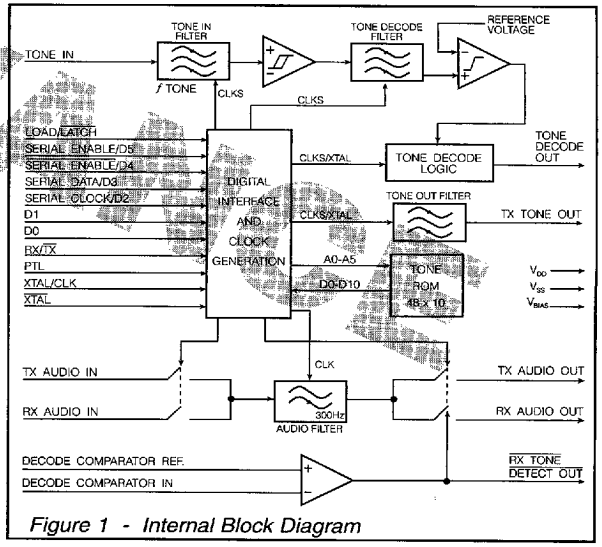


Figure 1 - Internal Block Diagram

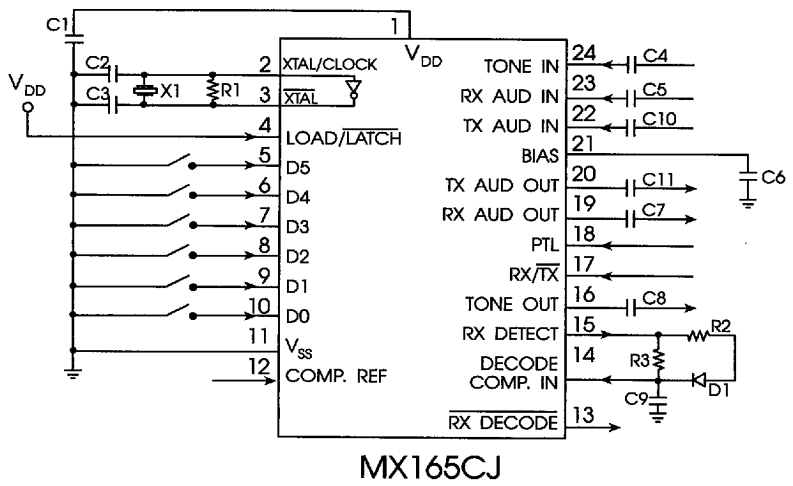
** The following tones are not specified in the TIA/EIA-603 Standard, and do not meet the Standard when used with their adjacent tones: 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz.*

PIN FUNCTION TABLE

Pin	Function
1	**V_{DD}:** Positive Supply.
2	**Xtal/Clock:** Input to the on-chip inverter used with a 1 MHz Xtal or external clock source.
3	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter (clock output).
4	**Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch RX/TX, PTL, and D0-D5. This pin is internally pulled to V_{DD}. A logic "1" applied to this input puts the 8 latches in "transparent" mode. A logic "0" applied to this input puts the 8 latches in the "latched" mode. In parallel mode data is loaded and latched by a logic 1-0 transition (see Fig. 3). In serial mode data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Fig. 4).
5	**D5/Serial Enable 1:** Data input D5 (in parallel mode). A logic "1" applied to this input together with a logic "0" applied to D4/Serial Enable 2 will put the device in serial mode (see Fig. 4). This pin is internally pulled to V_{DD}.
6	**D4/$\overline{\text{Serial Enable 2}}$:** Data input D4 (in parallel mode). A logic "0" applied to this input together with a logic "1" on pin 5 will place the device in serial mode (see Fig. 5). This pin is internally pulled to V_{DD}.
7	**D3/Serial Data Input:** Data input D3 (in parallel mode). In serial mode this pin becomes the serial data input for D5-D0, RX/TX and PTL (see Fig. 4). D5 is clocked first and PTL last. This pin is internally pulled to V_{DD}.
8	**D2/Serial Clock:** Data input D2 (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see Fig. 4). This pin is internally pulled to V_{DD}.
9	**D1:** Data input D1 (in parallel mode). This pin is internally pulled to V_{DD}.
10	**D0:** Data input D0 (in parallel mode). This pin is internally pulled to V_{DD}.
11	**V_{SS}:** Negative supply.
12	**Decode Comparator Ref.:** This pin is internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1M resistors depending on the logical state of the RX Tone Decode Out pin. RX Tone Decode Out = 1 will bias this input $2V_{DD}/3$; a logic "0" will bias this input $V_{DD}/3$. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce "chatter" under marginal conditions.
13	**$\overline{\text{RX Tone Decode Out}}$:** This is the gated output of the decode comparator. This output is used to gate the RX Audio path. A logic "0" on this pin indicates a successful decode and that the Decode Comparator Input pin is more positive than the Decode Comparator Ref. input (see Table 1).
14	**Decode Comparator Input:** This is the inverting input of the decode comparator. This pin is normally connected to the integrated output of the RX Tone Detect line.
15	**RX Tone Detect:** In RX mode this output will go to logic "1" during a successful decode. It must be externally integrated to control response and deresponse times (see Table 1).
16	**TX Tone Out:** The CTCSS sinewave output appears on this pin under control of the RX/$\overline{\text{TX}}$ pin. This pin, when not transmitting a tone, may be biased to V_{DD}-0.7V or O/C (see Table 1).

PIN FUNCTION TABLE

Pin	Function
17	**RX/$\overline{TX}$:** This input (in parallel mode) selects RX or TX modes (see Fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.
18	**PTL:** In parallel RX mode this pin operates as a "Push To Listen" function by enabling the RX audio path, thus overriding the tone squelch function. In parallel TX mode this pin reverses the phase of the transmitted CTCSS tone (used for squelch tail elimination). In serial mode this function is serially loaded (see Fig. 2).
19	**RX Audio Out:** This is the high pass filtered receive audio output pin. This pin outputs audio when RX Tone Decode = 0, or PTL = 1, or when Notone is programmed (see Table 2). In TX mode this pin is biased to $V_{DD}/2$.
20	**TX Audio Out:** This is the high pass filtered transmit audio output pin. In TX mode this pin outputs audio present at the TX Audio Input pin. In RX mode this pin is biased to $V_{DD}/2$.
21	**Bias:** This pin is the output of an internally generated $V_{DD}/2$ bias level and would normally be externally decoupled to V_{SS} via capacitor C7.
22	**TX Audio In:** This is the TX Audio input pin. In TX mode it may be prefiltered, using the TX audio path, thus helping to aviod talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. This pin is internally biased to $V_{DD}/2$.
23	**RX Audio In:** This is the input to the audio high pass filter in RX mode. It is internally biased to $V_{DD}/2$.
24	**Tone Input:** This is the input to the CTCSS tone detector. It is internally biased to $V_{DD}/2$.



Component	Values
R1	1MΩ
R2	560kΩ
R3	820kΩ
X1	1MHz
C1	0.1µF
C2	68pF
C3	33pF
C4	0.1µF
C5	0.1µF
C6	0.47µF
C7	0.1µF
C8	0.1µF
C9	0.1µF
C10	0.1µF
C11	0.1µF
D1	small signal

Tolerances: Resistors: ±10%
Capacitors: ±20%
Xtal: ±0.1%

Figure 2 - External Components

I/O CONDITIONS

	INPUT PIN CONDITION			OUTPUT PIN CONDITION		RESULT/FUNCTION					
D0-D5	RX/$\overline{TX}$	PTL	Decode Comp. Input	RX Tone Detect	$\overline{Tone}$ Decode	Tone Transmitter Enabled	TX Tone Phase Reversed	TX Audio Path Enabled	Tone Decoder Enabled	RX Audio Path Enabled	Notes
Tone	0	0	X	0	1	Yes	No	Yes	No	No (bias)	1a
Tone	0	1	X	0	1	Yes	Yes	Yes	No	No (bias)	1b
No tone	0	X	X	0	1	No (bias)	X	Yes	No	No (bias)	2
Tone	1	0	0	0	1	No (o/c)	X	No	Yes	No (bias)	3a
Tone	1	1	0	0	1	No (o/c)	X	No	Yes	Yes	3b
Tone	1	X	1	1	0	No (o/c)	X	No	Yes	Yes	4
No tone	1	X	X	X	0	No (o/c)	X	No	Yes	Yes	5

Table 1 - Combinations of Input/Output Conditions

o/c = open circuit
X = don't care

Notes:

1a. Normal tone transmit condition.
1b. Tone transmit with phase reversed.
2 Notone programmed in TX mode, tone transmit O/P set to $V_{DD}/2$. TX audio path enabled.
3a. Normal decode standby.
3b. Normal decode standby with PTL used to enable audio.
4. Normal decode of correct CTCSS tone condition, PTL has no effect.
5. Notone programmed in RX mode, tone transmit O/P (o/c). RX audio path enabled.

FILTER RESPONSE

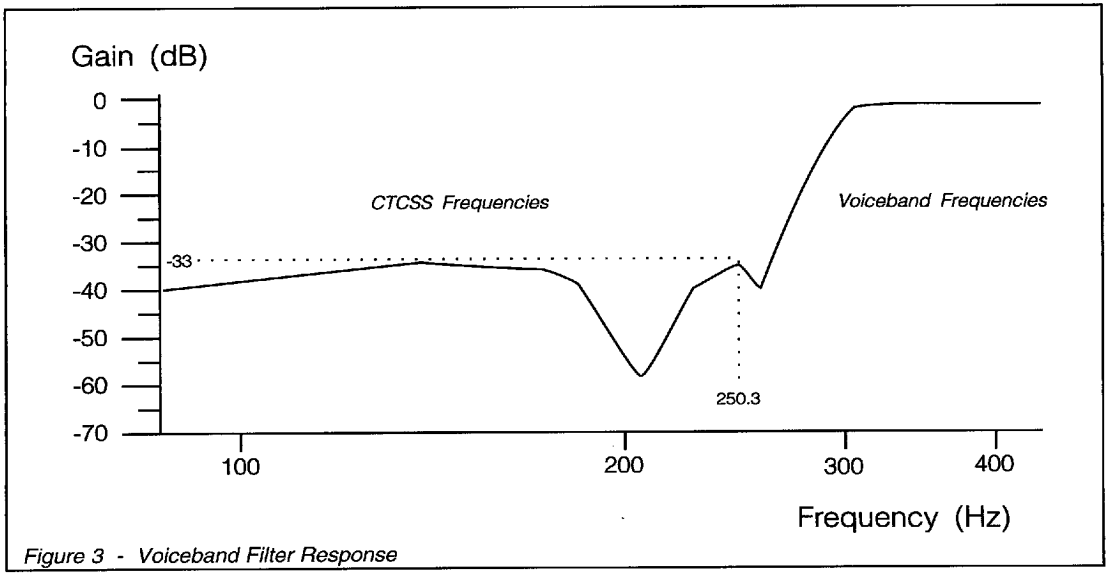
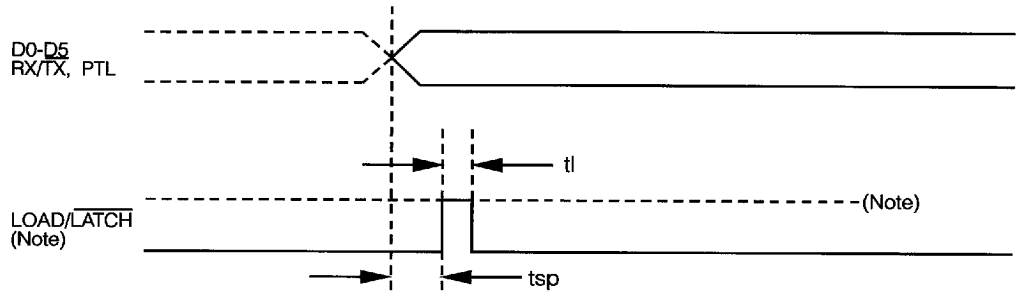


Figure 3 - Voiceband Filter Response

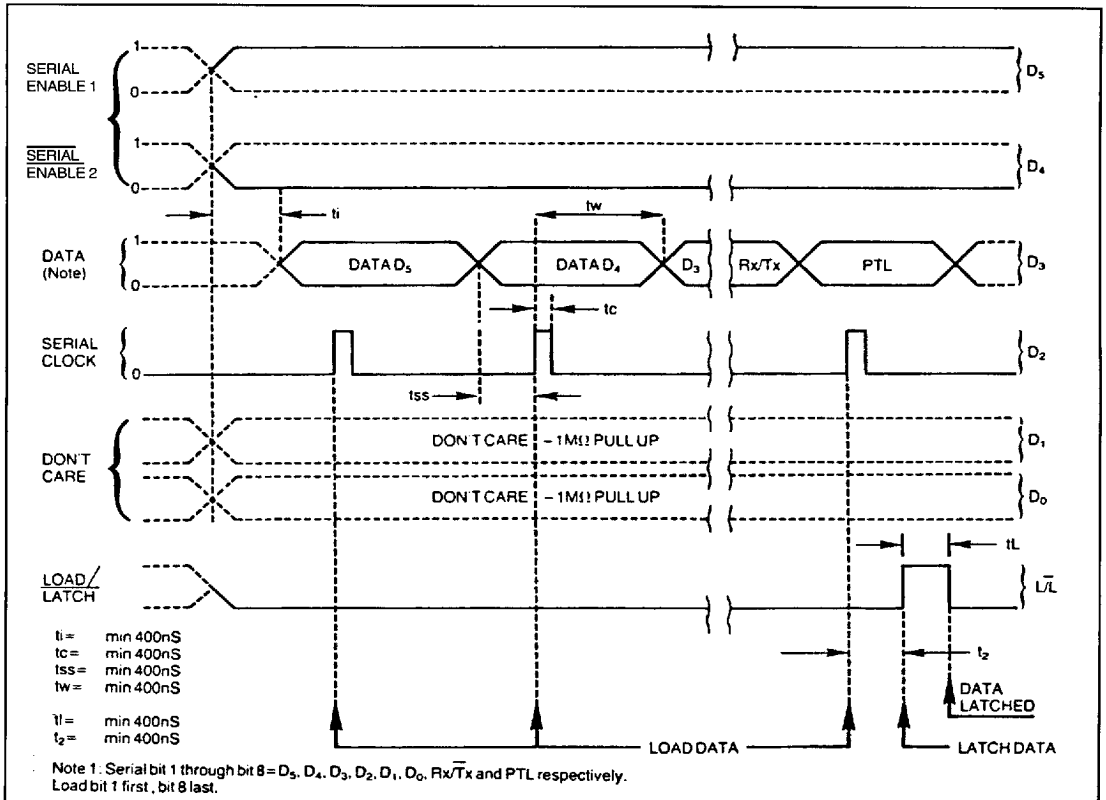
SERIAL AND PARALLEL MODE TIMING



Note: For wired, non microprocessor applications Load/Latch should be connected to V_{DD}.

tl min. = 400ns
tsp min. = 400ns

Figure 4 - Parallel Mode (not to scale)



Note 1: Serial bit 1 through bit 8 = D_5, D_4, D_3, D_2, D_1, D_0, Rx/$\overline{Tx}$ and PTL respectively.
Load bit 1 first, bit 8 last.

Figure 5 - Serial Mode (not to scale)

CTCSS PROGRAMMING TABLE

Tone			Programming Inputs						
TIA/EIA-603 Nominal Frequency (Hz)	MX165C Freq. (Hz)	Δf_0 (%)	D5	D4	D3	D2	D1	D0	Hex
67.0	66.98	-0.029	1	1	1	1	1	1	3F
69.3	69.32	0.024	1	1	1	0	0	1	39
71.9	71.901	0.001	0	1	1	1	1	1	1F
74.4	74.431	0.042	1	1	1	1	1	0	3E
77.0	76.965	-0.046	0	0	1	1	1	1	0F
79.7	79.677	-0.029	1	1	1	1	0	1	3D
82.5	82.483	-0.021	0	1	1	1	1	0	1E
85.4	85.383	-0.020	1	1	1	1	0	0	3C
88.5	88.494	-0.007	0	0	1	1	1	0	0E
91.5	91.456	-0.048	1	1	1	0	1	1	3B
94.8	94.76	-0.042	0	1	1	1	0	1	1D
97.4	97.435	-0.036	1	1	1	0	1	0	3A
100.0	99.96	-0.040	0	0	1	1	0	1	0D
103.5	103.429	-0.069	0	1	1	1	0	0	1C
107.2	107.147	-0.05	0	0	1	1	0	0	0C
110.9	110.954	0.049	0	1	1	0	1	1	1B
114.8	114.84	0.035	0	0	1	0	1	1	0B
118.8	118.793	-0.006	0	1	1	0	1	0	1A
123.0	123.028	0.023	0	0	1	0	1	0	0A
127.3	127.328	0.022	0	1	1	0	0	1	19
131.8	131.674	-0.095	0	0	1	0	0	1	09
136.5	136.612	0.082	0	1	1	0	0	0	18
141.3	141.323	0.016	0	0	1	0	0	0	08
146.2	146.044	-0.107	0	1	0	1	1	1	17
151.4	151.441	0.027	0	0	0	1	1	1	07
156.7	156.875	0.112	0	1	0	1	1	0	16
• 159.8	159.936	0.085	1	1	0	0	0	1	31
162.2	162.311	0.069	0	0	0	1	1	0	06
167.9	167.708	-0.114	0	1	0	1	0	1	15
173.8	173.936	0.078	0	0	0	1	0	1	05
179.9	179.654	-0.137	0	1	0	1	0	0	14
• 183.5	183.680	0.098	1	1	0	0	1	0	32
186.2	186.289	0.048	0	0	0	1	0	0	04
• 189.9	190.069	0.089	1	1	0	0	1	1	33
192.8	192.864	0.033	0	1	0	0	1	1	13
• 196.6	196.329	-0.138	1	1	0	1	0	0	34
• 199.5	199.312	-0.094	1	1	0	1	0	1	35
203.5	203.645	0.071	0	0	0	0	1	1	03
• 206.5	206.207	-0.142	1	1	0	1	1	0	36
210.7	210.848	0.070	0	1	0	0	1	0	12
218.1	217.853	-0.113	0	0	0	0	1	0	02
225.7	225.339	-0.160	0	1	0	0	0	1	11
• 229.1	229.279	0.078	1	1	0	1	1	1	37
233.6	233.359	-0.103	0	0	0	0	0	1	01
241.8	241.970	0.070	0	1	0	0	0	0	10
250.3	250.282	-0.007	0	0	0	0	0	0	00
• 254.1	254.162	0.024	1	1	1	0	0	0	38
Notone		N/A	1	1	0	0	0	0	30
Serial Input Mode		N/A	1	0	Data	Clock	X	X	2X

Table 2 - CTCSS Tones

•Not specified in the TIA/EIA-603 tone set, and does not meet the TIA/EIA-603 specification when used with their adjacent tones.

CTCSS Decode Performance

F_N (Hz)	Band Separation- (Hz)	F_A -1.23% (Hz)	F_A (Hz)	F_A +1.23% (Hz)	Band Separation+ (Hz)
67.000	NA	66.157	66.980	67.804	1.150
69.300	1.130	68.465	69.317	70.169	1.371
71.900	1.371	71.017	71.901	72.785	1.243
74.400	1.256	73.516	74.431	75.346	1.269
77.000	1.246	76.018	76.965	77.911	1.391
79.700	1.312	78.697	79.677	80.656	1.431
82.500	1.370	81.469	82.483	83.497	1.476
85.400	1.420	84.333	85.383	86.432	1.526
88.400	1.461	87.288	88.374	89.461	1.582
91.500	1.489	90.331	91.456	92.580	1.746
94.800	1.637	93.595	94.760	95.925	0.988
97.400	0.963	96.237	97.435	98.633	0.867
100.000	0.844	98.731	99.960	101.189	1.793
103.500	1.657	102.157	103.429	104.700	1.964
107.200	1.812	105.829	107.147	108.464	1.881
110.900	1.854	109.590	110.954	112.318	1.908
114.800	1.974	113.428	114.840	116.252	1.954
118.800	1.958	117.332	118.793	120.254	2.131
123.000	2.121	121.515	123.028	124.540	2.123
127.300	2.147	125.762	127.328	128.893	2.248
131.800	2.119	130.055	131.674	133.293	2.524
136.500	2.473	134.932	136.612	138.292	2.302
141.300	2.403	139.585	141.323	143.060	2.409
146.200	2.242	144.248	146.044	147.840	2.803
151.400	2.648	149.579	151.441	153.303	2.614
156.700	2.789	154.946	156.875	158.804	0.197
159.800	0.486	157.970	159.936	161.902	-0.513
162.200	-0.283	160.316	162.311	164.307	2.754
167.900	2.635	165.646	167.708	169.770	3.161
173.800	3.058	171.797	173.936	176.074	2.926
179.900	2.776	177.445	179.654	181.863	0.719
183.500	0.622	181.422	183.680	185.938	-0.669
186.200	-0.419	183.999	186.289	188.580	0.371
189.900	0.601	187.732	190.069	192.406	-0.570
192.800	-0.357	190.493	192.864	195.235	0.382
196.600	0.151	193.915	196.329	198.743	-0.240
199.500	-0.721	196.862	199.312	201.763	0.720
203.500	0.644	201.141	203.645	206.149	-0.682
206.500	-0.846	203.671	206.207	208.742	0.904
210.700	0.723	208.256	210.848	213.441	3.569
218.100	3.421	215.175	217.853	220.532	4.040
225.700	3.378	222.569	225.339	228.110	-0.155
229.100	-0.369	226.460	229.279	232.098	0.334
233.600	0.244	230.489	233.359	236.228	4.363
241.800	4.227	238.995	241.970	244.945	4.104
250.300	4.195	247.204	250.282	253.359	-0.529
254.100	-0.515	251.037	254.162	257.287	NA

Band Separation- = $DB_L[i] - 1.005*F_N[i-1]$
Band Separation+ = $0.995*F_N[i+1] - DB_H[i]$

Table 3 - CTCSS Decode Performance for the MX165C

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V
V_{SS} = 0V
T_{AMB}=25°C
Xtal/Clock f_0 = 1.0 MHz
0dB ref. = 300mVrms @ 1kHz

Composite signal: 300 mVrms 1kHz test tone, 75 mVrms noise (band limited 6kHz gaussian white noise), 30 mVrms CTCSS tone.

2

Characteristics	See Note	Min.	Typ.	Max.	TIA/EIA -603	Unit
STATIC VALUES						
Supply Voltage		2.75	3.75/5.0	5.5	-	V
Supply Current						
TX		-	3.0	-	-	mA
RX		-	3.0	-	-	mA
RX Monitor		-	2.0	-	-	mA
Tone Input Impedance		-	1	-	-	MΩ
Tone Output Impedance		-	1	-	-	kΩ
RX and TX Audio Input Impedance		-	1	-	-	MΩ
RX and TX Audio Output Impedance		-	1	-	-	kΩ
Digital Input Impedance	1	-	1	-	-	MΩ
Input logic"1"	1	70%V_{DD}	-	-	-	V
Input logic "0"	1	-	-	30%V_{DD}	-	V
Logic "1" output 1' source = 0.1mA	2	80%V_{DD}	-	-	-	V
Logic "0" output 1' sink = 0.1mA	2	-	-	20%V_{DD}	-	V
DYNAMIC VALUES						
Decoder						
Decode Input Signal Level	3	30	-	436	-	mVrms
Decode Response Time	3,6,7,10	-	-	250	250	ms
Deresponse Time	3,6,7,10	-	180	250	250	ms
Decode Selectivity						
Upper Decode Band Edge	3,11	1.005 F_i	-	.995 F_{i+1}	±0.5%f_i	Hz
Lower Decode Band Edge	3,11	1.005 F_{i-1}	-	.995 F_i	±0.5%f_i	Hz
Encoder						
Tone Output Level (relative to 775 mVrms)		548	775	-	-	mVrms
Tone Frequency Accuracy (f error)		-0.3	-	+0.3	-	%f_0
Risetime to 90% nominal O/P:						
f_0>100Hz	4,10	-	15	75	150	ms
f_0<100Hz	4,10	-	45	120	150	ms
Total Harmonic Distortion		-	2	5	-	%
Output Level Variation Between Tones	11	-1.0	-	+1.0	-	dB

Characteristics	See Note	Min.	Typ.	Max.	TIA/EIA -603	Unit
Audio Filter						
Total Harmonic Distortion	5,10	-	2	5	-	%
Output Noise Level	8	-	2	-	-	mVrms
(input a.c. short circuit, audio switch enabled)						
Sinad	9	36	40	-	-	dB
Spurious Emissions		-	-	-48	-	dB
Cutoff Frequency		-	300	-	-	Hz
Passband		300	-	3000	-	Hz
Bandpass Ripple	5	-1	-	+1	-	dB
Stopband Attenuation <250Hz	5	33	36	-	-	dB
Passband Gain 1kHz		-	0	-	-	dB
Audio Switch						
Isolation	9	-	60	-	-	dB
Serial/Parallel Inputs (See Figures 3 &4)						
Parallel Set-up Time t_{SP}		400	-	-	-	ns
Load/Latch Pulse Width t_l		400	-	-	-	ns
Serial Clock Pulse Width t_c		400	-	-	-	ns
Serial Set-up Time t_{ss}		400	-	-	-	ns
Serial Clock Frequency		-	1	-	-	MHz

NOTES:
1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite Signal Test Condition.
4. Any programming tone and RL = 10kΩ, CL = 15pF. This includes response to a phase reversal instruction.
5. 1kHz references = 0dB.
6. f_0>100Hz (for 100 Hz>f_0>67Hz: t=100/f_0Hz x 250ms)
7. See Figure 3.
8. Measured in a 30kHz bandwidth referenced to 300 mV.
9. Measured with an input level of 300 mV @ 1kHz, in a 30 kHz bandwidth.
10. Per TIA/EIA-603.
11. Only for the F_i in TIA/EIA-603, where F_i is the program tone.