MX16C451E

PARALLEL/ASYNCHRONOUS COMMUNICATIONS ELEMENT

DESCRIPTION

The MX16C451E is an universal synchronous receiver and transmitter with a bidirectional CENTRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56KHz. The MX16C451E fabricated in an advanced 2μ CMOS process to achieve low power drain and high speed requirements.

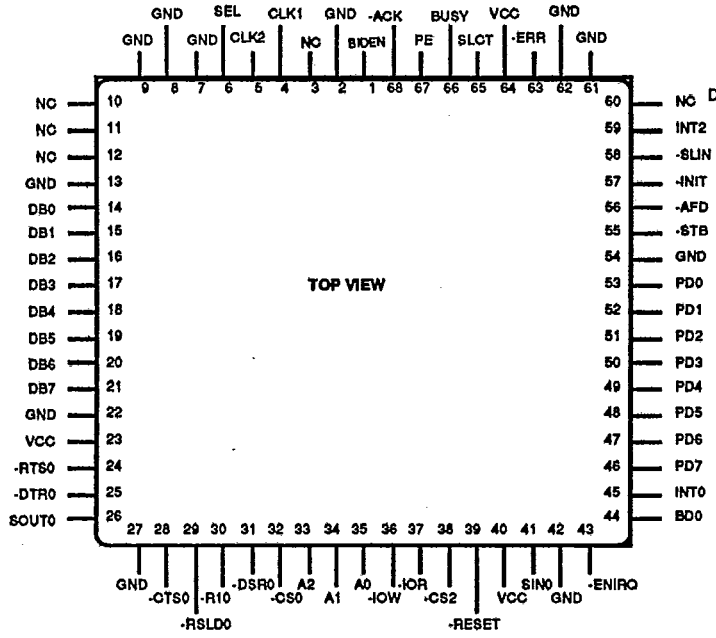
The MX16C451E is an improved version of the VL16C451 with higher speed operating access time. The MX16C451E performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The MX16C451E also provides the user with a fully bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on board status of the transfer operations being performed. The MX16C451E also has complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The MX16C451E can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

FEATURES

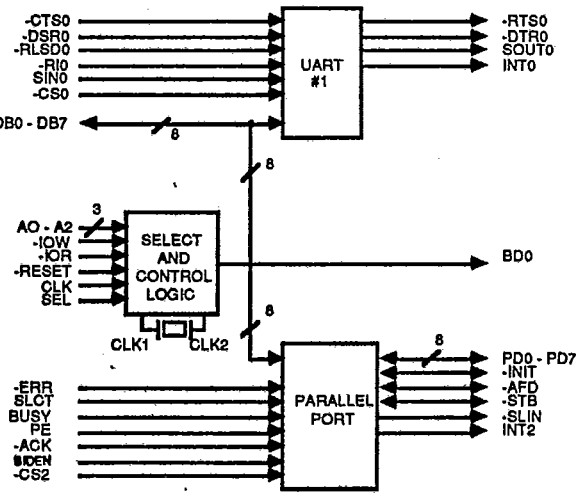
- Pin-to-pin and functionally compatible to VL16C451
- Bidirectional printer port
- Modem control signals (CTS-,RIS-,DSR-,DIR-,RI-, CD-)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Direct replacement of logic for PC/XT/AT
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Fully compatible with all new bidirectional PS/2 printer port
- High Data transfer rate

PIN DIAGRAM

MX16C451E



BLOCK DIAGRAM



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SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
-IOR	37	Input/Output Read Strobe: This is an active low input which causes the serial channel to output data to the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0, A1, A2. Chip select 0 (-CS0) selects UART and chip select 2 (-CS2) selects the line printer port.
-IOW	36	Input/Output Write Strobe: This is an active low input which causes data from the data bus (DB0-DB7) to be input to either UART or to the parallel port. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs (-CS0 and -CS2) enable the UART and the parallel port (respectively).
DB0-DB7	14-21	Data Bits DB0-DB7: The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the MX16C451E and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0,A1,A2	35,34,33	Address Lines A0-A2: The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels. Table 11 for the decode of the parallel line printer port.
CLK1	4	Crystal input 1 or external clock input. A crystal can be connected to this pin and CLK2 pin to utilize the internal oscillator circuit. An external clock can be used to clock the internal circuit and the baud rate generator for custom transmission rates.
CLK2	5	Crystal input 2. This pin should be tied to ground when the external clock is used.
SEL	6	Crystal or external clock select pin. To select external clock source to the MX16C451E CLK1 input, this pin should be tied to GND. On board crystal oscillator circuit can be activated by tieing this pin to VCC and connecting a crystal to CLK1 and CLK2 input pins.
SOUT0	26	Serial Data Output: This line is the serial data outputs from the UART's transmitter circuitry. A mark(1) is a logic "one" (high) and space(0) is a logic "zero" (low). SOUT0 is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
-CTS01	28	Clear to Send Inputs: The logical state of the -CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR(4)] of the UART. A change of stateof the -CTS pin, since the previous reading of the MSR causes the setting of DCTS [MSR(0)] of each Modem Status Register. When a -CTS pin is active (low), the modem is indicating that data on the associated SOUT0 can be transmitted.
DSR0	31	Data Set Ready Inputs: The logical state of the DSR0 pin is reflected in MSR(5) of the Modem Status Register. DDSR[MSR(1)] indicates whether the DSR0 pin has changed state since the previous reading of the MSR. When a DSR0 pin is low,the modem is indicating that it is ready to exchange data with the UART.
DTR0	25	Data Terminal Ready Output: The DTR0 pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 ofthe UART. This signal is cleared (high) by writing a logic 0 to the DTR bit [MCR(0)] or whenever a reset occurs. When active (low), the DTR0 pin indicates to the DCE the UART is ready to receive data.

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SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
-RTS0	24	Request to Send Outputs: The -RTS0 signal is an output on the UART used to enable the modem. The -RTS0 pin is set low by writing a logic 1 to MCR(1) bit 1 of the UART's Modem Control Register. The -RTS0 pin is reset high by Reset. A low on the -RTS0 indicates to the DCE thatthe UART has data ready to transmit. In half duplex operations, -RTS0 is used to control the direction of the line.
-RI0	30	Ring Indicator Input: When low, -RI0 indicates that a telephone ringing signal has been received by the modem or data set. The -RI signal is a modem control input whose condition is tested by reading MSR(6) (RI) of the UART. The Modem Status Register output TERI[MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER(3) = 1] and -RI0 changes from a high to low, an interrupt is generated.
BIDEN	1	I/O direction select. A high enables the software controlled mode (input/output). A low puts the parallel port in the output mode.
SIN0	41	Serial Data Input: The serial data inputs moves information from the communication line or modem to the MX16C451E receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
-RLSD0	29	Receive Line Signal Detect: When active(low), -RLSD output indicates that the data carrier has been detected by the modem or data set. -RLSD is a modem input whose condition can be tested by the CPU by reading MSR(7) (RLSD) of the Modem Status Registers. MSR(3) (DRLSD) of the Modem Status Register indicates whether the -RLSD input has changed since the previous reading of the MSR. -RLSD has no effect on the receiver. If the -RLSD changes state with the modem status interrupt enabled, an interrupt occur.
-RESET	39	Reset: When low, the reset input forces the MX16C451E into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its outputs is cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
-ENIRQ	43	Interrupt source selection (active low). The External ACK-can be selected as an interrupt source by tieing this pin to GND. Tieing this pin to VCC, will set the internal interrupt logic to latched state, reading the STATUS register will reset the INT2 output.
INT0	45	Serial Channel Interrupt Output: This three-state output is enabled by the MCR bit 2. The serial channel interrupt goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of the serial channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset operation.
-CS0,-CS2	32,38	Chip Selects: Each Chip Select input acts as an enable for the write and read signals for its channel. -CS2 enables the serial port, while -CS2 enables the signals to the line printer port.

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SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
BDO	44	Bus Buffer Output: This active high output is asserted when this serial channel or the parallel port is read. This output can be used to control the system bus driver device (74LS245).
PD0-PD7	53-46	Parallel Data Bits (0-7): These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when -LPTOE is held in the high state.
-STB	55	Line Printer Strobe: This open-drain line provides communication between the MX16C451E and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
-AFD	56	Line Printer Autofeed: This open-drain line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer. Line Printer Initialize: This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started.
-INIT	57	Line Printer Initialize: This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started.
-SLIN	58	Line Printer Select: This open-drain line selects the printer when it is active low.
INT2	59	Interrupt Printer Port: This signal is an active high, three-state output, generated by the positive transition of -ACK. It is enabled by bit 4 of the Write Control Register.
-ERROR	63	Line Printer Error: This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition.
SLCT	65	Line Printer Selected: This is an input line from the line printer that goes high when the line printer has been selected.
BUSY	66	Line Printer Busy: This is an input line from the line printer that goes high when the line printer is not ready to accept data.
PE	67	Line Printer Paper Empty: This is an input line from the line printer that goes high when the printer runs out of paper.
-ACK	68	Line Printer Acknowledge: This input goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
VCC	3,23,40,64	Power Suply: The power supply requirement is 5 V ±5%.
GND	2,5-9,13,22, 27,42,43,54, 61,62	Ground (0 V): All pins must be tied to ground for proper operation.

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FUNCTIONAL DESCRIPTION:

SERIAL CHANNEL REGISTERS

Three types of internal registers are used in the serial channel of the MX16C451E. They are used in the operations of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The MX16C451E data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion.

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below.

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LCR(3) Parity Enable (PEN)
LCR(4) Even Parity Select (EPS)
LCR(5) Stick Parity
LCR(6) Set Break
LCR(7) Divisor Latch Access Bit (DLAB)

LCR(0) and LCR(1) word length select bit 1: The number of bits in each serial character is programmed as shown in the following chart:

LCR(1)	LCR(0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selectrf, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled (LCR(3)-1), CLR(5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by

TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" 0 = Logic Low 1 = Logic High
Note: The serial channel is accessed when -CS0 is low.

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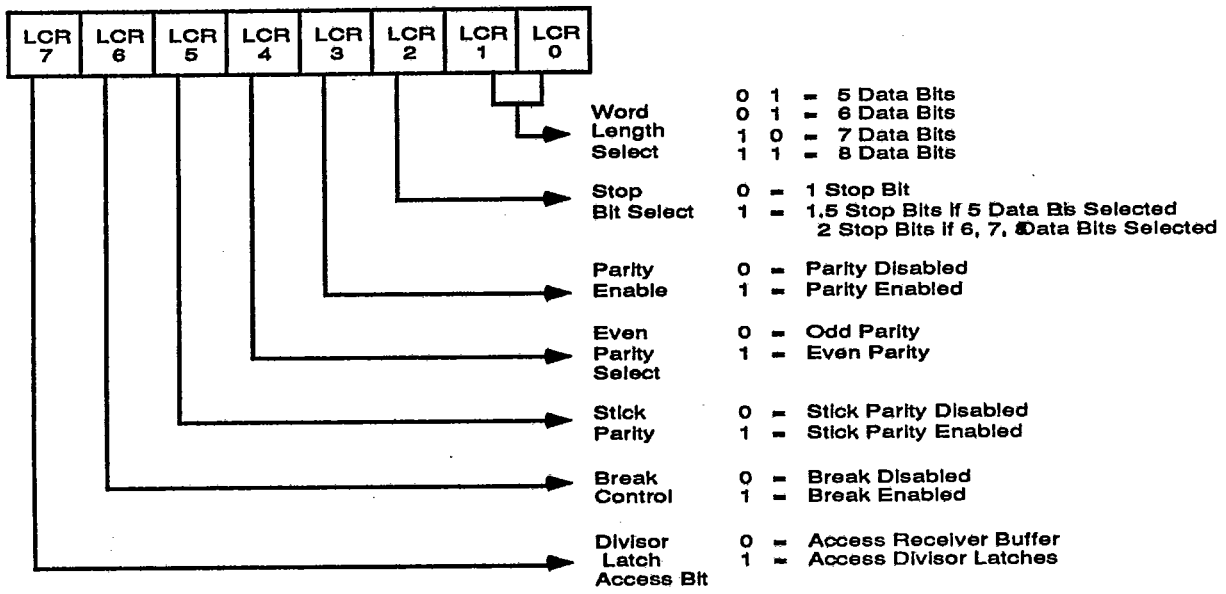
FIGURE 1. LINE CONTROL REGISTER



setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1), and clear break when normal transmission has to be restored.

LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel of the MX16C451E.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER(1)], an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR(1)-LSR(4). (OE, PE, FE, and BI.)

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TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	Logic 1	Logic 0
LSR(0) Data Ready (DR)	Ready	Not Ready
LSR(1) Overrun Error (OE)	Error	No Error
LSR(2) Parity Error (PE)	Error	No Error
LSR(3) Framing Error (FE)	Error	No Error
LSR(4) Break Interrupt (BI)	Break	No Break
LSR(5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR(6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR(7) Not Used		

The contents of the Line Status Register shown in Table 2 are described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR(4)). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2) = 1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the MX82C50A is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER(1) = 1). THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmiter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3. The MCR can be written and read. The -RTS and -DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0, 1, 3, and 4 are shown below:

MCR(0): When MCR(0) is set high, the -DTR output is forced low. When MCR(0) is reset low, the -DTR output is forced high. The -DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

TABLE 3. MODEM CONTROL REGISTER BITS

MCR BITS	Logic 1	Logic 0
MCR(0) Data Terminal Ready (DTR)	-DTR Output Low	-DTR Output High
MCR(1) Request to Send (RTS)	-RTS Output Low	-RTS Output High
MCR(2) 0		
MCR(3) Interupt (INT) Enable	INT Enabled	INT Disabled
MCR(4) Loop	Loop Enabled	Loop Disabled
MCR(5) 0		
MCR(6) 0		
MCR(7) 0		

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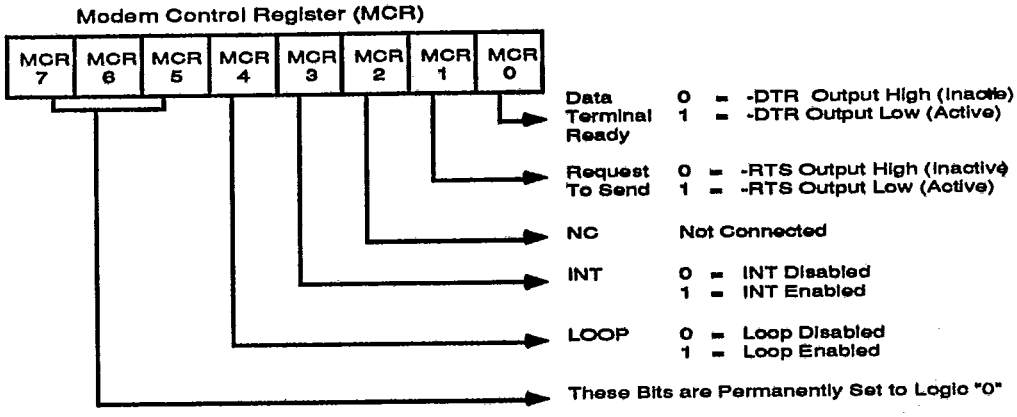
FIGURE 2. MODEM CONTROL REGISTER



MCR(1): When MCR(1) is set high, the RTS output is forced low. When MCR(1) is reset low, the -RTS output is forced high. The -RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(3): When MCR(3) is set high, the INT output is enabled.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs (-CTS, -DSR, and -RI) are disconnected. The modem control outputs (-DTR and -RTS) are internally connected to the four modem control inputs. The modem control pins are forced to their active state (high).

In the Diagnostic mode, data transmitted is immediately received. This allow the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR(5) - MCR(7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read each of the serial channel modem signal inputs by accessing the data bus interface of the MX16C451E. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are -CTS, -DSR, -RI, and -RLSD. MSR(4) - MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR(0) Delta Clear Send (DCTS): DCTS indicates that the -CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the -DSR input to the serial channel has changed state since the last time it was read by the CPU.

TABLE 4. MODEM STATUS REGISTER BITS

MSR BITS	Mnemonic	Description
MSR(1)	DDSR	Delta Data Set Ready
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(0)	DCTS	Delta Clear to Send
MSR(3)	DRLSD	Delta Data Carrier Detect
MSR(4)	-CTS	Clear to Send
MSR(5)	-DSR	Data Set Ready
MSR(6)	-RI	Ring Indicator
MSR(7)	-RLSD	Receiver Line Signal Detect

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MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the -RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on -RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the -RSLD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the -CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in loop mode [MSR(4) = 1], MSR(4) is equivalent to -RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the -DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR(4) = 1], MSR(5) is equivalent to DTR in the MCR.

MSR(6) Ring Indicator: Indicates the status of the RI input (pin 39). If the channel is in the loop mode [MCR(4) = 1], MSR(6) is not connected in the MCR.

MSR(7) Receive Line Signal Detect: Recieve Line Signal Detect indicates the status of the Receive Line Signal Detect (-RLSD) input. If the channel is in the loop mode [MCR(4) - 1], MSR(4) is equivalent to OUT2 of the MCR.

The modem status inputs (-RI, -RLSD, -DSR, and -CTS) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DRLSD are true, and a state change occurs during a read operation (-DISTR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read -DISTR operations. If a status condition is generated during a read -DISTR operation, the status bit is not set until the trailing edge of the read -DISTR.

If a status bit is set during a read -DISTR operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read -DISTR instead of being set again.

Each MX16C451E serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2 to the power of 16 - 1 (see also BRG description). The output frequency of the Baud Generator is 16x the data rate [divisor # = clock + (baud rate x 16)] .
Two 8-bit divisor latch registers store the divisor in a 16-bit binary format. These Divisor Latch register must be loaded during initialization. Upon loading either of the Divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in each serial channel of the MX16C451E is programmable for 5, 6, 7, or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the low of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7:

RBR(0)	Data Bit 0
RBR(1)	Data Bit 1
RBR(2)	Data Bit 2
RBR(3)	Data Bit 3
RBR(4)	Data Bit 4
RBR(5)	Data Bit 5
RBR(6)	Data Bit 6
RBR(7)	Data Bit 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflect the staus of the THR. The TEMT flag [LSR(5)] indicates if both the THR and TSR are empty.

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THR Bits 0 thru 7

THR(0)	Data Bit 0
THR(1)	Data Bit 1
THR(2)	Data Bit 2
THR(3)	Data Bit 3
THR(4)	Data Bit 4
THR(5)	Data Bit 5
THR(6)	Data Bit 6
THR(7)	Data Bit 7

Scratchpad Register is an 8-bit Read/Write register that has no effect on any channel in the MX16C451E. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR(0)	Data Bit 0
SCR(1)	Data Bit 1
SCR(2)	Data Bit 2
SCR(3)	Data Bit 3
SCR(4)	Data Bit 4
SCR(5)	Data Bit 5
SCR(6)	Data Bit 6
SCR(7)	Data Bit 7

TABLE 5. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the interrupt Source or THR Write
0	0	0	Fourth	Modem Status	-CTS, -DSR -RI, -RSLD	MSR Read

X = Not Defined

FIGURE 3. INTERRUPT CONTROL LOGIC

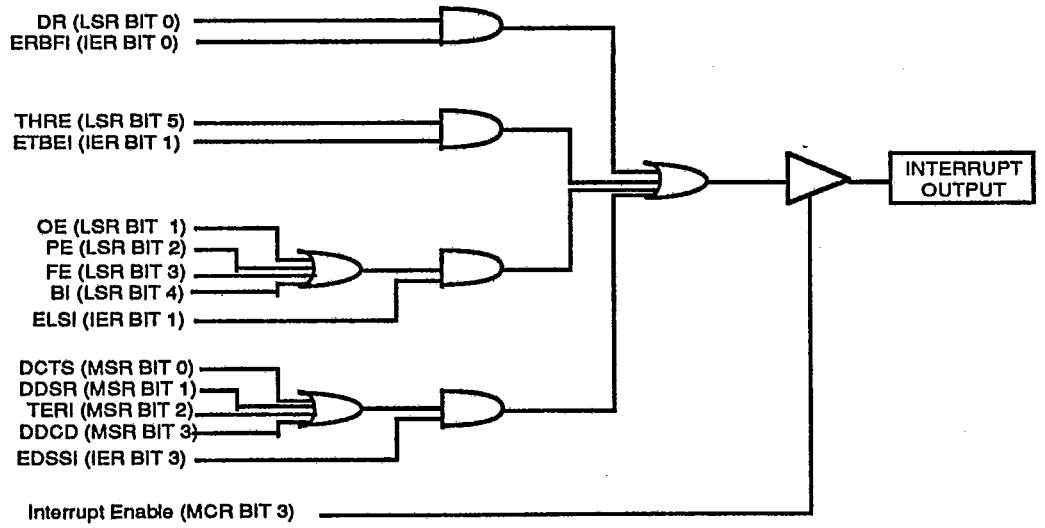

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TABLE 6. SERIAL CHANNEL ACCESSIBLE REGISTERS

	Register Bit Number							
Register Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TE MT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received

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INTERRUPTS

The Interrupt Identification Register (IIR) in the serial channel of the MX16C451E has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR(0): IIR(0) can be used in either as hard-wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write register used to independently enable the four serial channel interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 3 and are described below.

IER(0): When programmed high [IER(0) = Logic 1], IER(0) enables Received Data Available interrupt.

IER(1): When programmed high [IER(1) = Logic 1], IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When programmed high [IER(2) = Logic 1], IER(2) enables Receiver Line Status interrupt.

IER(3): When programmed high [IER(3) = Logic 1], IER(3) enables the Modem Status interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

TRANSMITTER

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5- to 8-bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, both THRE and TEMT are high. The first word written causes THRE to be reset to 0. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

RECEIVER

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status information for the receiver is provided in the Line Status Register to the Receiver Buffer Register , the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR(2). There is circuitry

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which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is symmetrical square wave, the center of the data cells will occur within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

BAUD RATE GENERATOR (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divison Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Tables 7, 8, and 9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

RESET

After power up, the MX16C451E-Reset input (MR) should be held low for 500 ns to reset the MX16C451E circuits to an idle mode until initialization. A low on –Reset causes the following:

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (Reset high), the MX16C451E remains in the idle mode until programmed.

A hardware reset of the MX16C451E sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interupt occurs due to THRE.

A summary of the effect of a reset on the MX16C451E is given in Table 10.

PROGRAMMING

Each serial channel of the MX16C451E is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

TABLE 7. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the MX16C451E serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

CLOCK INPUT OPERATION

The maximum input frequency of the external clock of the MX16C451Eis 3.1 MHz.

TABLE 8. BAUD RATES (2.4576 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

TABLE 9. BAUD RATES (3.072 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

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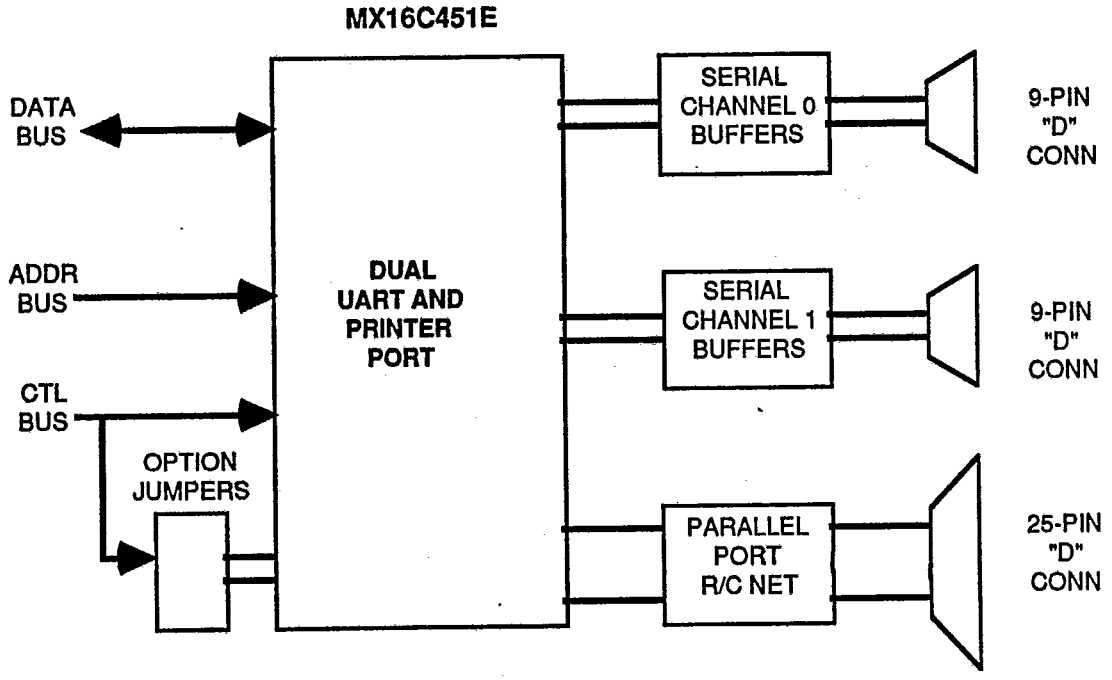
TABLE 10. RESET

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 are Permanently Low
Line Control Register	Reset	All Bits Low
MODEM Control Register	Reset	All Bits Low
Line Status Register	Reset	All Bits Low, Except Bits 5 and 6 High
MODEM Status Register	Reset	Bits 0-3 Low Bits 4-7 Input Signal
SOUT	Reset	High
Intrpt (RCVR Errs)	Read LSR/Reset	Low
Intrpt (RCVR Data Ready)	Read RBR/Reset	Low
Intrpt (THRE)	Read IIR/Write THR/Reset	Low
Intrpt (Modem Status Changes)	Read MSR/Reset	Low
-Out2	Reset	High
-RTS	Reset	High
-DTR	Reset	High
-Out1	Reset	High

DEVICE APPLICATION



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FUNCTIONAL DESCRIPTION:

PARALLEL PORT REGISTERS

The MX16C451E's parallel port interfaces the device to a Centronics-style printer. When Chip Select 2 (-CS2) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (-IOR) and write (-IOW) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus.

The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (-BUSY), Acknowledge (-ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (-ERROR). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines.

They are Interrupt Enable (IRQ ENB), Select In (SLIN), Initialize the Printer (INIT), Autofeed the Paper (AUTOFD), Strobe (STROBE), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

TABLE 11. PARALLEL PORT REGISTERS

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	-BUSY	-ACK	PE	SLCT	-ERROR	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	-INIT	AUTOFD	STROBE
Write Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	-INIT	AUTOFD	STROBE

TABLE 12. PARALLEL PORT REGISTER SELECT

Control Pins					Register Selected
-IOR	-IOW	-CS	A1	A0	
0	1	0	0	0	Read Data
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

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AC CHARACTERISTICS TA = 0°C TO +70°C, VCC = 5V ± 5% (Note 1,5)

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	-DISTR Strobe Width	75		ns	
RC	Read cycle	135		ns	
tDDD	Delay from -DISTR to Data		75	ns	100 pF Load
tHZ	-DISTR to Floating Data Delay	0	50	ns	100 pF Load, Note 4
tDOW	-DOSTR Strobe Delay	50		ns	
WC	Write Cycle	135		ns	
tDS	Data Setup Time	10		ns	
tDH	Data Hold Time	25		ns	
tRA	Address Hold Time from -DISTR	0		ns	Note 2
tRCS	Chip Select Hold Time from -DISTR	0		ns	Note 2
tAR	-DISTR Delay from Address	10		ns	Note 2
tCSR	-DISTR Delay from Chip Select	10		ns	Note 2
tWA	Address Hold TIme from -DOSTR	5		ns	Note 2
tWCS	Chip Select Hold Time from -DOSTR	5		ns	Note 2
tAW	-DOSTR Delay from Address	25		ns	Note 2
tCSW	-DOSTR Delay from Select	10		ns	Note 2
tRW	Reset Pulse Width	5		µs	
tXH	Duration of Clock High Pulse	140		ns	External Clock
tXL	Duration of Clock Low Pulse	140		ns	External Clock

Notes:
1. RCLK is internally derived fron the internal -BAUDOUT signal.
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timing are referenced to valid 0 and 1. (see AC TEST POINTS.)

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AC CHARACTERISTICS (Cont.) TA = 0°C TO +70°C, VCC = 5V ± 5% (Note 1,5)

Symbol	Parameter	Min	Max	Units	Conditions
Transmitter					
tHR1	Delay from Rising Edge of -DOSTR (WR THR) To Reset Interrupt		75	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	24	40	CLK Cycles	Note 3
tSI	Delay from Initial Write to Interrupt	16	24	CLK Cycles	Note 3
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK Cycles	Note 3
tIR	Delay from -DISTR (RD IIR) to Reset Interrupt (THRE)		75	ns	100 pF Load
Modem Control					
tMDO	Delay from -DOSTR (WR MCR) to Output		50	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		70	ns	100 pF Load
tRIM	Delay to Reset Interrupt from -DISTR (RS MSR)		70	ns	100 pF Load
Receiver					
tSINT	Delay from Stop to Set Interrupt		1	CLK cycles	Note 3
tRINT	Delay from -DISTR (RD RBR/RDLSR) to Reset Interrupt		200	ns	100 pF Load
Parallel Port					
tDT	Data Time	1		µs	
tSB	Strobe Time	1	500	µs	
tAD	Acknowledge Delay (Busy Start to Acknowledge)			µs	Defined by Printer
tAKD	Acknowledge Delay (Busy End to Acknowledge)			µs	Defined by Printer
tAK	Acknowledge Duration Time			µs	Defined by Printer
tBSY	Busy Duration Time			µs	Defined by Printer
tBSD	Busy Delay Time			µs	Defined by Printer

Notes:
1. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timing are referenced to valid 0 and 1. (see AC TEST POINTS.)

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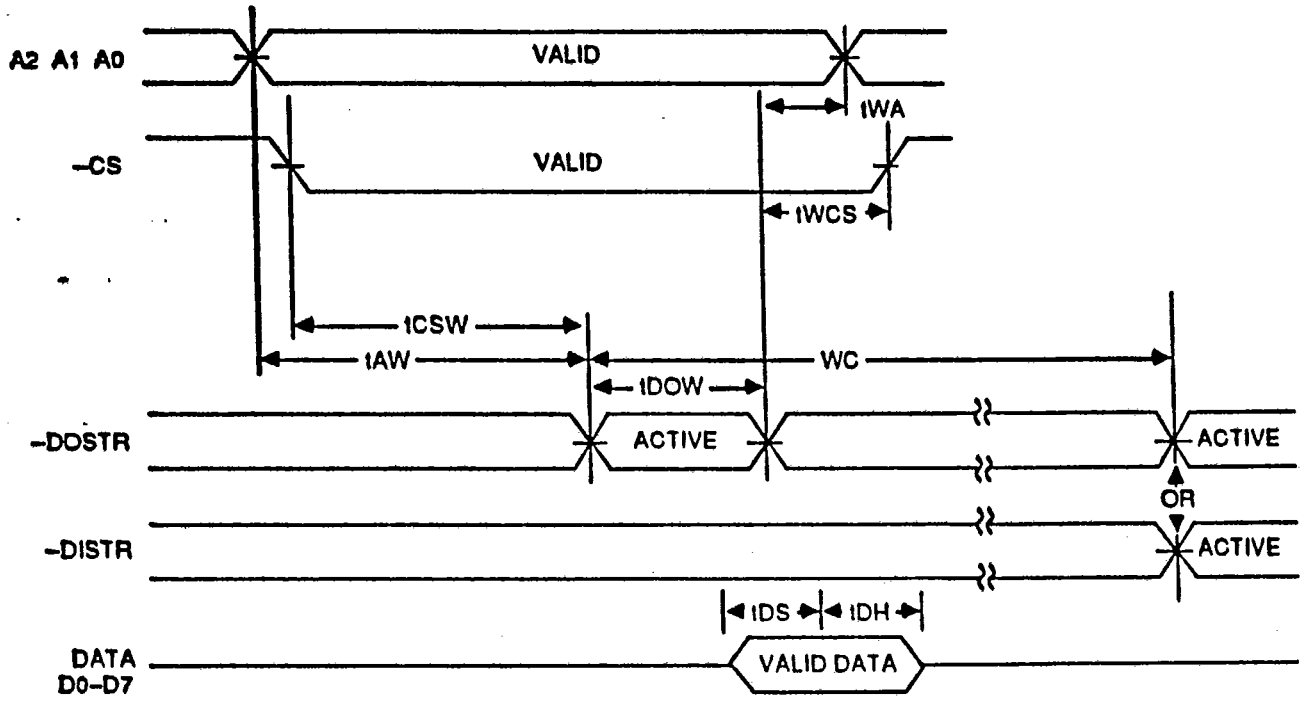
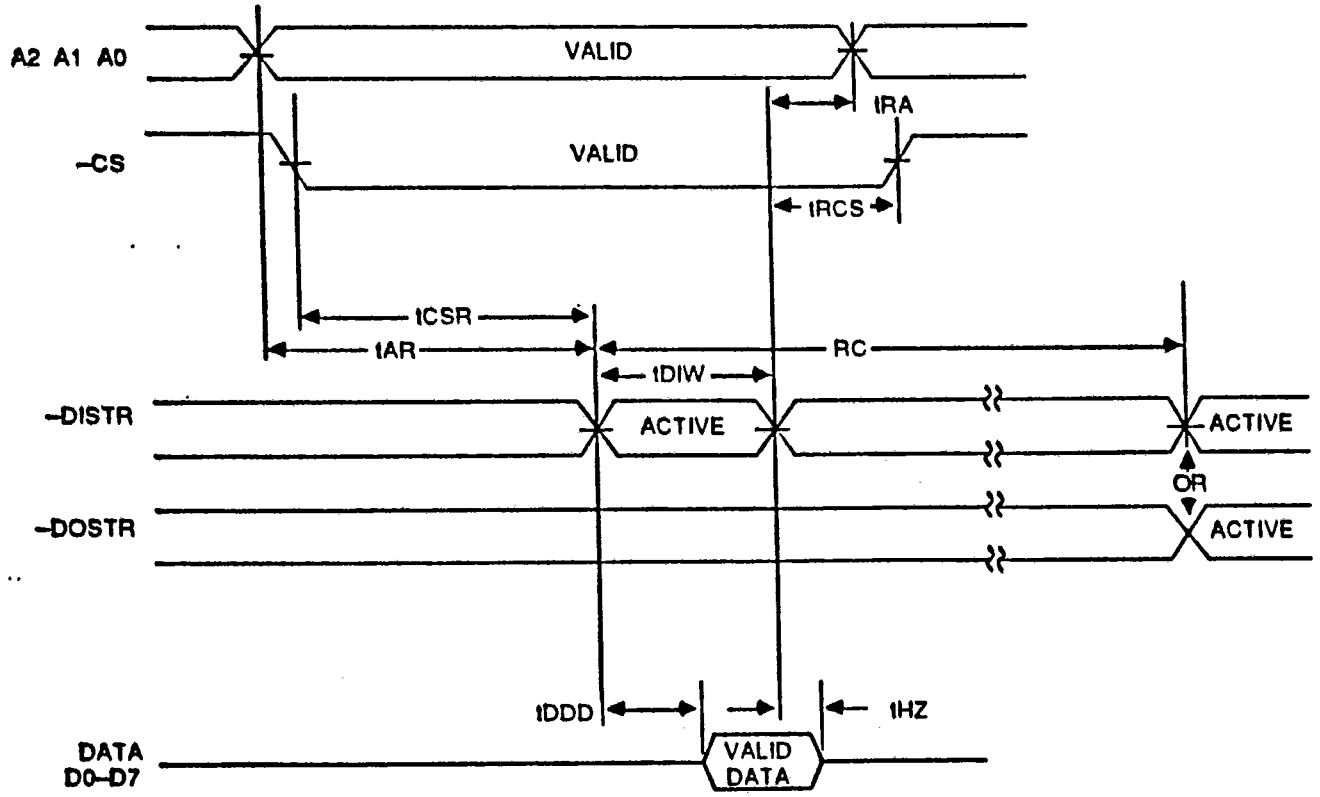
WRITE CYCLE TIMING



READ CYCLE TIMING



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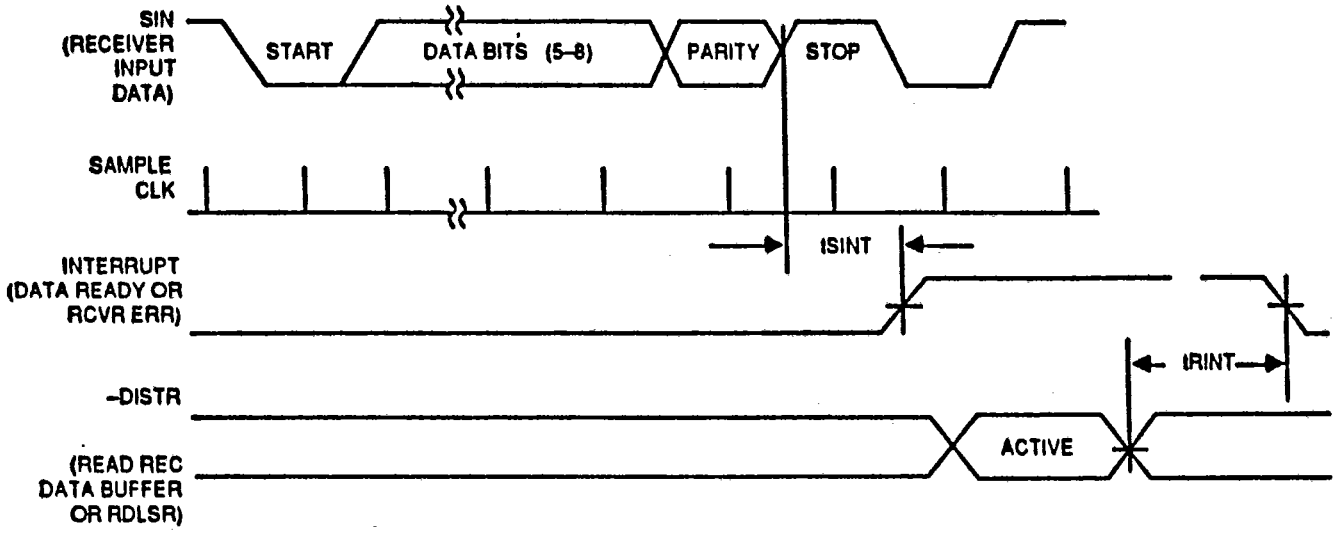
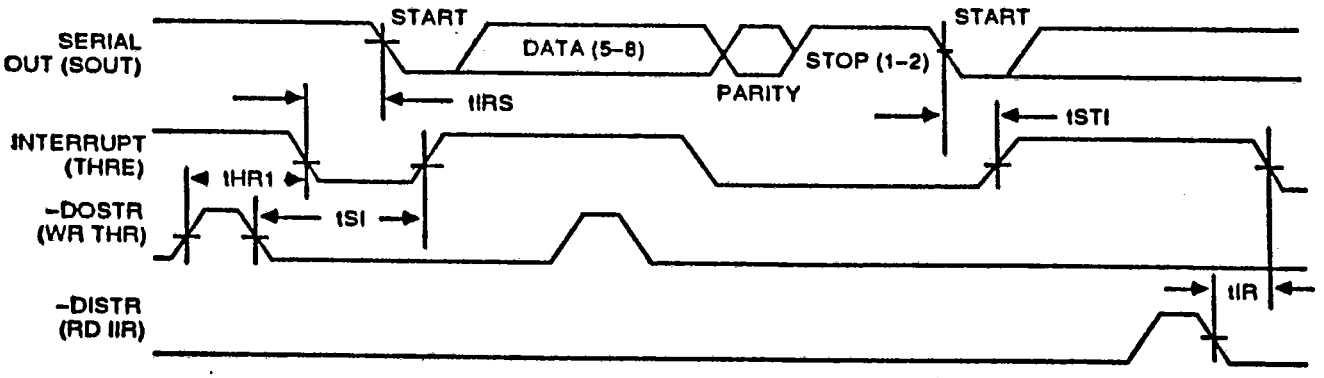
RECEIVER TIMING



TRANSMITTER TIMING



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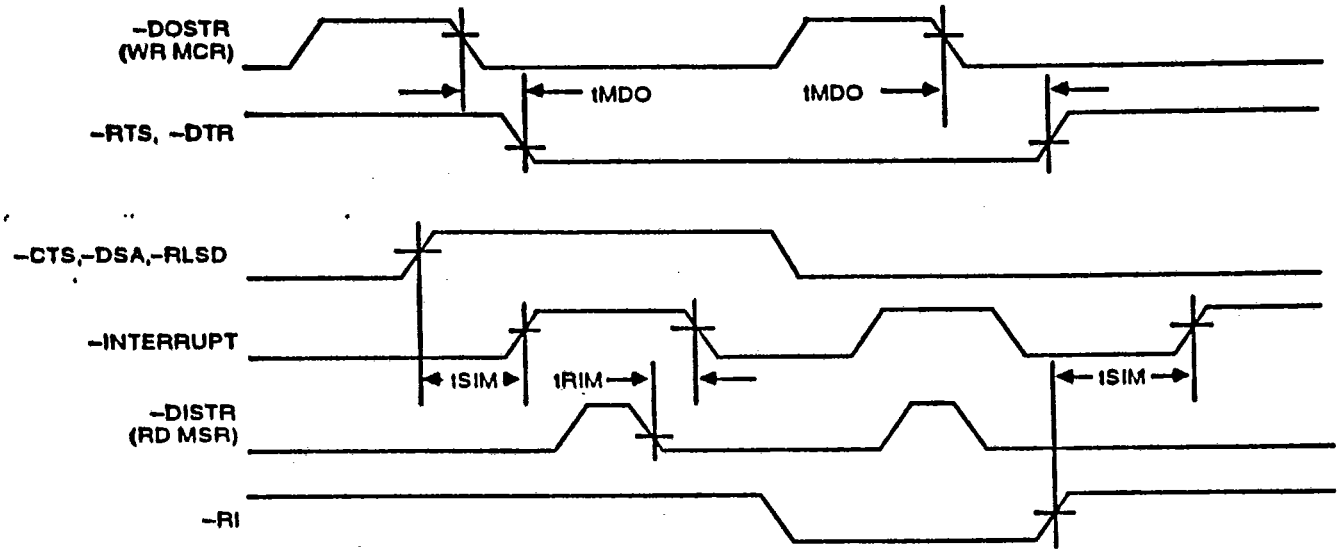
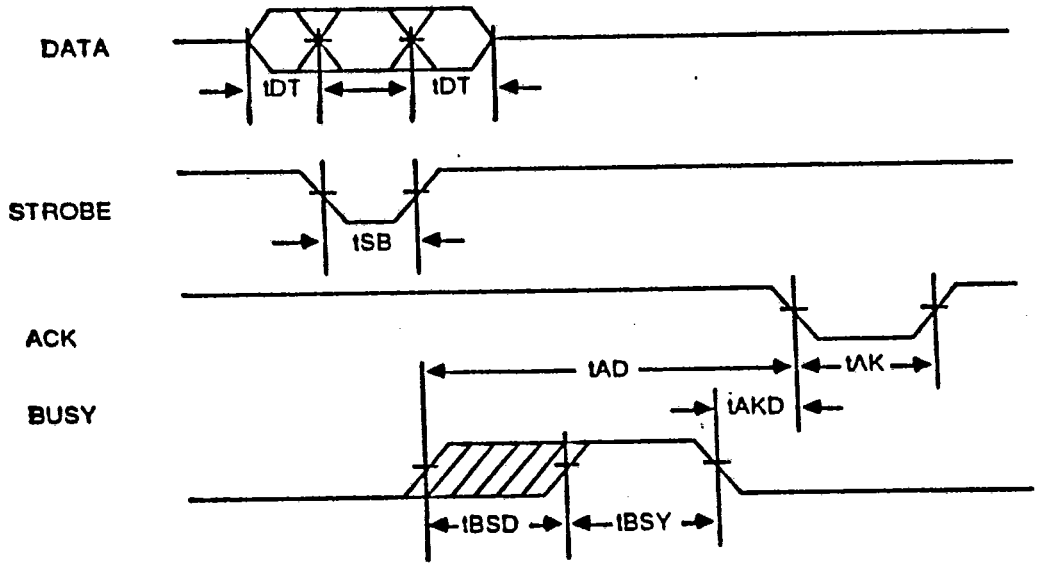
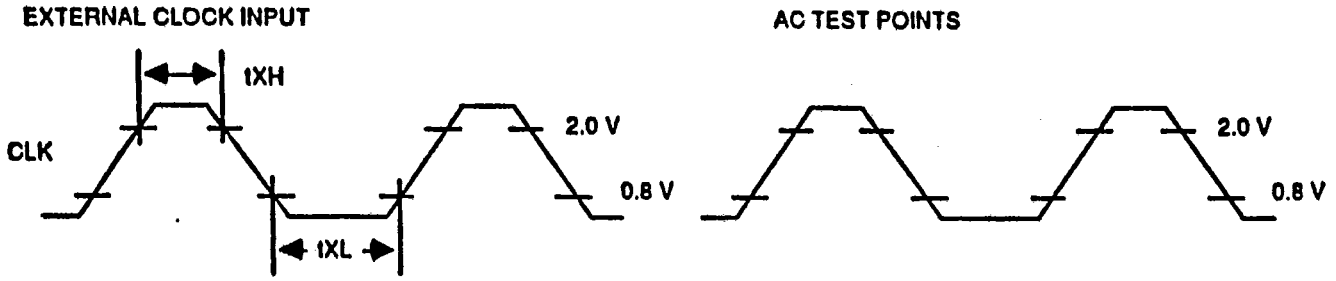
MODEM TIMING



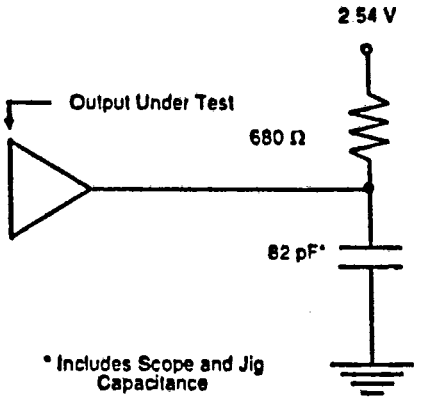
PARALLEL PORT TIMING



AC TESTING INPUT/OUTPUT WAVEFORMS



TEST CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature -10C to +70C
Storage Temperature -65C to +150C
Supply Voltage to Ground Potential -0.5V to Vcc +0.3V
Applied Output Voltage -0.5V to Vcc +0.3V
Applied Input Voltage -0.5V to +7.0V
Power Dissipation 500mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C TO +70°C, VCC = 5V ± 5%

Symbol	Parameter	Min	Max	Units	Conditions
VILX	Clock Input Low Voltage	-0.5	0.6	V	
VIHX	Clock Input High Voltage	3.0	VCC	V	
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.2	VCC	V	
VOL	Output Low Voltage		0.4	V	IOL = 6.0 mA on DB0-DB7 IOL = 20 mA on PD0-PD7 IOL = 10 mA on -INIT, -AFD, -STB, and -SLIN (see Note 1) IOL = 6.0 mA on all other outputs
VOH	Output High Voltage	2.4		V	IOH = -6.0 mA on DB0-DB7 IOH = -12.0 mA on PD0-PD7 IOH = -0.2 mA on -INIT, -AFD, -STB, and -SLIN IOH = -6.0 mA on all other outputs.
ICC	Power Supply Current		30	mA	VCC = 5.25 V, No loads on SIN0,1, -DSR0,1; -RLSD0,1; -CTS0,1. RI0,RI1 = 2.2 V. Other inputs = 0.8 V. Baud rate generator = 4 MHz. Baud rate = 56K
IIL	Input Leakage		±10	µA	VCC = 5.25 V, GND = 0 V. All other pins floating
ICL	Clock Leakage		±10	µA	VIN = 0 V, 5.25 V
IOZ	3-State Leakage		±20	µA	VCC = 5.25 V, GND = 0 V. VOUT = 0 V, 5.25 V 1) Chip Deselected 2) Chip and write mode selected
VIL(RES)	Reset Schmitt VIL		0.8	V	
VIH(RES)	Reset Schmitt VIH	2.0		V	

Note 1: -INIT, -AFD, -STB, and -SLIN are open collector output pins that each have an internal pull-up resistor (2.5 kΩ - 3.5 KΩ) to Vcc. This will generate a maximum of 2.0 mA of internal IOL. In addition to this internal current, each pin will sink at least 10 mA, while maintaining the VOL specification of 0.4 V Max.

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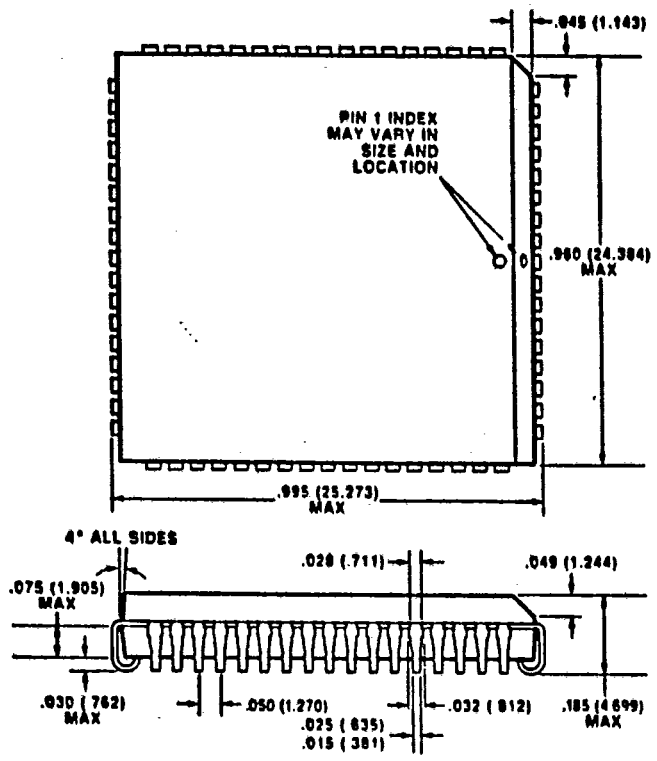
PACKAGE OUTLINE

68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

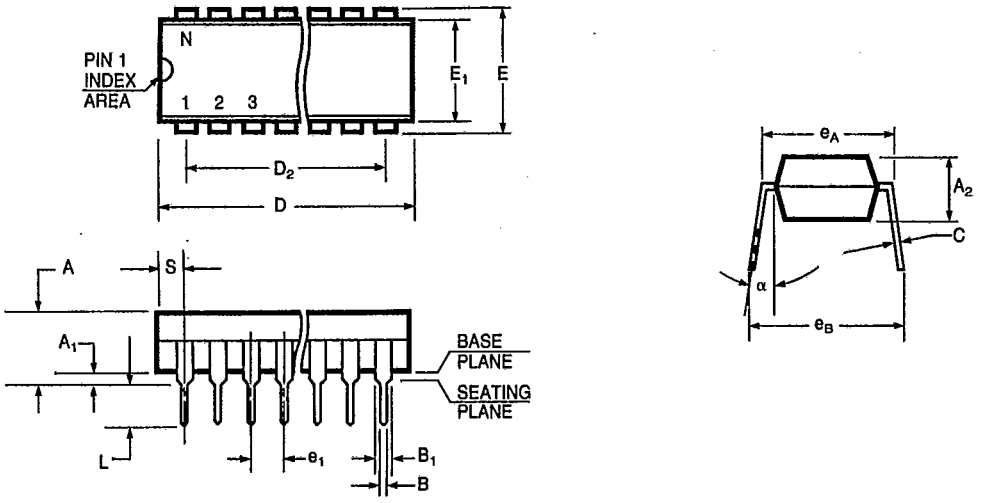


NOTES UNLESS OTHERWISE SPECIFIED
1. TOLERANCE TO BE ± .005 (0.127)
2. LEADFRAME MATERIAL COPPER
3. LEAD FINISH MATTE TIN PLATE OR SOLDER DIP
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES

ORDERING INFORMATION:

PART NUMBER	OPERATING TEMPERATURE	PACKAGE TYPE
MX16C451E QC	0 - 70°C	68 PIN PLCC

NOTE:
If external clock option is required, please refer to the MX16C451 data sheet.

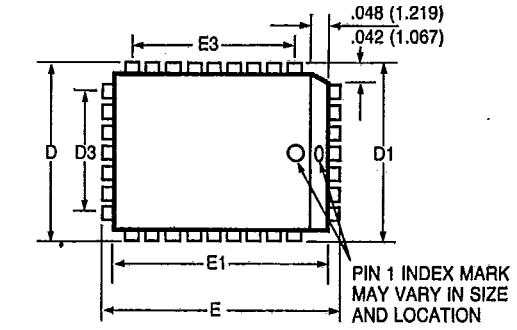


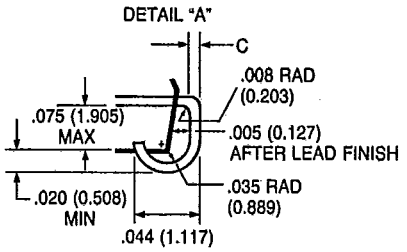
PLASTIC DUAL-IN-LINE PACKAGES (PDIP)

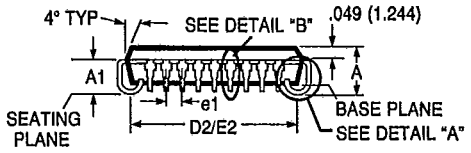
16, 18, 20, 24, 28 LEAD 300 MIL WIDE AND 24, 28, 32, 40 LEAD 600 MIL WIDE

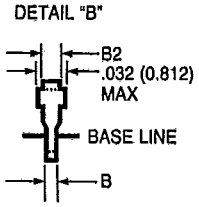
LEADS	24		24		28		28		32		40	
WIDTH	.300		.500		.300		.600		.600		.600	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)
A1	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)
A2	.125 (3.18)	.155 (3.94)	.135 (3.43)	.165 (4.19)	.125 (3.18)	.155 (3.94)	.135 (3.43)	.165 (4.19)	.135 (3.43)	.165 (4.19)	.135 (3.43)	.165 (4.19)
B	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)
B1	.060 (1.52)	TYP	.060 (1.52)	TYP	.060 (1.52)	TYP	.060 (1.52)	TYP	.050 (1.27)	TYP	.060 (1.52)	TYP
C	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)
D	1.230 (31.24)	1.270 (32.26)	1.230 (31.24)	1.280 (32.51)	1.345 (34.16)	1.355 (34.42)	1.390 (35.31)	1.470 (37.34)	1.640 (41.66)	1.660 (42.16)	2.030 (51.56)	2.080 (52.83)
D2	1.100 (27.94)	TYP	1.100 (27.94)	TYP	1.300 (33.02)	TYP	1.300 (33.02)	TYP	1.400 (35.56)	TYP	1.900 (48.26)	TYP
E	.300 (7.62)	.320 (8.13)	.600 (15.24)	.620 (15.75)	.300 (7.62)	.325 (8.26)	.600 (15.24)	.620 (15.75)	.600 (15.24)	.620 (15.75)	.600 (15.24)	.620 (15.75)
E1 (4)	.240 (6.10)	.280 (7.11)	.520 (13.21)	.560 (14.22)	.270 (6.86)	.290 (7.37)	.520 (13.21)	.560 (14.22)	.520 (13.21)	.560 (14.22)	.520 (13.21)	.560 (14.22)
e1 (3)	.100 (2.54)	TYP	.100 (2.54)	TYP	.100 (2.54)	TYP	.100 (2.54)	TYP	.100 (2.54)	TYP	.100 (2.54)	TYP
eA(3)	.300 (7.62)	TYP	.600 (15.24)	TYP	.300 (7.62)	TYP	.600 (15.24)	TYP	.600 (15.24)	TYP	.600 (15.24)	TYP
eB (3)	.350 (8.89)	TYP	.650 (16.51)	TYP	.350 (8.89)	TYP	.650 (16.51)	TYP	.650 (16.51)	TYP	.650 (16.51)	TYP
L	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)
N	24		24		28		28		32		40	
S	.040 (1.02)	.085 (2.16)	.040 (1.02)	.085 (2.16)	.020 (.508)	.030 (.762)	.040 (1.02)	.085 (2.16)	.040 (1.02)	.085 (2.16)	.040 (1.02)	.090 (2.29)
∝ (5)	0	15	0	15	0	15	0	15	0	15	0	15
Theta JA Cu: (6)			55		50		55		45		45	
°C/Watt AL42: (6)			110		105		110		105		100	

NOTES:
1. Refer to applicable symbol glossary.
2. All dimensions are in inches (mm).
3. e1, eA and eB apply for installing on a PC board.
4. D and E1 do not include mold flash.
5. ∝ in degrees applies to spread of leads.
6. The Thermal Resistance, Theta JA, in °C/Watt, quoted above is for a 10,000 sq. mil die in still air and shown for both copper and alloy-42 frames. Values are approximate.
7. Lead frame material: alloy 42 or copper.
8. Lead finish: Matte tin or Sn/Pb solder.
9. Note: Call Manufacturer for dimensional information on 16, 18, 20, 48 and 64 lead packages.









PLASTIC LEADED CHIP CARRIERS (PLCC)

24, 32, 44, 68, AND 84 LEAD

LEADS	28		32		44		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165 (4.19)	.180 (4.57)	.100 (2.54)	.140 (3.56)	.165 (4.19)	.180 (4.57)	.165 (4.19)	.200 (5.08)	.165 (4.19)	.200 (5.08)
A1	.090 (2.29)	.120 (3.05)	.060 (1.52)	.095 (2.41)	.090 (2.29)	.120 (3.05)	.090 (2.29)	.130 (3.30)	.090 (2.29)	.130 (3.30)
B	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)
B2	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)
C	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)
D	.485 (12.32)	.495 (12.57)	.485 (12.32)	.495 (12.57)	.685 (17.40)	.695 (17.65)	.985 (25.02)	.995 (25.27)	1.185 (30.10)	1.195 (30.35)
D1	.450 (11.43)	.456 (11.58)	.447 (11.35)	.453 (11.51)	.650 (16.51)	.656 (16.66)	.950 (24.13)	.958 (24.33)	1.150 (29.21)	1.158 (29.41)
D2	.390 (9.91)	.430 (10.92)	.390 (9.91)	.430 (10.92)	.590 (14.99)	.630 (16.00)	.890 (22.61)	.930 (23.62)	1.090 (27.69)	1.130 (28.70)
D3	.300 (7.62)	REF	.300 (7.62)	REF	.500 (12.70)	REF	.800 (20.32)	REF	1.000 (25.40)	REF
E	.485 (12.32)	.495 (12.57)	.585 (14.86)	.595 (15.11)	.685 (17.40)	.695 (17.65)	.985 (25.02)	.995 (25.27)	1.185 (30.10)	1.195 (30.35)
E1	.450 (11.43)	.456 (11.58)	.547 (13.89)	.553 (14.05)	.650 (16.51)	.656 (16.66)	.950 (24.13)	.958 (24.33)	1.150 (29.21)	1.158 (29.41)
E2	.390 (9.91)	.430 (10.92)	.490 (12.45)	.530 (13.46)	.590 (14.99)	.630 (16.00)	.890 (22.61)	.930 (23.62)	1.090 (27.69)	1.130 (28.70)
E3	.300 (7.62)	REF	.400 (10.16)	REF	.500 (12.70)	REF	.800 (20.32)	REF	1.000 (25.40)	REF
e1	.050 (1.27)	TYP	.050 (1.27)	TYP	.050 (1.27)	TYP	.050 (1.27)	TYP	.050 (1.27)	TYP
N	28		32		44		68		84	
ND	7		7		11		17		21	
NE	7		9		11		17		21	
Theta JA (5) (°C/Watt)	45		45		45		45		45	

NOTES:
1. Refer to applicable symbol glossary.
2. All dimensions are in inches (mm).
3. Controlling dimension inch.
4. D1 and E1 do not include mold flash.
5. The Thermal Resistance, Theta JA, in °C/Watt, quoted above is for a 10,000 sq. mil die in still air with copper frame. Values are approximate.
6. Lead frame material: copper.
7. Lead finish: Matte tin or Sn/Pb solder dip.
8. Note: Call Manufacturer for dimensional information on 20, 52 and 84 lead packages.