MX16C452

DUAL ASYNCHRONOUS COMMUNICATIONS ELEMENT

DESCRIPTION

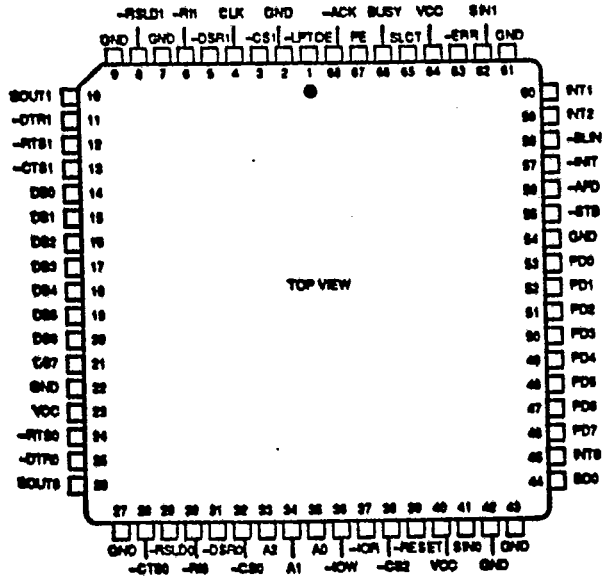
The MX16C452 is a dual universal asynchronous receiver and transmitter with a bidirectional CENIRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56kHz. The MX16C452 fabricated in an advanced 2u CMOS process to achieve low power drain and high speed requirements.

The MX16C452 is an imporved version of the VL16C452 with higher speed operating access time. The MX16C452 performs the parallel to serial/serial to parallel conversion on the data chracters received from the CPU or the MODEM. The MX16C452 also provides the user with a fully bidirectional parallel data port that fully supports the paralle CENTRONICS type printer. The on borad status of the transfer operations being performed. The MX16C452 also has complete MODEM control capability,and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The MX16C452 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

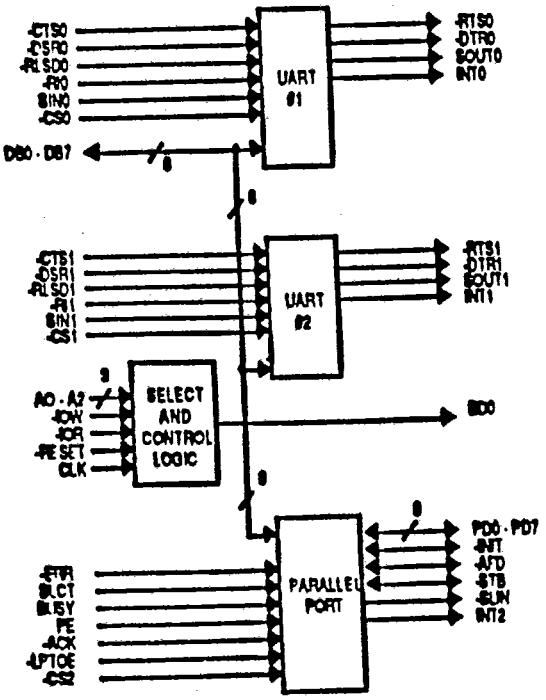
FEATURES

* Pin-to-pin and functionally compatible to VL16C452
* Bidirectional printer port
* Modem control signals (CTS-, RTS-, DSR-, DTR-, RI-, CD-,)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Direct replacement of logic for PC/XT/AT
* Status report register
* Independent trasmit and receive control
* TTL compatible inputs, outputs
* Fully compatible with all new bidirectional PS/2 printer port
* High data transfer rate

PIN DIAGRAM



BLOCK DIAGRAM



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MX16C452

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
SIN0,SIN1	41,62	Serial Data Inputs: The serial data inputs move information from the communication line or modem to the MX16C452 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
-CS0,-CS1, -CS2	32,3,38	Chip Selects: Each Chip Select input acts as an enable for the write and read signals for the serial channels 0 (-CS0) and 1 (-CS1). -CS2 enables the signals to the line printer port.
BDO	44	Bus Buffer Output: This active high output is asserted when either serial channel or the parallel port is selected as an output. This output can be used to control the system bus driver device (74LS245).
PD0-PD7	53-46	Parallel Data Bits (0-7): Theses eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when the port is not selected (-CS2 is high).
-RESET	39	Reset: When low, the reset input forces the MX16C452 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
INT0,INT1	45,60	Serial Channel Interrupts: Each serial channel interrupt goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of its associated channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset operation.
-RI0,-RI1	30,6	Ring Indicator Inputs: When low, -RI indicates that a telephone ringing signal has been received by the modem or data set. The -RI signal is a modem control input whose condition is tested by reading MSR(6) (RI) of each UART. The Modem Status Register output TERI[MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER(3) = 1] and RI changes from a high to low, an interrupt is generated.
-LPTOE	1	Line Printer Output Enable: This input signal enables the parallel line printer when it is low. When this signal is high, the pins of the line printer are held in a high-impedance state. This line may be tied to ground for normal line printer operation.
VCC	23,40,64	Power Supply: 5V ±5%
GND	2,7,9,22,27, 42,43,54,61	Ground (0 V): All pins must be tied to ground for proper operation.
-RLSD0, -RLSD1	29,8	Receive Line Signal Detect: When active(low), -RLSD indicates that the data carrier has been detected by the modem or data set. -RLSD is a modem input whose condition can be tested by the CPU by reading MSR(7) (RLSD) of the Modem Status Registers. MSR(3) (DRLSD) of the Modem Status Register indicates whether the -RLSD input has changed since the previous reading of the MSR. -RLSD has no effect on the receiver. If the -RLSD changes state with the modem status interrupt enabled, an interrupt is generated.

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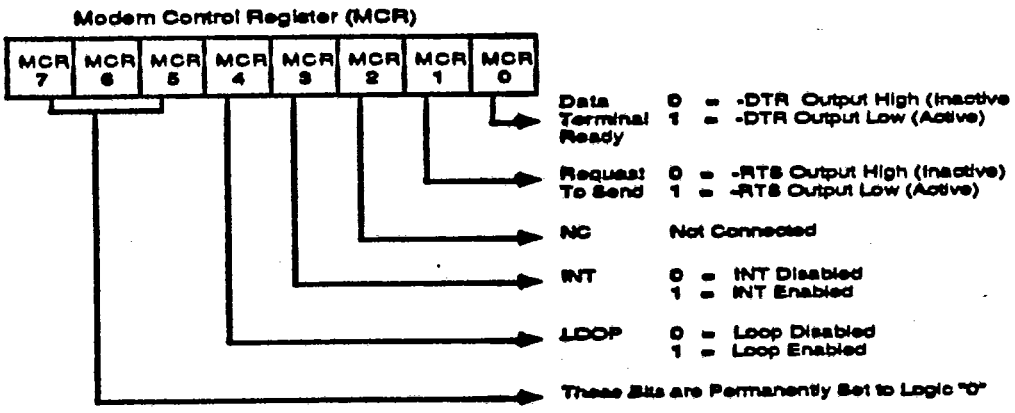
MODEM CONTROL REGISTER



BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

MODEM CONTROL REGISTER BITS

MCR BITS	Logic 1	Logic 0
MCR(0) Data Terminal Ready (DTR)	-DTR Output Low	-DTR Output High
MCR(1) Request to Send (RTS)	-RTS Output Low	-RTS Output High
MCR(2) 0		
MCR(3) Interupt (INT) Enable	INT Enabled	INT Disabled
MCR(4) Loop	Loop Enabled	Loop Disabled
MCR(5) 0		
MCR(6) 0		
MCR(7) 0		

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PARALLEL PORT REGISTERS

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	BUSY	ACK	PE	SLCT	ERROR	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	INIT	AUTOFD	STROBE
Write Port	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	1	IRQ ENB	SLIN	INIT	AUTOFD	STROBE

TABLE 12. PARALLEL PORT REGISTER SELECT

Control Pins					Register Selected
-IOR	-IOW	-CS2	A1	A0	
0	1	0	0	0	Read Port
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Port
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

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SERIAL CHANNEL ACCESSIBLE REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TE MT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

*LSB Data Bit 0 is the first bit transmitted or received

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THR Bits 0 thru 7

THR(0)	Data Bit 0
THR(1)	Data Bit 1
THR(2)	Data Bit 2
THR(3)	Data Bit 3
THR(4)	Data Bit 4
THR(5)	Data Bit 5
THR(6)	Data Bit 6
THR(7)	Data Bit 7

Scratchpad Register is an 8-bit Read/Write register that has no effect on any channel in the MX16C452. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

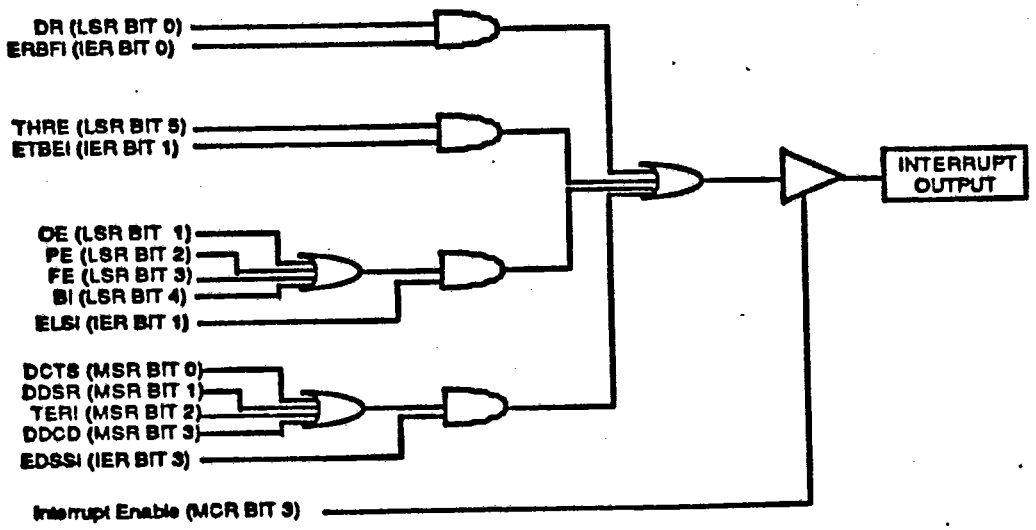
SCR(0)	Data Bit 0
SCR(1)	Data Bit 1
SCR(2)	Data Bit 2
SCR(3)	Data Bit 3
SCR(4)	Data Bit 4
SCR(5)	Data Bit 5
SCR(6)	Data Bit 6
SCR(7)	Data Bit 7

TABLE 5. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the Interrupt Source or THR Write
0	0	0	Fourth	Modem Status	-CTS, -DSR -RI, -RSLD	MSR Read

X = Not Defined

FIGURE 3. INTERRUPT CONTROL LOGIC



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ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature -10C to +70C
Storage Temperature -65C to +150C
Supply Voltage to Ground Potential -0.5V to Vcc +0.3V
Applied Output Voltage -0.5V to Vcc +0.3V
Applied Input Voltage -0.5V to +7.0V
Power Dissipation 500mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C TO +70°C, VCC = 5V ± 5%

Symbol	Parameter	Min	Max	Units	Conditions
VILX	Clock Input Low Voltage	-0.5	0.6	V	
VIHX	Clock Input High Voltage	3.0	VCC	V	
VIL	Input Low Voltage	-0.5	0.8	V	
VIH	Input High Voltage	2.2	VCC	V	
VOL	Output Low Voltage		0.4	V	IOL = 6.0 mA on DB0-DB7 IOL = 20 mA on PD0-PD7 IOL = 10 mA on -INIT, -AFD, -STB, and -SLIN (see Note 1) IOL = 6.0 mA on all other outputs
VOH	Output High Voltage	2.4		V	IOH = -6.0 mA on DB0-DB7 IOH = -12.0 mA on PD0-PD7 IOH = -0.2 mA on -INIT, -AFD, -STB, and -SLIN IOH = -6.0 mA on all other outputs.
ICC	Power Supply Current		30	mA	VCC = 5.25 V, No loads on SIN0,1, -DSR0,1; -RLSD0,1; -CTS0,1. RI0,RI1 = 2.2 V. Other inputs = 0.8 V. Baud rate generator = 4 MHz. Baud rate = 56K
IIL	Input Leakage		±10	µA	VCC = 5.25 V, GND = 0 V. All other pins floating
ICL	Clock Leakage		±10	µA	VIN = 0 V, 5.25 V
IOZ	3-State Leakage		±20	µA	VCC = 5.25 V, GND = 0 V. VOUT = 0 V, 5.25 V 1) Chip Deselected 2) Chip and write mode selected
VIL(RES)	Reset Schmitt VIL		0.8	V	
VIH(RES)	Reset Schmitt VIH	2.0		V	

Note 1: -INIT, -AFD, -STB, and -SLIN are open collector output pins that each have an internal pull-up resistor (2.5 kΩ - 3.5 KΩ) to Vcc. This will generate a maximum of 2.0 mA of internal IOL. In addition to this internal current, each pin will sink at least 10 mA, while maintaining the VOL specification of 0.4 V Max.

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AC CHARACTERISTICS TA = 0°C TO +70°C, VCC = 5V ± 5% (Note 1,5)

Symbol	Parameter	Min	Max	Units	Conditions
tDIW	-IOR Strobe Width	75		ns	
RC	Read cycle	135		ns	
tDDD	Delay from -IOR to Data		75	ns	100 pF Load
tHZ	-IOR to Floating Data Delay	0	50	ns	100 pF Load, Note 4
tDOW	-IOW Strobe Delay	50		ns	
WC	Write Cycle	135		ns	
tDS	Data Setup Time	10		ns	
tDH	Data Hold Time	25		ns	
tRA	Address Hold Time from -IOR	0		ns	Note 2
tRCS	Chip Select Hold Time from -IOR	0		ns	Note 2
tAR	-IOR Delay from Address	10		ns	Note 2
tCSR	-IOR Delay from Chip Select	10		ns	Note 2
tWA	Address Hold Time from -IOW	5		ns	Note 2
tWCS	Chip Select Hold Time from -IOW	5		ns	Note 2
tAW	-IOW Delay from Address	25		ns	Note 2
tCSW	-IOW Delay from Select	10		ns	Note 2
tRW	Reset Pulse Width	5		µs	
tXH	Duration of Clock High Pulse	140		ns	External Clock
tXL	Duration of Clock Low Pulse	140		ns	External Clock

Notes:
1. RCLK is internally derived fron the internal -BAUDOUT signal.
2. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timing are referenced to valid 0 and 1. (see AC TEST POINTS.)

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AC CHARACTERISTICS (Cont.) TA = 0°C TO +70°C, VCC = 5V ± 5% (Note 1,5)

Symbol	Parameter	Min	Max	Units	Conditions
Transmitter					
tHR1	Delay from Rising Edge of -IOW (WR THR) To Reset Interrupt		75	ns	100 pF Load
tIRS	Delay from Initial INTR Reset to Transmit Start	24	40	CLK Cycles	Note 3
tSI	Delay from Initial Write to Interrupt	16	24	CLK Cycles	Note 3
tSTI	Delay from Stop to Interrupt (THRE)		8	CLK Cycles	Note 3
tIR	Delay from -IOR (RD IIR) to Reset Interrupt (THRE)		75	ns	100 pF Load
Modem Control					
tMDO	Delay from -IOW (WR MCR) to Output		50	ns	100 pF Load
tSIM	Delay to Set Interrupt from MODEM Input		70	ns	100 pF Load
tRIM	Delay to Reset Interrupt from -IOR (RS MSR)		70	ns	100 pF Load
Receiver					
tSINT	Delay from Stop to Set Interrupt		1	CLK cycles	Note 3
tRINT	Delay from -IOR (RD RBR/RDLSR) to Reset Interrupt		200	ns	100 pF Load
Parallel Port					
tDT	Data Time	1		µs	
tSB	Strobe Time	1	500	µs	
tAD	Acknowledge Delay (Busy Start to Acknowledge)			µs	Defined by Printer
tAKD	Acknowledge Delay (Busy End to Acknowledge)			µs	Defined by Printer
tAK	Acknowledge Duration Time			µs	Defined by Printer
tBSY	Busy Duration Time			µs	Defined by Printer
tBSD	Busy Delay Time			µs	Defined by Printer

Notes:
1. The internal address strobe is always active.
3. RCLK = tXH and tXL.
4. Charge and discharge time is determined by VOL, VOH and the external loading.
5. All timing are referenced to valid 0 and 1. (see AC TEST POINTS.)

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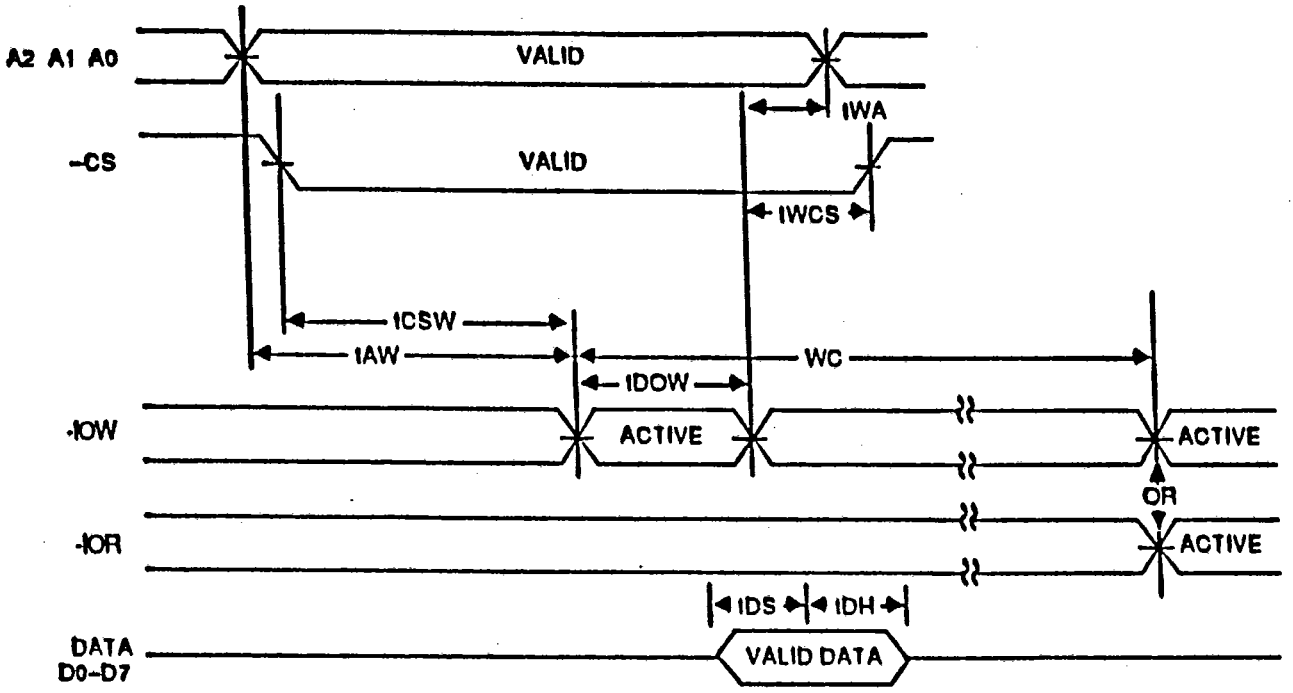
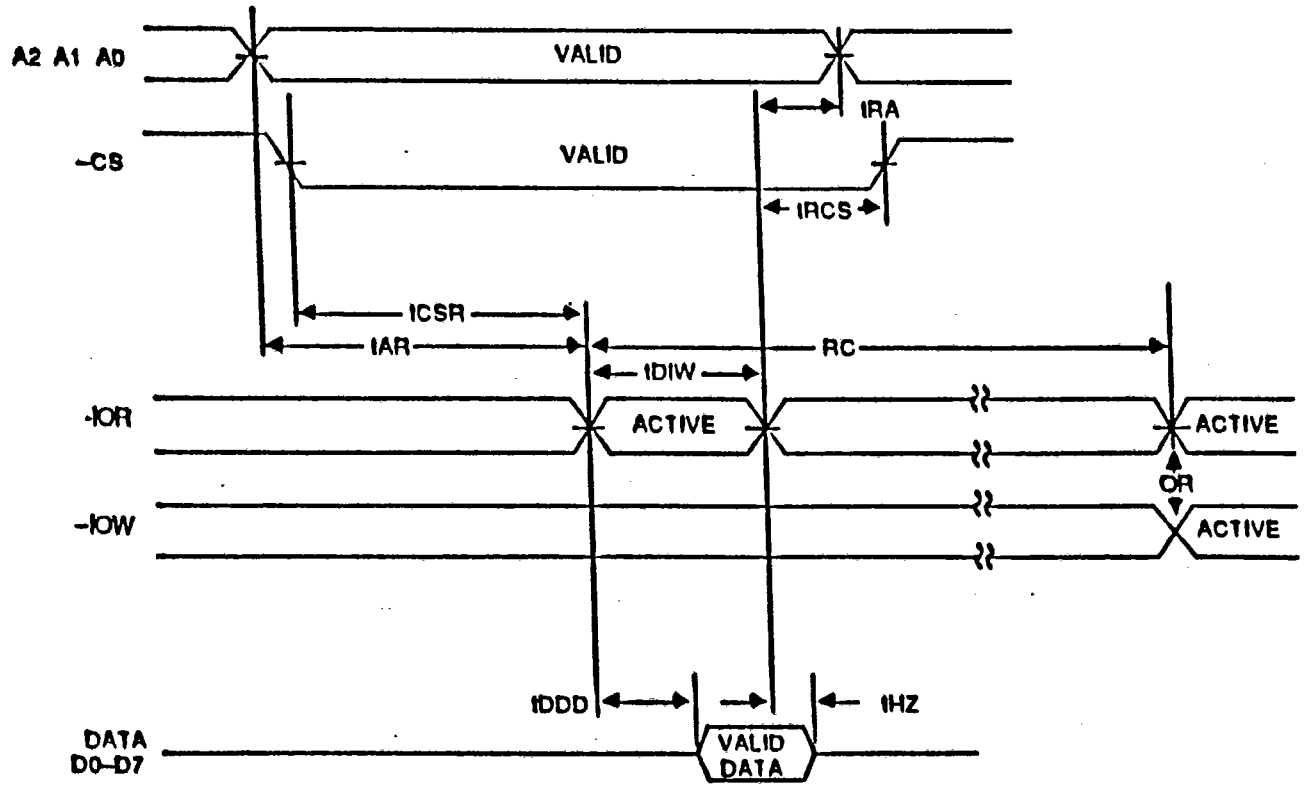
WRITE CYCLE TIMING



READ CYCLE TIMING



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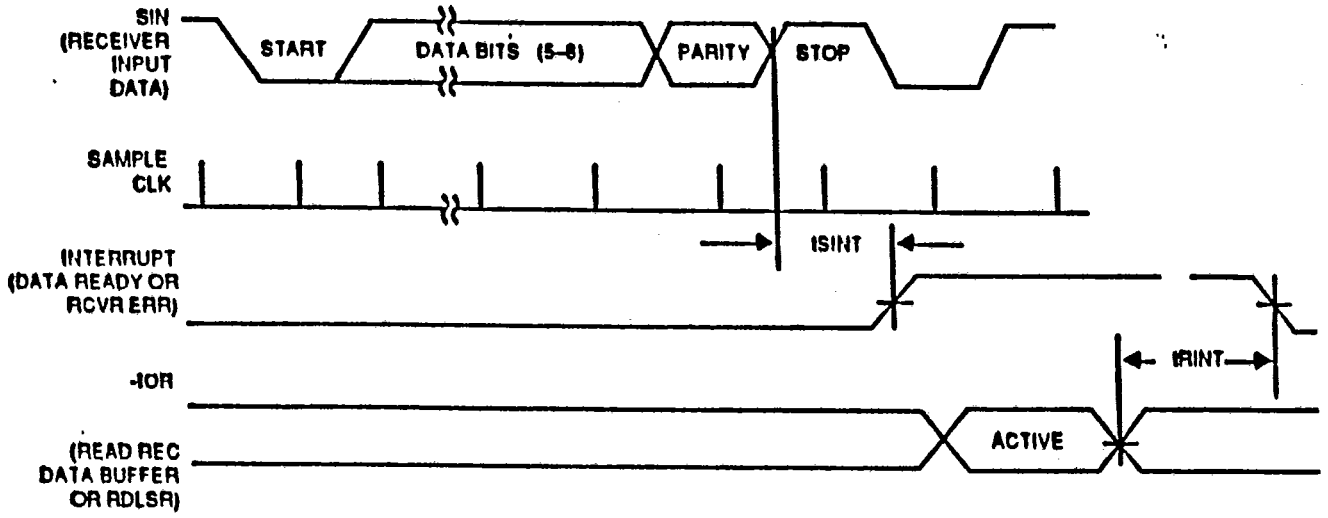
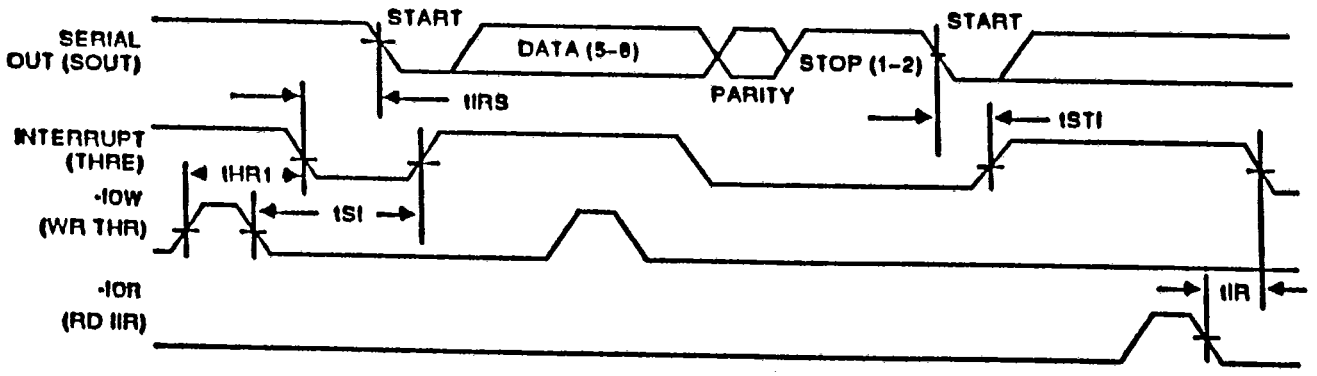
RECEIVER TIMING



TRANSMITTER TIMING



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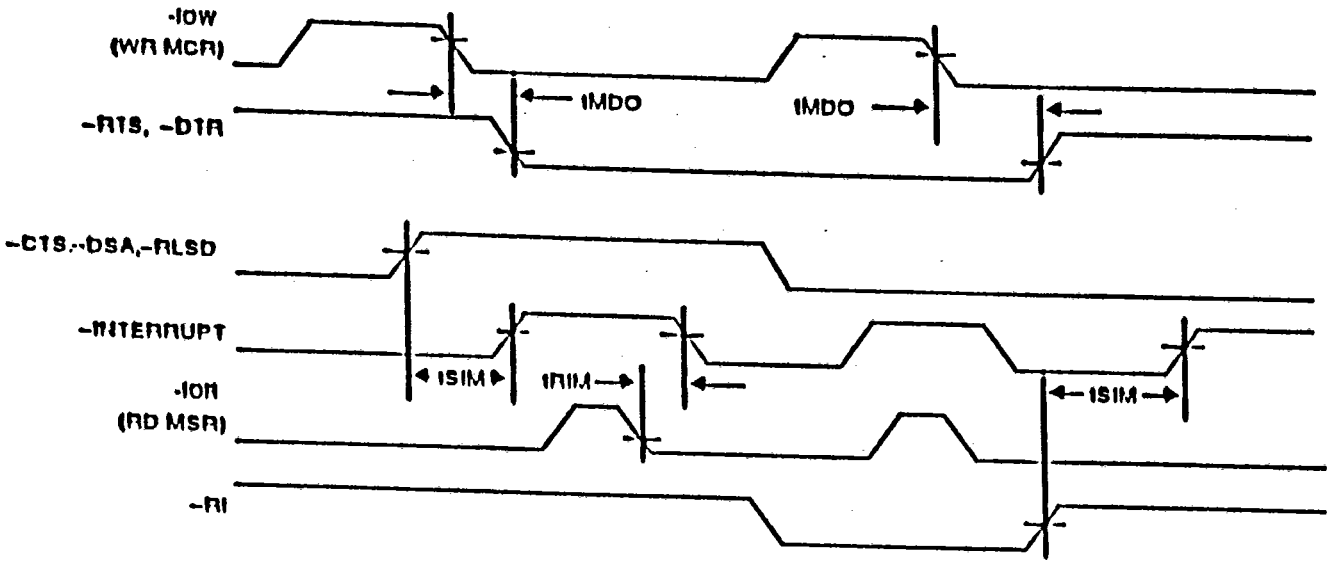
MX16C452

MODEM TIMING



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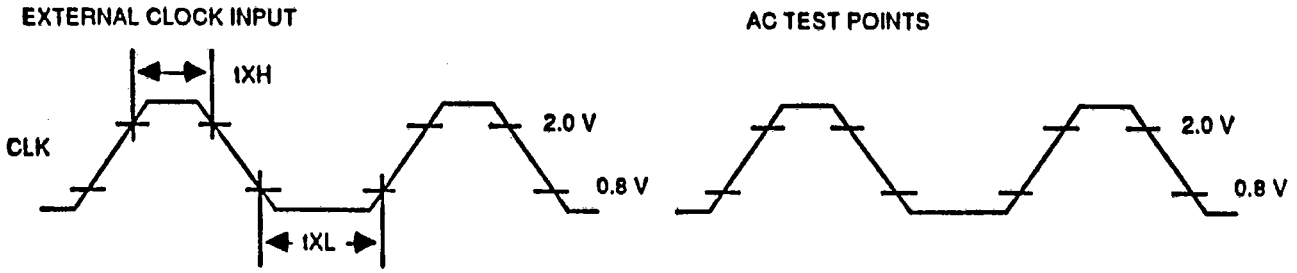
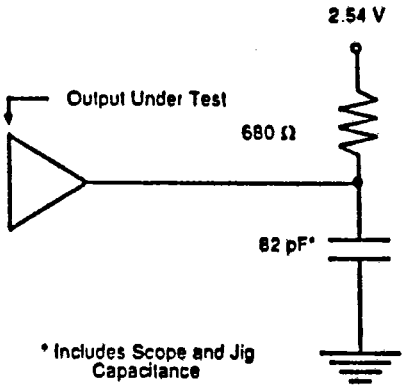
AC TESTING INPUT/OUTPUT WAVEFORMS



TEST CIRCUIT



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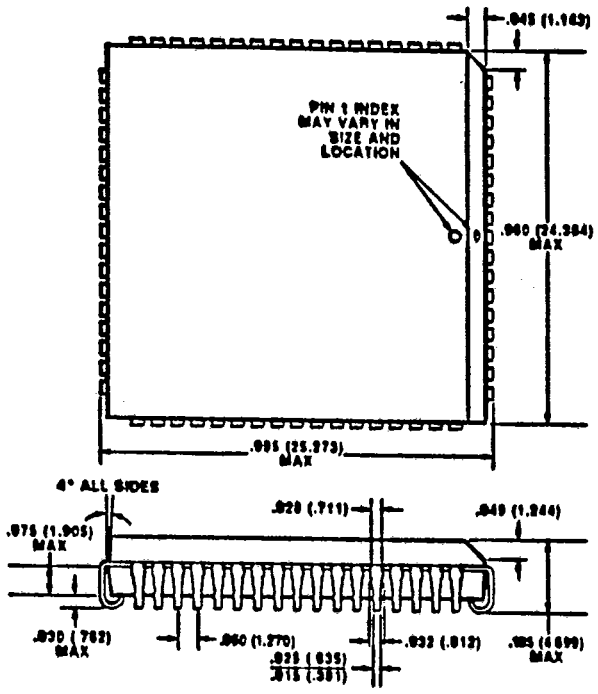
PACKAGE OUTLINES

68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



NOTES UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127)
2. LEADFRAME MATERIAL - COPPER.
3. LEAD FINISH MATTE TIN PLATE OR SOLDER DIP
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

ORDERING INFORMATION:

PART NUMBER	OPERATING TEMPERATURE	PACKAGE TYPE
MX16C452 QC	0 - 70°C	68 PIN PLCC

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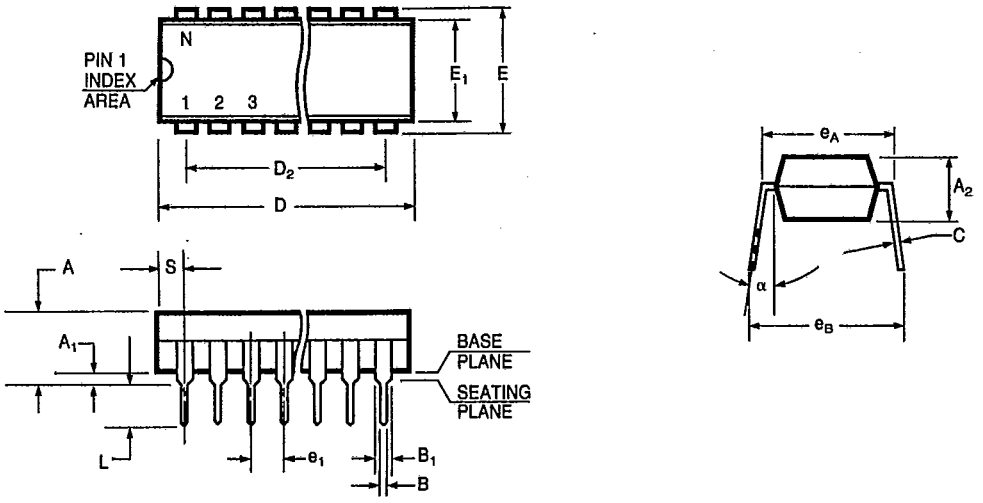

PLASTIC DUAL-IN-LINE PACKAGES (PDIP)

16, 18, 20, 24, 28 LEAD 300 MIL WIDE AND 24, 28, 32, 40 LEAD 600 MIL WIDE

LEADS	24		24		28		28		32		40	
WIDTH	.300		.500		.300		.600		.600		.600	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)	.150 (3.81)	.200 (5.08)
A1	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)	.015 (.381)	.070 (1.78)
A2	.125 (3.18)	.155 (3.94)	.135 (3.43)	.165 (4.19)	.125 (3.18)	.155 (3.94)	.135 (3.43)	.165 (4.19)	.135 (3.43)	.165 (4.19)	.135 (3.43)	.165 (4.19)
B	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)	.015 (.381)	.023 (.584)
B1	.060 (1.52)	TYP	.060 (1.52)	TYP	.060 (1.52)	TYP	.060 (1.52)	TYP	.050 (1.27)	TYP	.060 (1.52)	TYP
C	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)	.008 (.203)	.015 (.381)
D	1.230 (31.24)	1.270 (32.26)	1.230 (31.24)	1.280 (32.51)	1.345 (34.16)	1.355 (34.42)	1.390 (35.31)	1.470 (37.34)	1.640 (41.66)	1.660 (42.16)	2.030 (51.56)	2.080 (52.83)
D2	1.100 (27.94)	TYP	1.100 (27.94)	TYP	1.300 (33.02)	TYP	1.300 (33.02)	TYP	1.400 (35.56)	TYP	1.900 (48.26)	TYP
E	.300 (7.62)	.320 (8.13)	.600 (15.24)	.620 (15.75)	.300 (7.62)	.325 (8.26)	.600 (15.24)	.620 (15.75)	.600 (15.24)	.620 (15.75)	.600 (15.24)	.620 (15.75)
E1 (4)	.240 (6.10)	.280 (7.11)	.520 (13.21)	.560 (14.22)	.270 (6.86)	.290 (7.37)	.520 (13.21)	.560 (14.22)	.520 (13.21)	.560 (14.22)	.520 (13.21)	.560 (14.22)
e1 (3)	.100 (2.54)	TYP	.100 (2.54)	TYP	.100 (2.54)	TYP	.100 (2.54)	TYP	.100 (2.54)	TYP	.100 (2.54)	TYP
eA(3)	.300 (7.62)	TYP	.600 (15.24)	TYP	.300 (7.62)	TYP	.600 (15.24)	TYP	.600 (15.24)	TYP	.600 (15.24)	TYP
eB (3)	.350 (8.89)	TYP	.650 (16.51)	TYP	.350 (8.89)	TYP	.650 (16.51)	TYP	.650 (16.51)	TYP	.650 (16.51)	TYP
L	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)	.120 (3.05)	.140 (3.56)
N	24		24		28		28		32		40	
S	.040 (1.02)	.085 (2.16)	.040 (1.02)	.085 (2.16)	.020 (.508)	.030 (.762)	.040 (1.02)	.085 (2.16)	.040 (1.02)	.085 (2.16)	.040 (1.02)	.090 (2.29)
∝ (5)	0	15	0	15	0	15	0	15	0	15	0	15
Theta JA Cu: (6)			55		50		55		45		45	
°C/Watt AL42: (6)			110		105		110		105		100	

NOTES:
1. Refer to applicable symbol glossary.
2. All dimensions are in inches (mm).
3. e1, eA and eB apply for installing on a PC board.
4. D and E1 do not include mold flash.
5. ∝ in degrees applies to spread of leads.
6. The Thermal Resistance, Theta JA, in °C/Watt, quoted above is for a 10,000 sq. mil die in still air and shown for both copper and alloy-42 frames. Values are approximate.
7. Lead frame material: alloy 42 or copper.
8. Lead finish: Matte tin or Sn/Pb solder.
9. Note: Call Manufacturer for dimensional information on 16, 18, 20, 48 and 64 lead packages.

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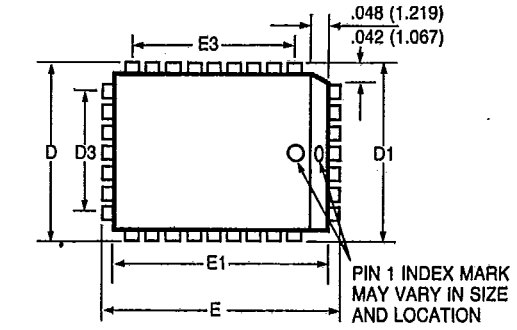

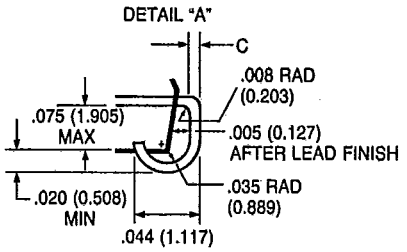

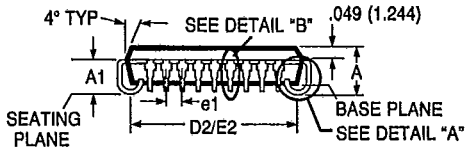

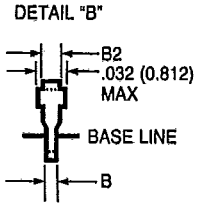

PLASTIC LEADED CHIP CARRIERS (PLCC)

24, 32, 44, 68, AND 84 LEAD

LEADS	28		32		44		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165 (4.19)	.180 (4.57)	.100 (2.54)	.140 (3.56)	.165 (4.19)	.180 (4.57)	.165 (4.19)	.200 (5.08)	.165 (4.19)	.200 (5.08)
A1	.090 (2.29)	.120 (3.05)	.060 (1.52)	.095 (2.41)	.090 (2.29)	.120 (3.05)	.090 (2.29)	.130 (3.30)	.090 (2.29)	.130 (3.30)
B	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)
B2	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)
C	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)
D	.485 (12.32)	.495 (12.57)	.485 (12.32)	.495 (12.57)	.685 (17.40)	.695 (17.65)	.985 (25.02)	.995 (25.27)	1.185 (30.10)	1.195 (30.35)
D1	.450 (11.43)	.456 (11.58)	.447 (11.35)	.453 (11.51)	.650 (16.51)	.656 (16.66)	.950 (24.13)	.958 (24.33)	1.150 (29.21)	1.158 (29.41)
D2	.390 (9.91)	.430 (10.92)	.390 (9.91)	.430 (10.92)	.590 (14.99)	.630 (16.00)	.890 (22.61)	.930 (23.62)	1.090 (27.69)	1.130 (28.70)
D3	.300 (7.62)	REF	.300 (7.62)	REF	.500 (12.70)	REF	.800 (20.32)	REF	1.000 (25.40)	REF
E	.485 (12.32)	.495 (12.57)	.585 (14.86)	.595 (15.11)	.685 (17.40)	.695 (17.65)	.985 (25.02)	.995 (25.27)	1.185 (30.10)	1.195 (30.35)
E1	.450 (11.43)	.456 (11.58)	.547 (13.89)	.553 (14.05)	.650 (16.51)	.656 (16.66)	.950 (24.13)	.958 (24.33)	1.150 (29.21)	1.158 (29.41)
E2	.390 (9.91)	.430 (10.92)	.490 (12.45)	.530 (13.46)	.590 (14.99)	.630 (16.00)	.890 (22.61)	.930 (23.62)	1.090 (27.69)	1.130 (28.70)
E3	.300 (7.62)	REF	.400 (10.16)	REF	.500 (12.70)	REF	.800 (20.32)	REF	1.000 (25.40)	REF
e1	.050 (1.27)	TYP	.050 (1.27)	TYP	.050 (1.27)	TYP	.050 (1.27)	TYP	.050 (1.27)	TYP
N	28		32		44		68		84	
ND	7		7		11		17		21	
NE	7		9		11		17		21	
Theta JA (5) (°C/Watt)	45		45		45		45		45	

NOTES:
1. Refer to applicable symbol glossary.
2. All dimensions are in inches (mm).
3. Controlling dimension inch.
4. D1 and E1 do not include mold flash.
5. The Thermal Resistance, Theta JA, in °C/Watt, quoted above is for a 10,000 sq. mil die in still air with copper frame. Values are approximate.
6. Lead frame material: copper.
7. Lead finish: Matte tin or Sn/Pb solder dip.
8. Note: Call Manufacturer for dimensional information on 20, 52 and 84 lead packages.

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