HARRIS SEMICONDUCTOR

FRX9130D, FRX9130R FRX9130H

Radiation Hardened P-Channel Power MOSFETs

June 1994

Features

- 3A, -100V, RDS(on) = 0.550Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma - Meets Pre-Rad Specifications to 100KRAD(Si) Defined End-Point Specs at 300KRAD(Si) and 1000KRAD(Si) Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot - Survives 3E9 RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 1.50nA Per-RAD(Si)/sec Typically
- Neutron - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm2
- Single Event - Typically Survives 1E5 IONS/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30μm at 80% BVDSS

Description

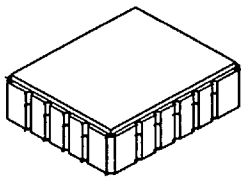
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100KRAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n°) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEU) and/or dose rate (GAMMA DOT) exposure.

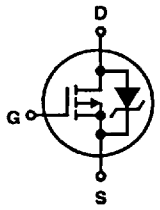
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

LCC 18 PIN



Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

		FRX9130D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25°C	ID	3	A
TC = +100°C	ID	2	A
Pulsed Drain Current	IDM	9	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C	PT	11.4	W
TC = +100°C	PT	4.5	W
Derated Above +25°C		0.09	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	9	A
Continuous Source Current (Body Diode)	IS	3	A
Pulsed Source Current (Body Diode)	ISM	9	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering) 10s Max	TL	300	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3656.1**

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -100V, VGS = 0 VDS = -80V, VGS = 0 VDS = -80V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	9	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 3A	-	-1.73	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 2A	-	0.550	Ω
Turn-On Delay Time	td(on)	VDD = -50V, ID = 3A Pulse Width = 3µs Period = 300µs, Rg = 25Ω 0 ≤ VGS ≤ 10 (See Test Circuit)	-	40	ns
Rise Time	tr		-	136	
Turn-Off Delay Time	td(off)		-	120	
Fall Time	tf		-	74	
Gate-Charge Threshold	QG(th)	VDD = -50V, ID = 3A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		18	72	
Gate-Charge Total	QGM		33	132	
Plateau Voltage	VGP		-2	-8	V
Gate-Charge Source	QGS		2	10	nc
Gate-Charge Drain	QGD		6	24	
Diode Forward Voltage	VSD	ID = 3A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 3A; di/dt = 100A/µs	-	300	ns
Junction-To-Case	RΘjc		-	11	°C/W
Junction-To-Ambient	RΘja	Free Air Operation	-	250	

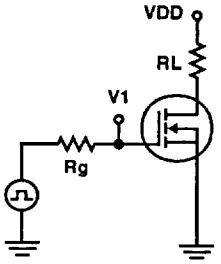


FIGURE 1. SWITCHING TIME TESTING

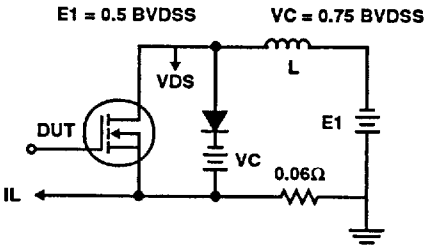


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

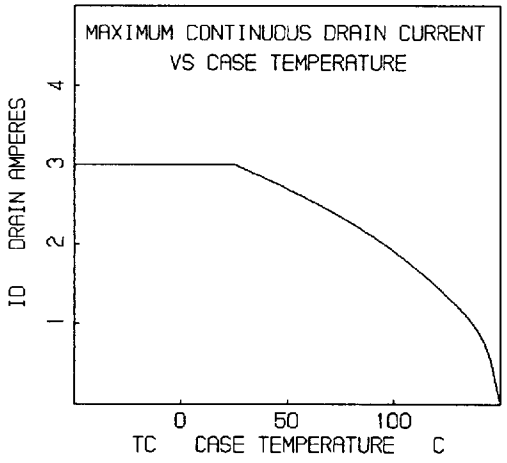
Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

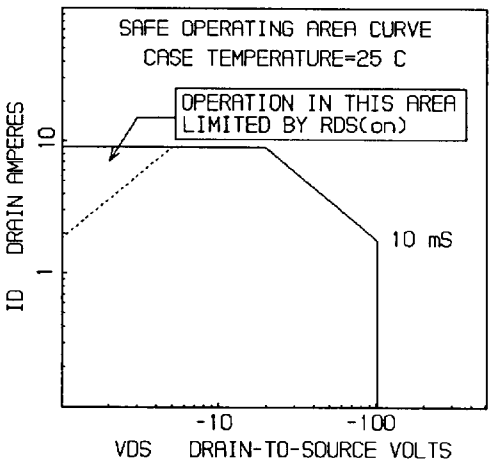
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS
					MIN	MAX	
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	FRX9130D, R	VGS = 0, ID = 1mA	-100	-	V
	(Note 5, 6)	BVDSS	FRX9130H	VGS = 0, ID = 1mA	-95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	FRX9130D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	FRX9130H	VGS = VDS, ID = 1mA	-1.5	-4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	FRX9130D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	FRX9130H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	FRX9130D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	FRX9130H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	FRX9130D, R	VGS = 0, VDS = -80V	-	25	µA
	(Note 5, 6)	IDSS	FRX9130H	VGS = 0, VDS = -80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	FRX9130D, R	VGS = -10V, ID = 3A	-	-1.73	V
	(Note 1, 5, 6)	VDS(on)	FRX9130H	VGS = -16V, ID = 3A	-	-2.60	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	FRX9130D, R	VGS = -10V, ID = 2A	-	0.550	Ω
	(Note 1, 5, 6)	RDS(on)	FRX9130H	VGS = -14V, ID = 2A	-	0.825	Ω

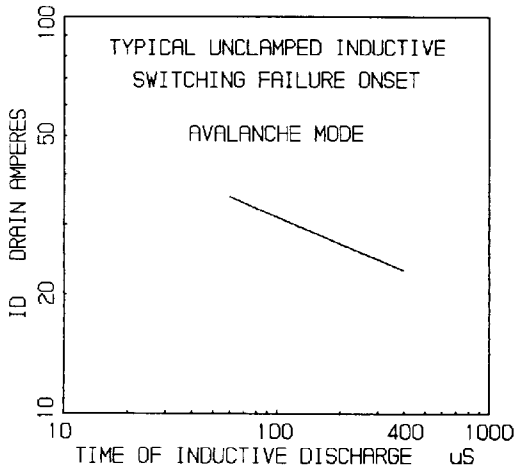
NOTES:

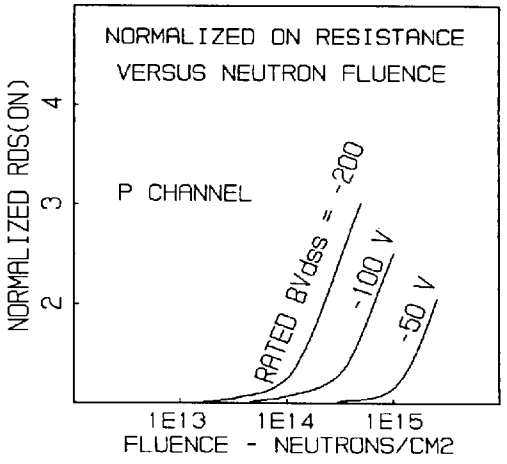
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R" Neutron = 3E13
5. Gamma = 1000KRAD(Si) Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 4/17/90 on TA 17731 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

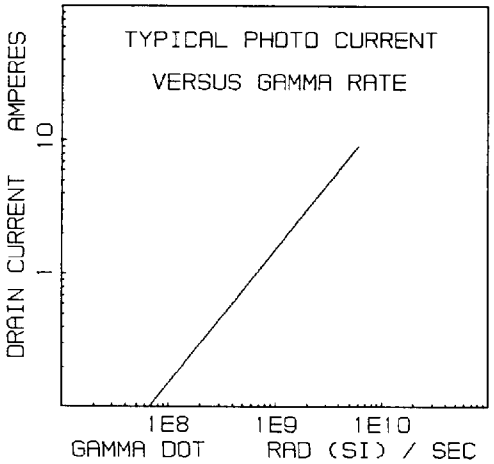
Typical Performance Characteristics

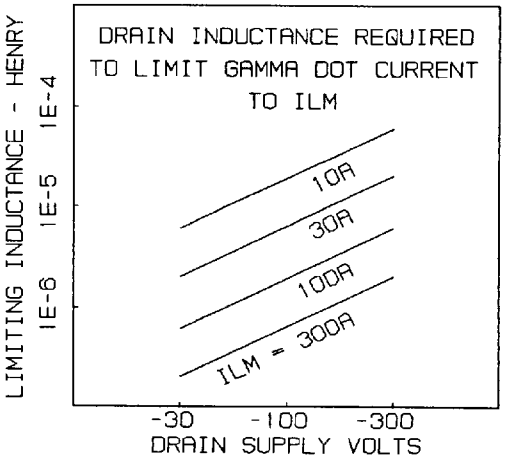




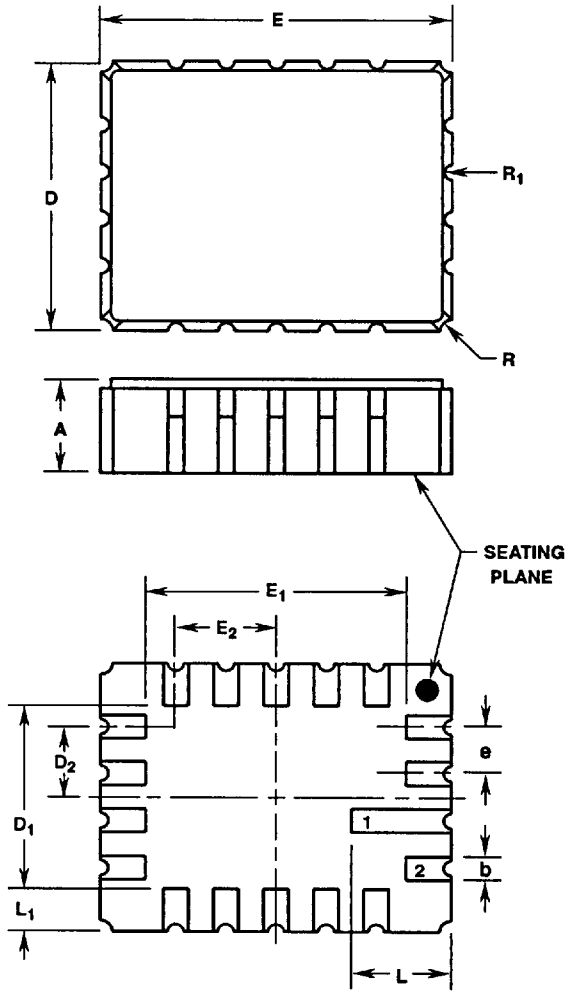








Packaging



18 Pin LCC

18 PIN CERAMIC LEADLESS CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.112	2.34	2.84	-
b	0.020	0.030	0.51	0.76	-
D	0.275	0.295	6.99	7.49	-
D_1	0.175	0.215	4.45	5.46	-
D_2	0.070	0.080	1.78	2.03	-
E	0.340	0.360	8.64	9.14	-
E_1	0.240	0.280	6.10	7.11	-
E_2	0.095	0.105	2.42	2.66	-
e	0.050 BSC		1.27 BSC		-
L	0.085	0.115	2.16	2.92	-
L_1	0.035	0.055	0.89	1.39	-
R	0.007	0.017	0.18	0.43	4
R_1	0.003	0.013	0.08	0.33	4

NOTES:

1. No current JEDEC outline for this package.
2. All exposed metallized areas shall be plated with a minimum of 50 microinches of gold over nickel unless otherwise stated.
3. Metallized castellations shall be connected to the seating plane and extend upward toward top of package.
4. Corner shape (notch, radius, square, etc.) may vary at the manufacturer's option.
5. Unless otherwise specified, a minimum clearance of 0.010 inches (0.25mm) shall be maintained between all metallized areas.
6. Controlling dimension: Inch.
7. Revision 1 dated 6-93.

ELEMENT	PAD	PINS CONNECTED
GATE	A	5
DRAIN	B	1, 2, 3, 4, 16, 17, 18
SOURCE	C	6, 7, 8, 9, 10, 11, 12, 13, 14, 15