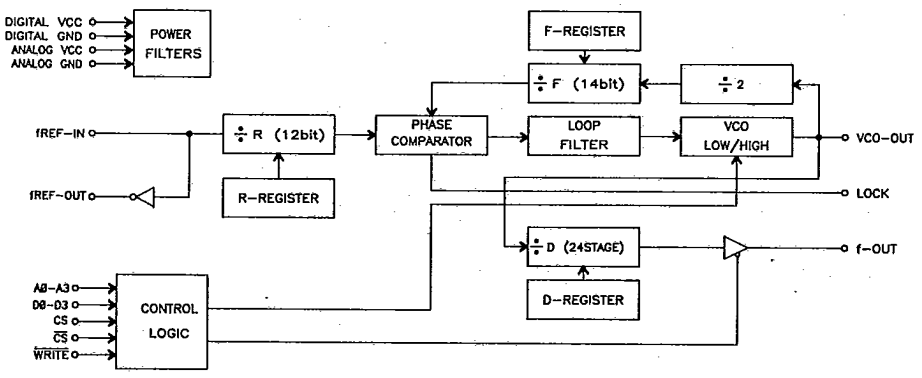
FS-30 DIGITAL FREQUENCY SYNTHESIZER

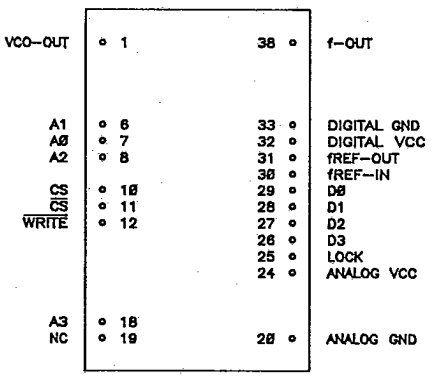
The Analytic Instruments **FS-30** is the first **complete,** easy to use, digitally programmable CMOS frequency synthesizer in a small (2.25" x 1.6") package. Its extremely wide frequency range covers over 9 decades, from .02Hz to over 31 MHz, with more than 27000 steps per decade. Such features as CMOS I/O, single-sided 5V supply, low cost and simple, microprocessor-compatible interface make the **FS-30** the ideal element in any design requiring an accurate, programmable clock.

Features:

- A **complete** synthesizer in one package.
- No external filters or other typical phase-lock loop components required.
- Over nine decade range: .02 Hz to 31 MHz.
- Compatible with any microprocessor, including low cost 4-bit CPUs.
- CMOS inputs and outputs.
- 5 volt supply, - no need to add new voltages to your system.
- Requires only a single, low-cost external crystal or clock oscillator.
- Tri-state output for in-circuit testability or busing of multiple clock sources. Ideal for ATE systems.
- Programmable resolution to 8192 steps/octave.
- Low power, (120mA worst case.)
- Frequency-Lock output indicator.
- Long term stability determined entirely by the external crystal.
- Completely programmable frequency, range and resolution.
- Fast lock time, - typically .1mS/ step for large frequency changes.
- All-digital interface. Simple to use.
- Fully shielded package.



FS-30 DIGITAL FREQUENCY SYNTHESIZER
Figure 1



FS-30
Figure 2

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The Analytic Instruments **FS-30** consists of 4 basic parts:

1. A highly programmable, wide range phase-lock loop running from 10.5 to 31MHz, (high range) or 165-525 KHz (low range.)
2. A 24-stage programmable output frequency divider.
3. Interface control logic.
4. Power supply filtering for high stability and noise reduction.

1. Phase Lock Loop

The phase-lock loop consists of a 12-bit reference divider, a 14-bit feedback divider, and a voltage controlled oscillator (VCO). The VCO output frequency (f_{out}) is

$$f_{out} = F \times (\text{step size}) \text{ and step size} = (2 \times f_{ref}) / R$$

where F is the value programmed in the F-register (range 3 to 16383), R is the value programmed in the R-register, (range 3-4095), and f_{ref} is the reference frequency of the external crystal or clock.

In the high-range of the VCO, the f_{out} range is 10.5 MHz to 31 MHz. In the VCO low range, the f_{out} range is 165 KHz to 525 KHz. Normally, the reference frequency, range and R are set only once, providing a fixed frequency-step size. The F-register is then varied to set the output frequency. For example, a reference frequency of 1Mhz with R=1000 provides a fundamental step of 2x1MHz/1000 = 2 KHz. Varying F from 7500 to 15,000 then provides 2KHz steps from 15 MHz (7500 x 2KHz) to 30 MHz (15,000 x 2 KHz),with 1/7500 = .013% resolution.

The wide choice of values for both R and F means the designer can tailor the output of the **FS-30** to the exact frequency requirements of the system.

2. Output Divider

The VCO output frequency can be further reduced by a factor of 2^D through the programmable 24-stage divider, ($0 <= D <= 23$). Each increment of the D-register divides the output frequency by half. The fundamental range and step-size of the VCO remains fixed by F, R and the reference frequency.

For example, if the previous values are used, (F = 7500 to 15,000, R = 1000, f_{ref} = 1MHz), a setting of D=4 provides an output range of 15MHz/(2^4) to 30MHz/(2^4) = .9375 MHz to 1.875 MHz in 7500 steps of 125 Hz.

3. Interface Control Logic

The **FS-30** has a four-bit address bus, a four-bit data bus, a /write line, and two chip-select lines, CS and /CS.

Truth Table

CS	/CS	/write	
0	0	x	no action
0	1	x	no action
1	1	x	no action
1	0	↓	write data to register at address

PROGRAMMING

		d0	d1	d2	d3	(d0=LSB)
Address 0:	F-register bits	F0	F1	F2	F3	
Address 1:	" "	F4	F5	F6	F7	
Address 2:	" "	F8	F9	F10	F11	
Address 3:	" "	F12	F13	x	x	(d2 and d3 unused)
Address 4:	R-register "	R0	R1	R2	R3	
Address 5:	" "	R4	R5	R6	R7	
Address 6:	" "	R8	R9	R10	R11	
Address 7:	unused					
Address 8:	D-register "	D0	D1	D2	D3	
Address 9:	" "	D4	x	x	Range-bit	

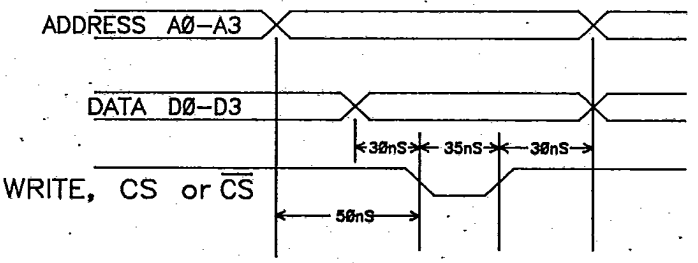
Address 10, 12, 14 = same effect as address 8.

Address 11, 13, 15 = same effect as address 9.

R-register = 3-4095
F-register = 3-16383
D-register = 0-23, (D=24 sets the output to high-impedance state)
Range-bit = 0, VCO high range (10.5 to 31 MHz)
= 1, VCO low range (165 to 525 KHz)

INTERFACE SPECIFICATIONS

Minimum set-up time, address line to /write	: 50 nS
Minimum set-up time, data lines to /write	: 30 nS
Hold time, data or address to /write	: 25 nS
/Write pulse, minimum width	: 35 nS



INTERFACE TIMING SPECIFICATIONS
Figure 3

POWER

The **FS-30** has two power and two ground lines, one pair providing +5V/gnd for digital circuitry, and one pair providing +5V/gnd for the VCO and loop filter. Since the **FS-30** contains on-board power supply filtering, these lines can normally be connected together. However, for minimum phase noise the analog and digital 5V/gnd lines should be supplied separately to prevent digital clock-noise from coupling back into the VCO. Excellent results can be obtained with inexpensive, low-current, 5-volt regulators, such as a 7805, on each supply line.

In any case, good grounding practice and power supply by-pass filtering should be observed.

The digital components of the **FS-30** typically draw 55 mA. However, supply current for CMOS devices varies with the switching frequency. Therefore, power requirements can be reduced somewhat by using the lowest possible reference oscillator frequency, and by using the lowest output divide, (D-register = 23).

The VCO analog circuitry draws approximately the same current over its entire range. Table 1 shows typical performance figures.

External Clock = 4mHz
R = 800

	F=1500	F=3000
D=0	104	118
D=23	98	105

External Clock = 1mHz
R = 200

	F=1500	F=3000
D=0	89	97
D=23	97	110

Current = $I_{DIGITAL}$ + I_{ANALOG} (in mA)
Table 1

TRI-STATE OUTPUT

The output of the **FS-30** may be disabled and set to a high-impedance state by setting the D-register to 24. This allows, for example, automatic test equipment to disable the system clock for forced-node testing. It also allows multiple **FS-30's** to be bused together onto one clock line.

The synthesizer is still active and running while the output is disabled. The VCO-output line is not disabled.

REFERENCE FREQUENCY LIMITS

The loop filter in the phase-lock loop reduces the output pulses of the digital phase detector to a nearly DC control signal into the VCO. The cutoff frequency of this filter is 950 rad/sec, or about 150 Hz. Therefore, the reference frequency as seen by the phase detector, (f_{ref}/R) should be substantially above 150 Hz to prevent reference frequency beats from passing through the filter into the VCO control voltage. The lowest recommended value for f_{ref}/ R is 400 Hz. Higher values provide reduced phase noise and faster lock times.

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LOCK TIME

The lock time for a phase-lock loop is very dependent on the reference frequency, the delta-change in the feedback divider, and the state of the detector at the time of the change. Generally, the **FS-30** locks faster with larger step-frequencies. At 10KHz/step, the **FS-30** typically takes .1mS/step for large delta-F changes.

The LOCK output signal is low when the **FS-30** is unlocked and high when locked. However, a small unlock period is continually present as the loop tracks the oscillator. On the **FS-30,** this is present as an unlock-pulse approximately 500 nS wide at the reference frequency (as seen by the phase detector) of f_{ref}/R.

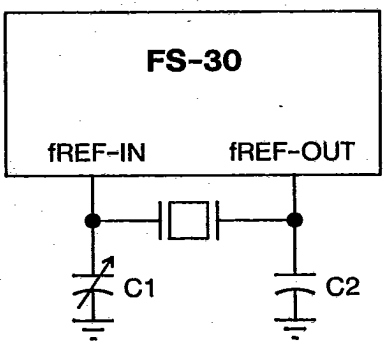
EXTERNAL CRYSTAL

The highest performance of the **FS-30** is achieved by using a CMOS compatible hybrid crystal oscillator for the reference input. It should supply a square wave, swinging between Digital-Gnd and Digital-Vcc, and be DC coupled to fref-IN. fref-OUT should be left unconnected and floating.

A fundamental-mode, parallel-resonant crystal may also be connect as shown in Figure 4. The frequency may be trimmed by varying C1.

In either case, good analog circuit design should be followed. The crystal and the associated components should be as close as possible to fref-IN and fref-OUT, and clock noise on the ground should be minimized.

The long-term stability of the **FS-30** is totally dependent on the long-term stability of the reference oscillator. The designer is free to choose the stability/cost ratio that best fits the application.



CRYSTAL OSCILLATOR
Figure 4

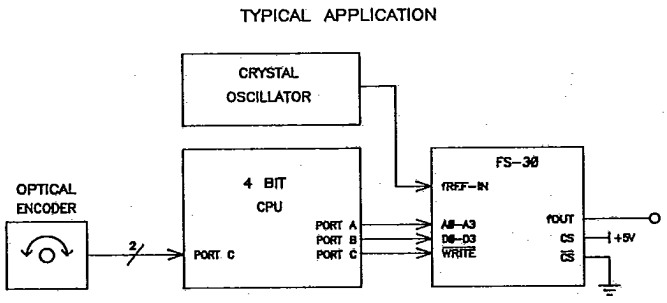
MAXIMUM RATINGS

VCC (analog and digital): 4.75 to 5.25 volt. 5 volts nominal.
Output Current at f_{out} : 25 mA.
Frequency : 30 MHz guaranteed, 31 MHz typical.

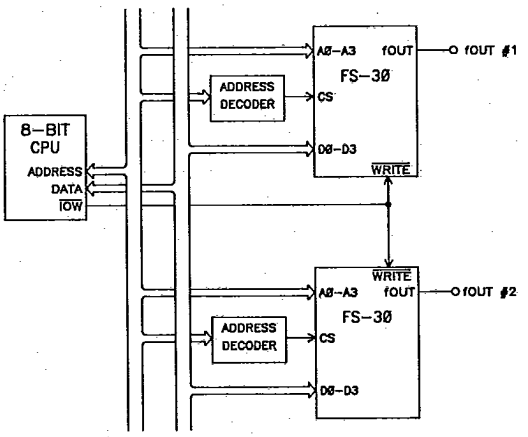
PHYSICAL DIMENSIONS

width: 1.60"
length: 2.25"
height: .50"
pin spacing, length: .10"
pin spacing, width: 1.20"
pin diameter: .020"

TYPICAL APPLICATIONS



ADJUSTABLE SQUARE WAVE GENERATOR
Figure 5



I/O MAPPED FS-30 on an 8-BIT CPU BUS
Figure 6

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