National Semiconductor

December 1989

FSA Series
ASPECT™ Standard Cells and Megacells

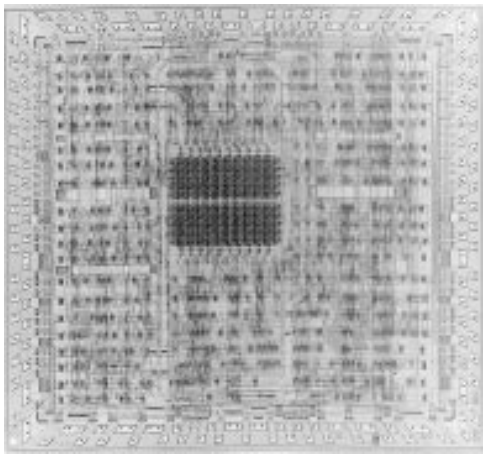
General Description

National Semiconductor offers the first **total solution for digital system design** using the high-performance combination of ECL (Emitter-Coupled Logic) and standard-cell design methodology.

The FSA Series provides a thorough combination of large and small logic, I/O, support cells, and even memory. The FSA Standard Cell Library offers a comprehensive set of 176 system-oriented functions, while the companion FSA Megacell Library offers 29 soft and hard megacells including critical computing engine components such as **embedded memory arrays, ALUs, multipliers, barrel shifters, and floating point units.**

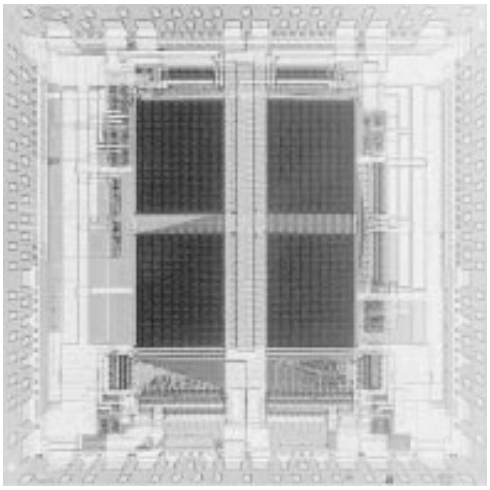
Features

- **Scalable ASPECT** (Advanced Single Poly Emitter Coupled Technology) **process technology provides migration path and state-of-the-art performance**
- Industry-first ECL standard cell and megacell libraries allow **mixed memory and logic up to 25k gates/chip**
- Comprehensive set of 29 megacells, including embedded RAM, and 176 standard cells allows system differentiation
- Typical internal logic performance 170 ps at 225 μA
- Consistent design-tools interface, DA4, runs on popular workstation platforms
- **EDIF-standard backplane** for open design automation methodology
- **Post-place-and-route back-annotation capability** updates emitter follower selection to optimize speed/power
- High-performance packaging technology offers high pin count, low thermal resistance
- Full support for testability



TL/U/10570–1

Photomicrograph of 16 x 16 Multiplier



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Photomicrograph of 128 x 18 3-Port Register File

RRD-B30M115/Printed in U. S. A.

ASPECT Standard Cells and Megacells

For high-end systems design, VLSI improves performance by eliminating chip I/O boundary crossings in the critical path and drastically reducing wire delays. Until recently, gate array and full custom have been the only two ECL VLSI approaches available. The new FSA standard cell methodology from National Semiconductor, based on ASPECT process technology, offers a **high-performance system design solution that approaches full-custom performance and layout efficiency, yet offers semi-custom cost and development time and correct-by-construction design.**

The combination of ASPECT process technology and standard cell methodology achieves integration levels usually associated with CMOS and gate speeds only SSI ECL or GaAs could previously offer. The result can be a 2- to 3-fold system performance improvement over other semicustom design and technology combinations.

FSA-Series cells are the best choice for high-throughput, high-performance applications such as super mini-computers, fiber optic telecommunications, ATE, RISC processors, and many military and aerospace systems.

ASPECT TECHNOLOGY INNOVATIONS

ASPECT 1 is a mature 2.0 μm process which achieves high density and performance with conservative lithography. It resembles a MOS process, utilizing self-aligned (bipolar) transistors, with enhancements over conventional ECL in the use of polysilicon for emitters, bases, collector contacts, and resistors. This polysilicon provides very low parasitic devices and increased packing density.

ASPECT is a scalable process, offering a migration path directly to the next-generation 0.8 μm ASPECT 3 process and beyond. ASPECT 1 performance is outstanding, with operating capabilities at frequencies in excess of 1 GHz. The use of silicided polysilicon for local interconnect allows reduced area to less then 2-3 mil^2 per equivalent gate. Quite simply put, small cell size translates to maximum operating speed.

STANDARD CELL LIBRARY DESCRIPTION

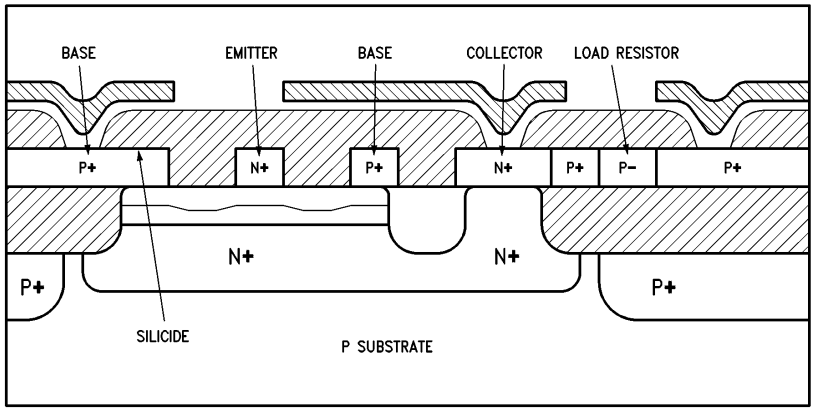
The circuit performance is complemented by the architectural functionality provided by the comprehensive set of standard cells and megacells. Cell complexity varies from a single gate to 20k gates. Standard cells are fixed height cells placed in rows. Power and bias voltage buses in the rows connect by abutment. **The ASPECT 1 standard cells library has a complete collection of 176 unique types.**

Logic gates range from the usual simple functions (buffers, ANDs, ORs, and XORs) to complex OAI (OR-AND-INVERT) gates with up to 21 inputs. A 9-bit XOR gate makes parity generation easy, and OR-XOR gates are geared toward efficient incrementer implementation. **Each of the basic cell types has programmable output drive,** with very low power gates available for use in latch based memories.

Arithmetic functions include full and half adders, carry-look-ahead generators, and Booth adders (muxed input operands with outputs in carry-save format). There is a large variety of multiplexors with up to 8 inputs. Storage elements include latches, registers, and flip-flops, as well as programmable register-latches (ratches). Also available are versions with multiplexed inputs. This reduces a level of logic in many designs, and can also be used to implement serial scan chains for testing.

Input, output, and bidirectional buffers are available which support **100k, 10k, and single- or dual-supply-TTL voltage levels.** Differential inputs and complementary outputs are supported, as well as enabled outputs and 50Ω or 25Ω drive capability.

Most cells have both true and complement outputs available ''free'' as a consequence of ECL design. This allows the designer to easily implement AND functions as NOR gates with inverted input signals (in ECL, NORs are faster, smaller, and consume less power than equivalent ANDs).



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ASPECT 1 Transistor with First Metal Layer

ASPECT Standard Cells and Megacells (Continued)

A selection of differential cells improves the performance of complex arithmetic functions through the use of series-gated circuits of up to three levels. High-power differential and single-ended cells are also provided for speed-critical functions such as clock distribution.

To ensure optimal drive capability while preserving speed and keeping power to a minimum, **emitter-follower selection is performed during back annotation based on place and route data.** The methodology includes five programmable current options for each emitter-follower. Emitter followers are terminated either resistively to V_{TT} ($-2V$) or actively to V_{EE}. In a single-supply environment, a simple mask option can connect all resistive emitter followers through alternate resistors to V_{EE}. Traditional negative voltage ECL power supplies are supported, with or without V_{TT}, as well as mixed TTL/ECL and $+5V$ only TTL.

A HEAD START WITH MEGACELLS AND EMBEDDED MEMORY

The wide selection of SSI and MSI logic functions and I/O options is complemented by a library of soft and hard megacells geared towards CPU, numerical processing, and memory functions. **A single chip can combine standard cells, megacells, and memory.**

Hard megacells are custom-designed functional blocks which provide most of the circuitry for many critical computing components. Wiring delay and area have been minimized since internal interconnect is by abutment of cells where possible. The custom layout makes hard megacells particularly fast, dense, and power thrifty. For example the megacell library includes multi-port register files with 3–5 ns access times.

Soft megacells are configured and tested blocks of standard cells designed to efficiently perform a given macro function. Soft megacells can save design time by providing a kernel on which to establish the chip design. Since soft megacells do not have fixed layouts, the aspect ratio may be chosen to optimize the overall chip area.

One key advantage of National's standard cell methodology using ASPECT process technology is the ability to **incorporate fast embedded memory in with the high-speed logic.** In addition to existing register-file megacells, National is developing a family of reconfigurable single- and multi-port memory megacells, which can be customized per customer request. National can also develop ASIC chips that are mostly memory with some logic, such as a cache RAM.

Contents of Standard Cell and Megacell Libraries

Standard Cells

Generic Type	Count
Buffers	9
AND/OAI Gates	24
OR/NOR Gates	17
XOR Gates	14
Clock-Distribution Cells	11
Decoders, Multiplexors	22
Latches, Muxed Latches	16
Flip Flops (6 with Scan Testability)	17
Arithmetic Function Cells	15
I/O Cells	31

Soft Megacells

ALU32AAM	32-bit binary ALU
ADD32AAM	32-bit binary adder
BLF32AAM	32-bit Boolean function generator
OFO32AAM	32-bit output formatter
OSO32AAM	32-bit single operand sign extender
OST32AAM	32-bit dual operand sign extender
INC32AAM	32-bit binary incrementer
OTC32AAM	32-bit binary two's complementer
ALU64AAM	64-bit binary ALU
ADD64AAM	64-bit binary adder
BLF64AAM	64-bit Boolean function generator
OFO64AAM	64-bit output formatter
OSO64AAM	64-bit single operand sign extender
OST64AAM	64-bit dual operand sign extender
INC64AAM	64-bit binary incrementer
OTC64AAM	64-bit binary two's complementer
STKY64AM	64-bit variable width OR/AND reduction operator
NRM64AAM	64-bit binary normalizer
PEN64AAM	64-bit priority encoder
RWDG1ZAM	64-bit RAM column slice

Hard Megacells

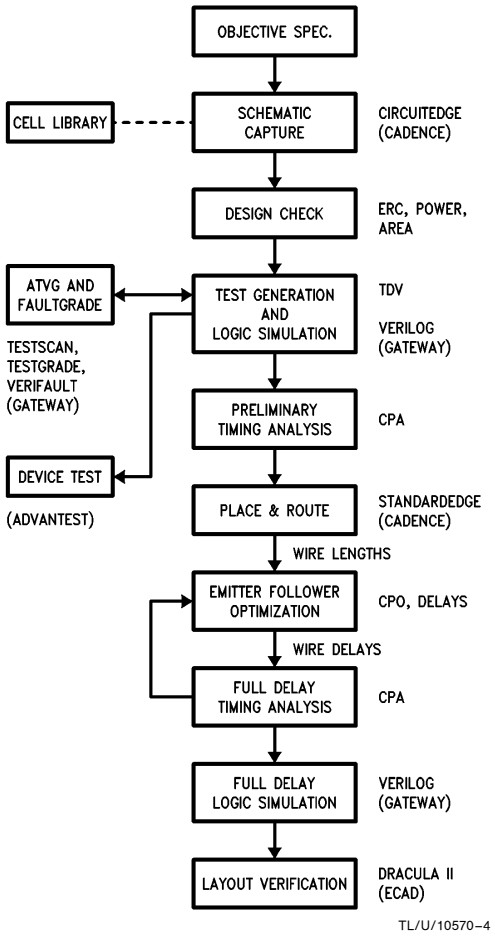
BSH32ZAM	32-bit funnel shifter (64 in 32 out)
BSH64AAM	32-bit barrel shifter, with last shift out bit
MPY16AAM	16-bit mixed mode binary integer multiplier
MPY54APM	54-bit binary mantissa multiplier, pipelineable
MPY54PPM	Two MPY54APMs in a two-stage pipeline
FMPY64AM	64-bit IEEE/DEC format floating point processor (MPY)
FALU64AM	64-bit IEEE/DEC format floating point processor (ALU)
RF6363AM	64 x 36 bit 3-port RAM
RF6366AM	64 x 36 bit 6-port RAM

Step-by-Step Design Methodology

The National standard cells design methodology is based on an EDIF (Electronic Data Interchange Format) backplane. Full hierarchical EDIF data is generated from schematics and compiled into a quick, compact database. This compiled EDIF database drives the remainder of the design process. The EDIF backplane means that the design methodology is not tied to any particular workstation or software. Improved products may be incorporated into the design methodology as they become available. For example, the only software that needs to be rewritten to support a new schematic capture package is the EDIF netlister.

The design tool set is a mixture of proprietary software written in house and standard packages from third party vendors, unified under a proprietary menu-driven shell called DA4. **DA4 provides a simplified, consistent user interface with a uni-directional design flow which guides the user step by step through the design process.**

ASPECT Standard Cells and Megacells (Continued)



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(Software is National proprietary unless otherwise attributed.)

Design Flow

SCHEMATIC CAPTURE

Schematic capture is performed on workstations using standard third-party software. A variety of schematic entry packages is supported, including Cadence CircuitEdge.

DESIGN CHECK

After Schematics are extracted and netlisted, ERC (Electrical Rules Check) is run to check for voltage mismatches, fanout violations and other errors. Power and area estimates are also generated.

LOGIC SIMULATION AND TEST GENERATION

Logic simulation is performed using Gateway's Verilog simulator and Hardware Description Language (HDL). Designs can be modeled initially at the behavioral level; then gate level netlists can be substituted in, module by module, as each schematic is completed. Behavioral models for large, regular structures (like data paths or register banks) may be substituted back in to improve simulation efficiency while the rest of the circuit is debugged at the gate level. **Mixing gate and behavioral models also allows efficient multi-chip system simulation.**

The cell logic models support Verilog version 1.4 timing constructs such as pin to pin delays, and setup and hold checks on registers. The netlister optionally selects full-delay timing models, or faster unit-delay models.

An integrated simulation and test language allowing for waveform descriptions unites National's simulation tools with automated test equipment. Functional test vectors are in TDV (Test Description Vectors) program syntax. TDV is a formatting program which **generates test vectors which can be run on the behavioral model of a design, the gate-level netlist, and actual silicon.**

TDV vectors are table based. Each table entry specifies the input stimulus and the expected response for a test vector. Several input formats are allowed, which may be intermixed: binary, hex, decimal, and octal. Free running clocks can be declared, to reduce the number of table entries required. Gated clocks which conditionally cycle on each vector are also supported. Timing parameters such as clock period, offset, width, and data strobe are adjustable. TDV supports AC device characterization as well as simple pass-fail testing.

The FSA standard cell library **includes cells for implementing scan path designs along with tools and models for performing ATVG** (Automatic Test Vector Generation) of full scan designs. Automatically generated vectors can be expanded and sent to TDV for verification through logic simulation. Support for JTAG (Joint Test Action Group) and BIST (Built-In Self Test) is available.

PLACE & ROUTE AND TIMING ANALYSIS

Static timing analysis is performed using proprietary National software called CPA (Critical Path Analyzer). CPA reports minimum and maximum delay paths through the circuit. It can also be used in ''pipeline mode'' to determine the delays between pipestage registers, as well as set-up and hold requirements of input registers, and propagation delays of output registers.

Timing analysis is performed both before and after place & route. Pre-place & route timing analysis uses estimated wire delays (or may be run without wire delays). CPA results at this stage alert the logic designer to slow critical paths that may require schematic changes.

When the schematic has been captured and simulated, the chip is placed & routed using automatic software. Results of preliminary timing analysis are used to influence placement so that critical net lengths are reduced. Most standard cells are macros consisting of a primitive cell and one or more programmable-current output emitter followers. **Software eliminates emitter followers on dangling outputs so that there is no power or area penalty if an output is left unused.**

After place & route, metal lengths on each layer for routed nets are extracted from the layout. Timing analysis is performed using wire delays computed from the extracted net lengths. CPA reports all paths which are too slow to achieve a specified performance. This information is fed to a **delay optimizer which powers up emitter-followers along the critical paths.** The delay optimizer can optimize speed without regard to power, or can also consider power consequences when selecting emitter-follower sizes. Emitter-follower sizes may also be explicitly selected by the logic designer, if desired. Since each of the five possible emitter-follower options is the same size, **emitter-follower selection may be performed post place & route without disturbing the layout.**

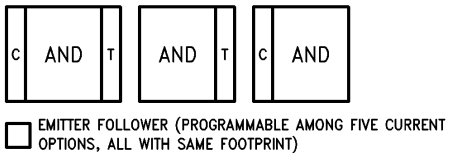
ASPECT Standard Cells and Megacells (Continued)

As a final timing verification, the design may be re-simulated with the logic simulator using accurate delay models and actual wire delays.

LAYOUT VERIFICATION

Before tape-out, the I/O pad ring and power buses are added, and several design checks are performed including power bus drop analysis, LVS (Layout Versus Schematic), and full chip DRC (Design Rule Check).

Layout Representation



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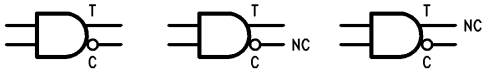
Schematic Representation



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NC = Not Connected (no wasted space or power)

Output Emitter Follower Optimization

Training

National provides training on gate array and standard cell design using DA4 design tools. These comprehensive courses are followed up by consultation and installation services to handle particular platform and design-requirements.

Another course that National offers is ECL principles for designers primarily familiar with CMOS/TTL practices.

Testing

Functional vectors for the tester are in TDV format, and may consist of up to 64k patterns. Optional AC test, ATVG, and fault grading capabilities are available.

The FSA test floor is linked to the manufacturing CIM (Computer Integrated Manufacturing) database. All test data from the fab floor to the final package test are resident in the same database and are under SPC (Statistical Process Control) to assure consistent high quality.

Standard Cell Library Summary

Worst case delay for random path and resistive emitter followers, $T_J = 125°C$, Fanout = 1, Process = worst case, Currents are worst case for primitive cells (excluding emitter followers).

Internal Cells

	IEE (μA)	ITT (μA)	Delay (ps)	Area (mil^2)	Description
BUFFERS, INVERTERS					
BUFAAAAG	301	0	292	4.9	Single-Ended Buffer
BUFADAAG	301	0	256	4.9	Single-Ended to Diff Buffer
BUFAHAAG	1146	0	257	6.1	Single-Ended Buffer with High Power
BUFDBAAG	301	0	209	4.9	Diff to Single-Ended Buffer
BUFDDAAG	302	0	200	4.9	Diff Buffer
BUFDDHAG	1148	0	190	6.1	Diff Buffer, High Speed
BUFHDAAG	2000	0	268	9.7	Super High Drive Diff Buffer (1500 μA)
BUFHHAAG	2014	0	304	8.5	Super High Drive Buffer (1500 μA)
REFHLAAG	301	0	—	3.6	HIGH/LOW Level Generator
GATES					
AND2AAAG	469	0	359	8.5	2-In AND/NAND
AND2ALAG	167	0	517	6.1	2-In AND/NAND, Low Power
AND2HAAG	1312	0	306	9.7	2-In AND/NAND with High Power
AND2HDAG	1146	0	167	9.7	Diff 2-In AND/NAND, High Speed
AND3HDAG	1144	0	174	9.7	Diff 3-In AND/NAND, High Speed
AND4AAAH	1238	686	515	20.7	4-In AND/NAND
NOA4HAAG	1312	0	290	10.9	3-In NOR into a 2-In AND/NAND, High Power
OAI21AAG	468	0	415	10.9	2-Wide 1/4 In OR/AND-Invert
OAI22AAG	468	0	396	8.5	2-Wide 1/2 In OR/AND-Invert
OAI22LAG	334	0	704	7.3	Low Power 2-Wide 2/2 In OR/AND-Invert
OAI24AAG	468	0	375	12.2	2-Wide 4/4 In OR/AND-Invert
OAI24LAG	334	0	616	10.9	Low Power 2-Wide 4/4 In OR/AND-Invert
OAI26AAG	602	0	383	15.8	2-Wide 6/6 In OR/AND-Invert
OAI26LAG	334	0	681	14.6	Low Power 2-Wide 6/6 In OR/AND-Invert
OAI27AAH	601	0	389	18.2	2-Wide 7/7 In OR/AND-Invert
OAI28AAH	601	0	393	20.7	2-Wide 8/8 In OR/AND-Invert
OAI2AAAG	468	0	365	8.5	2-Wide 2/2 In OR/AND-Invert
OAI41ZCH	602	930	399	18.2	4-Wide 3/3/3/3 In OR/AND-Invert
OAI42AAH	1237	686	574	26.7	4-Wide 2/2/3/4 In OR/AND-Invert
OAI43AAH	1236	686	629	26.7	4-Wide 3/3/3/4 In OR/AND-Invert
OAI44AAH	1236	686	574	26.7	4-Wide 2/3/4/4 In OR/AND-Invert
OAI46AAH	1236	686	680	30.4	4-Wide 4/4/4/6 In OR/AND-Invert
OAI55AAH	1536	721	732	34.0	5-Wide 5/4/4/4/2 In OR/AND-Invert
OAI66AAH	1702	721	571	37.7	6-Wide 6/5/4/3/2/1 In OR/AND-Invert
OR02AAAG	301	0	297	6.1	2-In OR/NOR
OR02ALAG	167	0	413	6.1	2-In OR/NOR, Low Power
OR02DAAG	301	0	269	6.1	2-In OR with Diff Output
OR02HAAG	1146	0	274	7.3	2-In OR/NOR, High Power

Standard Cell Library Summary

Worst case delay for random path and resistive emitter followers, T_J = 125°C, Fanout = 1, Process = worst case, Currents are worst case for primitive cells (excluding emitter followers). (Continued)

Internal Cells (Continued)

	IEE (μA)	ITT (μA)	Delay (ps)	Area (mil²)	Description
GATES (Continued)					
OR02HDAG	1146	0	229	7.3	Diff 2-In OR/NOR, High Speed
OR03AAAG	301	0	301	7.3	3-In OR/NOR
OR03ALAG	167	0	421	6.1	3-In OR/NOR, Low Power
OR03HAAG	1146	0	280	7.3	3-In OR/NOR, High Power
OR03HDAG	1146	0	238	7.3	Diff 3-In OR/NOR, High Speed
OR04AAAG	301	0	306	7.3	4-In OR/NOR
OR04ALAG	167	0	429	6.1	4-In OR/NOR, Low Power
OR04HAAG	1146	0	282	8.5	4-In OR/NOR, High Power
OR04HDAG	1146	0	247	8.5	Diff 4-In OR/NOR, High Speed
OR05AAAG	301	0	311	7.3	5-In OR/NOR
OR06AAAG	301	0	316	8.5	6-In OR/NOR
OR07AAAG	301	0	320	9.7	7-In OR/NOR
OR08AAAG	301	0	325	9.7	8-In OR/NOR
XOR2AAAG	468	0	344	8.5	2-In Exclusive OR/NOR
XOR2ALAG	167	0	494	6.1	2-In Exclusive OR/NOR, Low Power
XOR2BAAG	468	0	487	9.7	2-In Exclusive OR/NOR with 3-In OR on LOW Level
XOR2CAAG	468	0	478	9.7	2-In Exclusive OR/NOR with 2-In OR on LOW Level
XOR2DAAG	301	0	280	8.5	2-In Exclusive OR/NOR Single-Ended In, Diff OUT
XOR2EAAG	468	0	541	13.4	2-In EXCL OR/NOR with 3-In OR on Both Levels
XOR2FAAG	468	0	496	9.7	2-In Exclusive OR/NOR with 4-In OR on LOW Level
XOR2HDAG	1146	0	185	10.9	Diff 2-In Exclusive OR/NOR, High Speed
XOR3AAAH	937	610	559	20.7	3-In Exclusive OR/NOR (VET)
XOR3HDAG	1145	0	184	14.6	Diff 3-In Exclusive OR/NOR, High Speed
XOR4AAAH	1572	610	559	29.2	4-In Exclusive OR/NOR
XOR4HDAG	3434	1596	396	29.2	Diff 4-In Exclusive OR/NOR, High Speed
XOR6HDAG	3429	1596	386	37.7	Diff 6-In Exclusive OR/NOR, High Speed
XOR9AAAH	3273	1829	946	69.3	9-In Exclusive OR/NOR (Parity Network) (VET)
CLOCK DISTRIBUTION CELLS					
DLYDIAAG	5349	0	3354	83.9	Programmable Delay Line
DLYRIAAG	5349	0	808	86.3	Programmable Clock Generator
DLYSIAAG	4450	0	1134	93.6	Setable Delay String
EF0I0I0G	167	0	30	3.6	Level-Shifter with 125 μA Active Tail
EF0I0J0G	333	0	20	3.6	Level-Shifter with 250 μA Active Tail
EF0I0K0G	599	0	15	4.9	Level-Shifter with 450 μA Active Tail
EF0I0L0G	861	0	13	4.9	Level-Shifter with 650 μA Active Tail
EF0I0M0G	1134	0	12	4.9	Level-Shifter with 850 μA Active Tail
EF0I0N0G	1975	0	12	8.5	Level-Shifter with 1.5 mA Active Tail
OR02MAAG	1717	0	372	8.5	2-In OR Mode Driver for RAT3I/4I Cells
OR0SH0YG	3382	0	387	14.6	2-In NOR Scan Clock Driver, High Power

Standard Cell Library Summary

Worst case delay for random path and resistive emitter followers, T_J = 125°C, Fanout = 1, Process = worst case, Currents are worst case for primitive cells (excluding emitter followers). (Continued)

Internal Cells (Continued)

	IEE (μA)	ITT (μA)	Delay (ps)	Area (mil²)	Description
DECODERS, MULTIPLEXORS					
DEC24A0G	1377	0	258	21.9	2:4 Decoder
DEC24EAG	1673	0	258	24.3	2:4 Decoder w/Enable (Demultiplexor)
MUX2AAAG	468	0	477	8.5	2:1 Multiplexor
MUX2EAAH	602	0	508	12.2	2:1 Multiplexor with Enable
MUX2HAAG	301	0	344	8.5	2:1 Mux with Default HIGH, Selects are Pre-Dec
MUX2HDAG	1146	0	271	10.9	Diff 2:1 Multiplexor, High Speed
MUX2LAAG	301	0	415	8.5	2:1 Mux with Default LOW, Selects are Pre-Dec
MUX2NAAG	301	0	429	8.5	2:1 Multiplexor with 2-In NOR on Select
MUX3HAAG	301	0	404	12.2	3:1 Mux with Default HIGH, Selects are Pre-Dec
MUX3LAAG	301	0	494	12.2	3:1 Mux with Default LOW, Selects are Pre-Dec
MUX4HAAG	301	0	466	15.8	4:1 Mux with Default HIGH, Selects are Pre-Dec
MUX4HDAG	1145	0	232	17.0	Diff 4:1 Multiplexor, High Speed
MUX4LAAG	301	0	573	15.8	4:1 Mux with Default LOW, Selects are Pre-Dec
MUX5HAAG	301	0	529	14.6	5:1 Mux with Default HIGH, Selects are Pre-Dec
MUX5LAAG	301	0	649	19.4	5:1 Mux with Default LOW, Selects are Pre-Dec
MUX6HAAG	301	0	595	17.0	6:1 Mux with Default HIGH, Selects are Pre-Dec
MUX6LAAG	301	0	721	17.0	6:1 Mux with Default LOW, Selects are Pre-Dec
MUX7HAAG	301	0	664	20.7	7:1 Mux with Default HIGH, Selects are Pre-Dec
MUX7LAAG	301	0	786	20.7	7:1 Mux with Default LOW, Selects are Pre-Dec
MUX8HAAG	301	0	736	23.1	8:1 Mux with Default HIGH, Selects are Pre-Dec
MUX8LAAG	301	0	846	23.1	8:1 Mux with Default LOW, Selects are Pre-Dec
ORM6HAAG	1144	0	322	14.6	6/1 OR Mux, High Power
LATCHES, MUX LATCHES					
LAT2AAAH	301	342	411	8.5	Latch with 2-In OR on Data (VET)
LAT2DAAH	468	342	477	14.6	Latch with 2-In OR on Data, also Has Set/Reset
LAT2EAAH	301	342	473	10.9	Latch with 2-In OR Enable AND Master Reset (VET)
LAT2FAAH	469	342	479	13.5	Latch with 2-In OR on Data AND EN, also Has S/R
LATAAAAH	301	342	406	8.5	Latch
LATALAAG	167	342	770	7.3	Low Power Latch
LATDHAAG	1479	0	369	13.4	Latch, High Power w/Diff Clock
LATSRAAH	468	342	472	13.4	Latch with Set/Reset
MXL2AAAH	301	342	545	9.7	Latch with 2:1 Mux on Input, Pre-Dec Selects
MXL2LAAG	168	342	1006	9.7	Low Power 2:1 Mux Latch
MXL3AAAH	301	342	623	12.2	Latch with 3:1 Mux on Input, Pre-Dec Selects
MXL4AAAH	301	342	704	14.6	Latch with 4:1 Mux on Input, Pre-Dec Selects
MXL5AAAH	301	342	783	17.0	Latch with 5:1 Mux on Input, Pre-Dec Selects
MXL6AAAH	301	342	863	19.4	Latch with 6:1 Mux on Input, Pre-Dec Selects
MXL7AAAH	301	342	944	21.9	Latch with 7:1 Mux on Input, Pre-Dec Selects
RAT5LAAI	602	873	489	20.7	Scan Latch (Has VSB Level Output) (VET)

Standard Cell Library Summary

Worst case delay for random path and resistive emitter followers, T_J = 125°C, Fanout = 1, Process = worst case, Currents are worst case for primitive cells (excluding emitter followers). (Continued)

Internal Cells (Continued)

	IEE (μA)	ITT (μA)	Delay (ps)	Area (mil²)	Description
FLIP-FLOPS					
FDSRAAAG	886	0	816	25.5	Low Power Set/Reset Flip-Flop
FFD22AAH	769	685	564	23.1	D-Flip Flop with 2-In OR on Data AND Clk, & S/R
FFD2SAAH	769	685	561	23.1	D-Flip Flop with 2-In OR on Data, Has Set/Reset
FFDAAAAI	602	685	481	14.6	D-Flip Flop with True Clock (Has VSB Level Out)
FFDAHDAG	1680	0	344	18.2	Diff D-Flip Flop, High Speed
FFDCDAAG	937	0	424	14.6	D-Flip Flop with Diff Clock
FFDDDAAG	739	0	366	12.2	D-Flip Flop with Diff Clock AND Data
FFDRAAAH	602	685	559	15.8	D-Flip Flop with Reset
FFDSRAAH	769	685	562	23.1	D-TYPE Flip Flop with Set/Reset
FFJRAAAH	1070	685	594	26.7	JK-Flip Flop with Reset
FFJSRAAH	1237	685	597	30.4	JK-Flip Flop with Set/Reset
RAT2AAAH	602	685	476	20.7	2:1 Mux Register with Latch
RAT2LAAG	939	685	863	19.4	Low Power 2:1 Mux Register with Latch
RAT3IIIG	937	0	474	25.5	3:1 Mux Register with Latch, No VTT
RAT4IIIG	936	0	475	28.0	4:1 Mux Register with Latch, No VTT
RAT5RAAI	603	873	523	20.7	Scan Register (Has VSB Level Output)
RAT6AAAJ	603	873	498	25.5	Standard Ratch (Has VSB Level Output)
ARITHMETIC FUNCTIONS					
BAD4DZ0G	1944	0	276	32.8	Booth Adder, Diff Out
CLA1AAAG	2047	0	826	24.3	1-Bit Carry Lookahead Adder with True G
CLAD4AAG	2218	0	730	25.5	Diff In, Carry Lookahead Adder with True G
CLADAA0G	1644	0	766	20.7	Diff In, Single-Ended Out Carry Lookahead Adder
CLG7AZ0H	2099	520	475	20.7	Carry Lookahead Gen for 3rd Stage (4/3/2/1 OAI)
CLG9AZ0H	2215	520	475	26.7	Carry Lookahead Gen for 4th Stage (5/4/3/2/1 OAI)
CLGP1AAG	739	0	336	8.5	1-Bit Generate/Propagate Generator
CLGP40AG	10049	342	445	80.2	4-Bit Generate/Propagate Generator
CLGP50AG	11819	342	376	92.4	Carry Lookahead Gen/Propagate with 3 Carry Outs
FADAAAAG	1573	0	1004	25.5	Full Adder
FADDDA0G	1477	0	337	25.5	Diff Full Adder
FANDDA0G	1310	1218	338	24.3	Diff Full Adder with 2-In NOR
HADAAAAG	801	0	496	12.2	Half Adder
HADDDA0G	1144	0	321	14.6	Diff Half Adder
HANDDA0G	1310	0	303	17.0	Diff Half Adder with 2-In NOR

Standard Cell Library Summary

Worst case delay for random path and resistive emitter followers, T_J = 125°C, Fanout = 1, Process = worst case, Currents are worst case for primitive cells (excluding emitter followers). (Continued)

Input/Output Cells

	IEE (μA)	ITT (μA)	Delay (ps)	Area (mil²)	Description
INPUT BUFFERS					
IBF1AAAG	373	0	295	40.1	Input Buffer
IBFDAAAG	373	0	181	80.2	Diff Input Buffer
IBFDDAAG	373	0	171	80.2	Diff In/Out Input Buffer
IBFDDHAG	1219	0	150	80.2	HIGH Power Diff In/Out Input Buffer
IBFDHAAG	1219	0	181	80.2	HIGH Power Diff Input Buffer
IBFHAAAG	1218	0	309	40.1	HIGH Power Input Buffer
OUTPUT BUFFERS					
OBF1AZBG	4932	0	875	64.8	True/Complement F100K ECL Output Buffer
OBF1AZCG	4932	0	844	32.4	Complement F100K ECL Output Buffer
OBF1AZTG	4932	0	875	32.4	True F100K ECL Output Buffer
OBF1KZBG	3816	0	808	64.8	True/Comp Output Buffer, 10K Levels
OBF1KZCG	3816	0	905	32.4	Comp Output Buffer, 10K Levels
OBF1KZTG	3816	0	808	64.8	True Output Buffer, 10K Levels
OBF25ZCG	13098	0	1054	45.4	25Ω Comp Output with HI-Z Enable
OBF2AZBG	4933	0	869	64.8	2-In OR/NOR Output Buffer
OBF2AZCG	4933	0	886	32.4	2-In NOR Output Buffer
OBF2AZTG	4933	0	869	32.4	2-In OR Output Buffer
OBF2SZBG	30900	0	1230	64.8	2-In OR/NOR Out Buf, Term On-Chip
OBF2SZCG	17900	0	1280	32.4	2-In NOR Out Buf, Term On-Chip
OBF2SZTG	17900	0	1270	32.4	2-In OR Out Buf, Term On-Chip
I/O BUFFERS					
IOB2AAAH	7757	0	280	46.8	Bidi 2-In NOR Output Buffer

	IEE (μA)	ITTL (μA)	IET (μA)	Delay (ps)	Area (mil²)	Description
TTL CELLS						
BUF1TCZG	701	1127	0	3533	25.9	ECL-TTL X-Lating Buffer (2 Supply)
BUFSTCZG	2195	—	926	4611	25.9	ECL-TTL X-Lating Buffer (1 Supply)
IBFTAIIG	563	539	0	990	40.1	TTL-ECL X-Lating Input Buf (2 Supply)
IBFTSAAG	539	—	0	211	40.1	TTL-ECL X-Lating Input Buf (1 Supply)
IBFTSHFG	1611	—	0	154	40.1	TTL-ECL X-Lating Input Buf High Pwr
IOB1TIIG	2336	3513	0	990	62.4	Bidi ECL-TTL TRI-STATE® Buf (2 Supply)
IOBSTAAG	3503	—	2152	211	61.0	Bidi ECL-TTL TRI-STATE Buf (1 Supply)
OBF1TCZF	1435	2358	0	2294	45.4	ECL-TTL X-Lating Output Buf (2 Supply)
OBF1TTZG	1435	2877	0	2503	48.2	ECL-TTL TRI-STATE Output Buf (2 Supply)
OBFSTCZG	2917	—	2250	3842	45.4	ECL-TTL X-Lating Output Buf (1 Supply)
OBFSTTZG	2918	—	2152	4108	45.4	ECL-TTL TRI-STATE Output Buf (1 Supply)

Standard Cell Library Summary

Worst case delay for random path and resistive emitter followers, $T_J = 125°C$, Fanout = 1, Process = worst case, Currents are worst case for primitive cells (excluding emitter followers). (Continued)

Input/Output Cells (Continued)

	IEE (μA)	ITT (μA)	Delay (ps)	Area (mil^2)	Description
EMITTER FOLLOWERS					
EF0000IG	167	0	36	4.9	Active Emitter Follower with 125 μA Tail
EF0000JG	310	0	33	4.9	Active Emitter Follower with 250 μA Tail
EF0000KG	560	0	22	4.9	Active Emitter Follower with 450 μA Tail
EF0000LH	811	0	17	4.9	Active Emitter Follower with 650 μA Tail
EF0000MH	1064	0	15	4.9	Active Emitter Follower with 850 μA Tail
EF0000NG	1975	0	13	9.7	Active Emitter Follower with 1.5 mA Tail
EF0000YG	1035	0	7	3.6	Active Emitter Follower with 850 μA Tail
EF000CAG	0	342	14	3.6	Resistive Emitter Follower with 125 μA Tail
EF000CBG	0	616	14	3.6	Resistive Emitter Follower with 225 μA Tail
EF000CCG	0	894	12	3.6	Resistive Emitter Follower with 325 μA Tail
EF000CDG	0	1170	13	3.6	Resistive Emitter Follower with 425 μA Tail
EF000CEG	0	2323	13	3.6	Resistive Emitter Follower with 850 μA Tail
EF000CFG	0	3954	16	4.9	Resistive Emitter Follower with 1.5 mA Tail

Packaging

CERAMIC (HERMETIC) PACKAGING

National has a family of **ceramic packages with low thermal resistance and high bandwidth supporting a wide range of pin counts.** Two body types are available: PGAs (Pin Grid Arrays) on 0.100″ pin grid and LDCCs (Leaded Chip Carriers) at 0.025″ and 0.050″ lead pitch.

National offers **custom package design services** if a special package type is required. Experienced package designers are available and CAD systems are in place to expedite the design.

PLASTIC PIN GRID ARRAYS

National has developed a **proprietary high performance, low thermal resistance, plastic pin grid array technology.** This technology couples multilayer pc board technology for die substrate with plastic encapsulation technology and CuW heat spreaders to produce a high performance line of plastic packages.

TAPEPAK

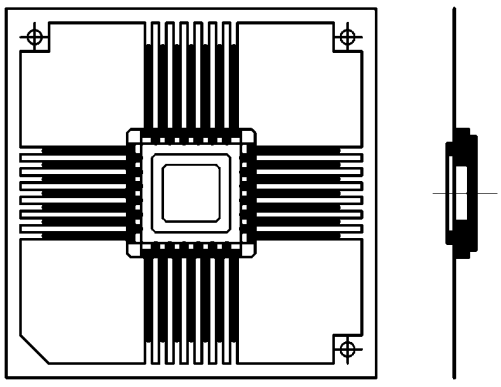
National's **tapepak technology** can be applied to the FSA cell library for high lead count, fine pitch, surface mount packaging at low costs.

CHIP ON TAPE AND MULTICHIP SUBSTRATE PACKAGING

For the ultimate in lead count and density, National offers a **complete solution for TAB** (Tape Automated Bonding) on multilayer ceramic substrate. ILB (Inner Lead Bond) pitch of down to 0.003″ will be available and outer lead bond pitch can be equal to ILB. National can provide chip on tape or a complete module.

Package Options as of 6/89

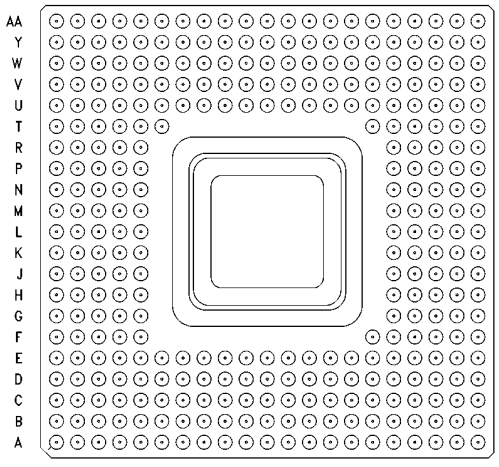
Pin Count	PGA	LDCC
24		Y
28		Y
84	Y	
109	Y	
116		Y
132	Y	Y
156	Y	
164		Y
169	Y	
172		Y
173	Y	
301	Y	
323	Y	



TL/U/10570–7

28-Pin Flatpak

Packaging (Continued)



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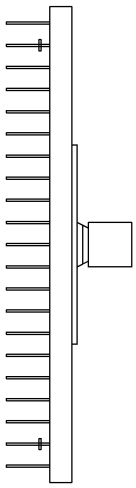

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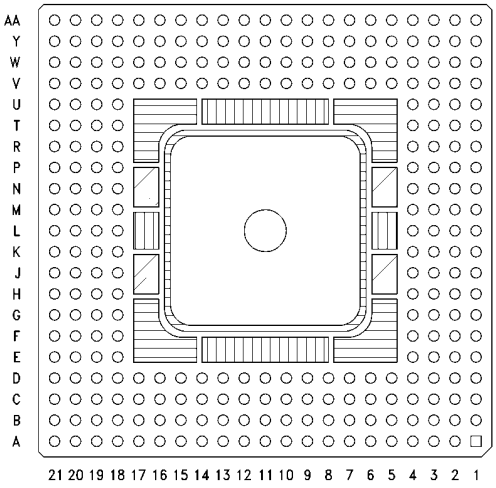
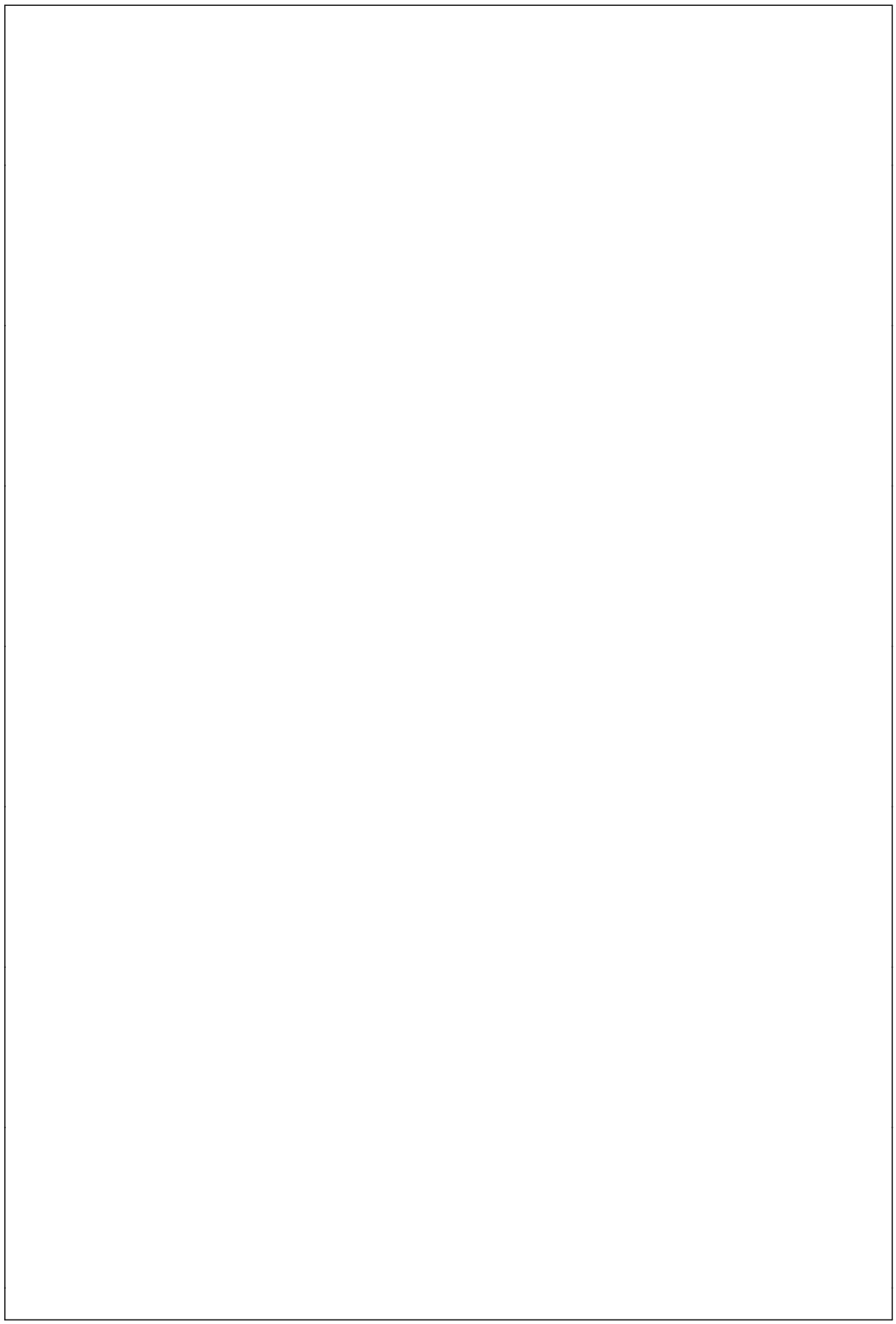


TL/U/10570–10

323-Pin Ceramic Pin Grid Array



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