LOW VOLTAGE, HIGH SPEED GMSK MODEM
4 kbps to 40 kbps

FEATURES

- **MX•COM MX'D SIGNAL CMOS**
- **FULL- OR HALF-DUPLEX OPERATION**
- **DATA RATES FROM 4KBPS TO 40KBPS**
- **SELECTABLE BT: 0.3 OR 0.5**
- **LOW VOLTAGE OPERATION**
  3 TO 5.5 V
- **LOW POWER USAGE**
- **LOW PIN COUNT**
- **MEETS RCR STD-18 (JAPAN)**

APPLICATIONS

- **PORTABLE WIRELESS DATA**
  - **CELLULAR DIGITAL PACKET DATA (CDPD)**
  - **MOBITEX* MOBILE DATA SYSTEM**
- **DATA FOR GPS/DIFFERENTIAL GPS**
- **WIRELESS BAR CODE READERS**
- **WIRELESS LANS**

MX589J
24 pin CDIP

MX589DW
24 pin SOIC

Description

The MX589 is a single-chip synchronous Modem designed for wireless data applications. Employing Gaussian Minimum Shift Keying (GMSK) baseband modulation, the MX589 features a wide range of available data rates: 4,000 to 40,000 bits per second.

The data rate and choice of BT (0.3 or 0.5) are pin-programmable to provide for different system requirements.

The TX and RX digital data interfaces are bit serial, synchronized to TX and RX data clocks generated by the modem. Separate TX and RX Powersave inputs allow full or half-duplex operation. RX input levels can be set by a suitable a.c. and d.c. level adjusting circuit built with external components around an on-chip RX input amplifier.

Acquisition, lock and hold of RX data signals is made easier and faster by the use of RX Control Inputs to clamp, detect and/or hold input data levels and can be set by the µProcessor as required.

The RX S/N output gives an indication of the quality of the received signal.

The MX589 features a mixed signal CMOS process that offers considerably lower current drain than DSP technology. For data rates up to 20kbps, drain is typically 1.5mA at 3V, and for data rates up to 40kbps at 5V, it is typically 4.0mA.

The MX589 is available in 24-pin SOIC and CDIP packages.

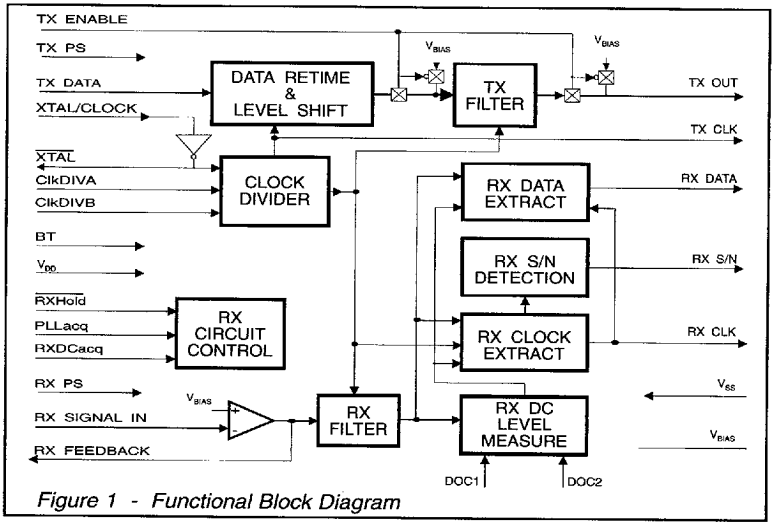
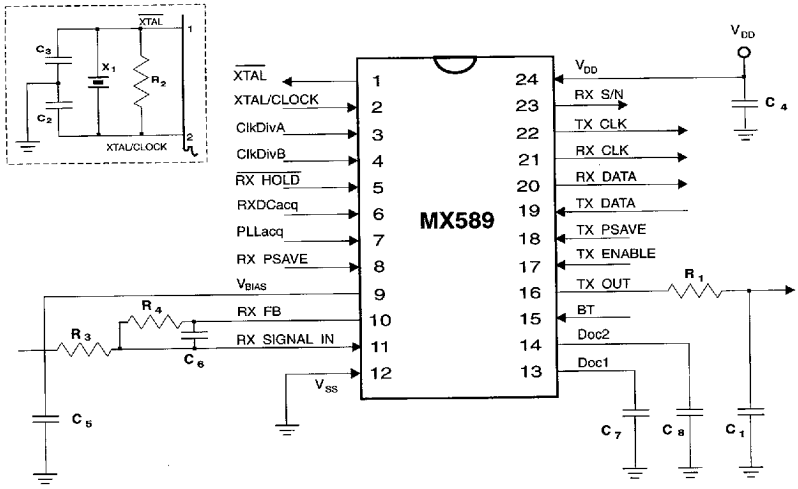


Figure 1 - Functional Block Diagram

** MOBITEX is a registered trademark of Swedish Telecom.*

Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the "$\overline{\text{Xtal}}$" pin left unconnected. Note that operation of the MX589 without a suitable Xtal or clock input may cause device damage.
3 4	**ClkDivA:** These two logic level inputs control the internal clock divider and hence the transmit **ClkDivB:** and receive data rate. See Table 1.
5	**$\overline{\text{RX Hold}}$:** A logic "0" applied to this input will 'freeze' the Clock Extraction and Level Measurement circuits unless they are in 'acquire' mode.
6	**RXDCacq:** A logic "1" applied to this input will set the RX Level Measurement circuitry to the 'acquire' mode.
7	**PLLacq:** A logic "1" applied to this input will set the RX Clock Extraction circuitry to 'acquire' mode (see Table 2).
8	**RX PSAVE:** A logic "1" applied to this input will powersave all receive circuits except for RX CLK output (which will continue at the set bit-rate) and cause the RX Data and RX S/N outputs to go to a logic "0".
9	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to V_{SS} by a capacitor mounted close to the pin.
10	**RX FB:** The output of the RX Input Amplifier/The input to the RX Filter.
11	**RX Signal In:** The input to RX input amplifier.
12	**V_{SS}:** Negative supply rail. Signal ground.
13 14	**Doc1:** Connections to the RX Level Measurement Circuitry. A capacitor should be **Doc2:** connected from each pin to V_{SS}.
15	**BT:** A logic level to select the modem BT (the ratio of the TX Filter's -3dB frequency to the Bit-Rate). A logic "1" sets the modem to a BT of 0.5, a logic "0" to a BT of 0.3.
16	**TX Out:** The TX signal output from the MX589 GMSK Modem.
17	**TX Enable:** A logic "1" applied to this input enables the transmit data path through the TX Filter to the TX Out pin. A logic "0" will put the TX Out pin to V_{BIAS} via a high impedance.
18	**TX PSAVE:** A logic "1" applied to this input will powersave all transmit circuits except for the TX Clock.
19	**TX Data:** The logic level input for the data to be transmitted. This data should be synchronous with TX CLK.
20	**RX Data:** A logic level output carrying the received data, synchronous with RX CLK.
21	**RX CLK:** A logic level clock output at the received data bit-rate.
22	**TX CLK:** A logic level clock output at the transmit-data rate.
23	**RX S/N:** A logic level output which may be used as an indication of the quality of the received signal.
24	**V_{DD}:** Positive supply rail. A single +5 volt power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin.



Component	Value	Tolerance	Component	Value	Tolerance
R_1	Note 1	±5%	C_3	Note 5	
R_2	1.0MΩ	±10%	C_4	0.1µF	±20%
R_3	Note 2	±10%	C_5	1.0µF	±20%
R_4	100kΩ	±10%	C_6	22.0pF	±20%
C_1	Note 1	±10%	C_7	Note 4	
C_2	Note 5		C_8	Note 4	
			X_1	Note 3	

Figure 2 - External Components

Notes

1. The RC network formed by R_1 and C_1 is required between the TX Out pin and the input to the modulator. This network, which can form part of any d.c. level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C_1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

   The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:

   BT of 0.3 = 0.34/bit rate (bits/second)
   BT of 0.5 = 0.22/bit rate (bits/second)
   with suitable values for common bit rates being:

		R_1	C_1
8000 bps	BT = 0.3	91.0kΩ	470pF
4800 bps	BT = 0.5	100kΩ	470pF
9600 bps	BT = 0.5	47.0kΩ	470pF
19,200 bps	BT = 0.5	22.0kΩ	470pF
32,000 bps	BT = 0.3	47.0kΩ	220pF
32,000 bps	BT = 0.5	47.0kΩ	150pF
38,400 bps	BT = 0.3	47.0kΩ	180pF
38,400 bps	BT = 0.5	47.0kΩ	120pF

   Note that in all cases the value of R_1 should not be less than 20.0 kΩ, and that the calculated value of C_1 includes calculated parasitic capacitances.

2. R_3, R_4 and C_6 form the gain components for the RX Input signal. R_3 should be chosen as required by the signal input level.

3. The MX589 can operate correctly with Xtal/Clock frequencies between 1.0MHz and 6.5MHz (see Table 1). Operation of this device without a Xtal or Clock input may cause device damage.

4. C_7 and C_8 should both be 15.0nF for a data rate of 8kbps, and inversely proportional to the data rate for other data rates, e.g. 30.0nF at 4kbps, 3.0nF at 40kbps.

5. The values chosen for C_2 and C_3, including strays, should be suitable for the frequency of X1 and the supply voltage:

   5V $C_2 = C_3 = 33$pF at 1MHz falling to 18pF at 6.5MHz
   3V $C_2 = C_3 = 33$pF at 1MHz falling to 18pF at 5MHz

   The ESR of X1 should be less than 2kΩ at 1 MHz falling to 150Ω at the maximum frequency.

Application Information

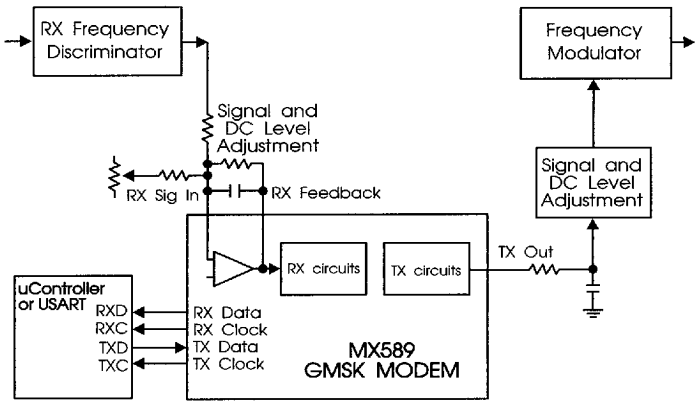


Figure 3 - External Signal Paths

Clock Oscillator and Dividers

The TX and (nominal) RX data rates are determined by division of the frequency present at the Xtal pin, which may be generated by the on-chip Xtal oscillator or derived from an external source. Any Xtal/clock frequency in the range 1.0 to 5.0 MHz for V_{DD}=3.0V, or 1.0 to 6.5 MHz for V_{DD}=5.0V may be used, depending on the desired data rate.

The division ratio is controlled by the logic level inputs on ClkDivA/B (pins 3 & 4), and is shown in the table below - together with an indication of how various 'standard' data rates may be derived from common µP Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal/clock Frequency}}{\text{Division Ratio (Clk DivA/B)}}$$

Pin 3	Pin 4	Division Ratio	Xtal/Clock Frequency (MHz)			
			4.096	4.9152	2.048	2.4576
0	0	128	32kbps	38.4kbps	16 kbps	19.2 kbps
0	1	256	16 kbps	19.2 kbps	8 kbps	9.6 kbps
1	0	512	8 kbps	9.6 kbps	4 kbps	4.8 kbps
1	1	1024	4 kbps	4.8 kbps	-	-

Table 1 - Xtal/Clock Frequencies and Corresponding Data Rates

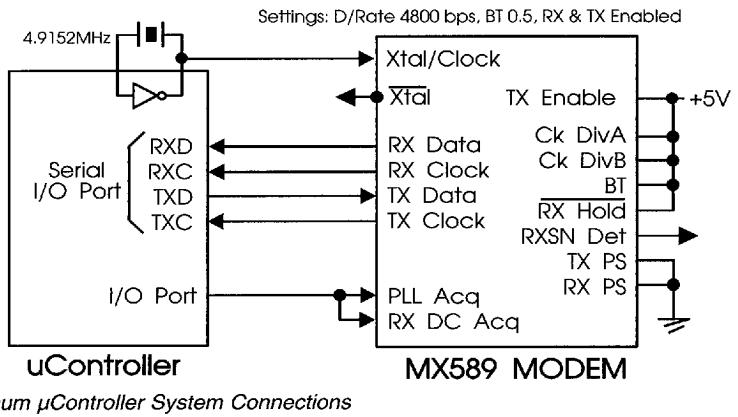


Figure 4 - Minimum µController System Connections

Application Information .....

RX Signal Path Description

The function of the RX circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide DC level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide RX data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the MX589's RX Filter by a suitable gain and DC level adjusting circuit. This circuit can be built with external components around the on-chip RX Input Amplifier. The gain should be set so that the signal level at the RX Feedback pin is nominally 1V peak to peak (for V_{DD}=5.0V) centered around V_{BIAS} when receiving a continuous "1111000011110000.." data pattern.

Positive going signal excursions at RX Feedback pin will produce a logic "0" at the RX Data Output. Negative going excursions will produce a logic "1."

The received signal is fed through the lowpass RX Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors, one of which measures the amplitude of the 'positive' parts of the received signal. The other measures the amplitude of the 'negative' portions. (Positive refers to signal levels higher than $V_{DD}/2$, and negative to levels lower than $V_{DD}/2$.)

External capacitors are used by these detectors, via the Doc1 & Doc2 pins, to form voltage 'hold' or 'integrator' circuits. These two levels are then used to establish the optimum DC level decision-thresholds for the Clock and Data extraction, depending upon the RX signal amplitude and any DC offset.

RX Circuit Control Modes

The RX Circuit blocks are controlled by externally applied logic levels to the PLLacq, $\overline{\text{RX Hold}}$ and RXDCacq pins (see Table 2). Table 2 shows control signals, the functions they control and their modes of operation.

RX Hold	RXDCacq	PLLacq	RX Level Measurement Mode	PLL Mode
LO	LO	LO	Hold	Hold
LO	LO	HI	Hold	Acquire
HI	LO	LO	Averaging Peak Detect	Track
HI	LO	HI	Averaging Peak Detect	Acquire
X	LO to HI	X	Clamp	X
HI	HI	HI	Fast Peak Detect	Acquire
LO	HI	LO	Fast Peak Detect	Hold
HI	LO	HI to LO	Averaging Peak Detect	Medium Bandwidth
HI	HI	LO	Fast Peak Detect mode	Track

X=Don't Care

PLL Acquire: Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. The Acquire mode will operate as long as PLLacq is a logic "1".

PLL Medium Bandwidth: The correction applied to the extracted clock is limited to a maximum of ±1/16th bit-period for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a "1" to "0" transition of the PLLacq input, provided that the RX Hold input is a logic "1".

PLL Track Mode (Narrow Bandwidth): The correction applied to the extracted clock is limited to a maximum of ±1/64th bit-period for every two received zero-crossings. The PLL operates in this mode whenever the RX Hold Input is a logic "1" and PLLacq has been a logic "0" for at least 30 bit periods (after Medium Bandwidth operation for instance).

PLL Hold: The PLL feedback loop is broken, allowing the RX Clock to freewheel during signal fade periods.

RX Level Measurement Clamp: Operates for one bit-time after a "0" to "1" transition of the RXDCacq input. The external capacitors are rapidly charged towards a voltage mid-way between the received signal input level and V_{BIAS}, with the charge time-constant being of the order of 0.5bit-time.

RX Level Measurement Fast Peak Detect: The voltage detectors act as peak-detectors, one capacitor is used to capture the 'positive'-going signal peaks of the RX Filter output signal and the other capturing the 'negative'-going peaks. The detectors operate in this mode whenever the RXDCacq input is at a logic "1," except for the initial 1-bit Clamp-mode time.

RX Level Measurement Averaging Peak Detect: Provides a slower but more accurate measurement of the signal peak amplitudes.

RX Level Measurement Hold: The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000 bits] towards V_{BIAS}).

Table 2 - RX Circuit Controls

Application Information .....

RX Clock Extraction

The 'RX Clock Extraction' circuit is based on a zero crossing tracking loop which uses a multimode or multiresolution digital PLL. The lowest timing resolution option (Acquire mode) allows for fast initial phase acquisition. At most 8 zero crossings are required for initial acquisition. The loop can be programmed to operate in this mode using the RX Hold and the PLLacq pins (see Table 2).

The highest timing resolution, which is 1/64 bit-period, is obtained when the PLL is in its track mode. This mode of operation yields the least amount of phase jitter, which is desirable to limit the associated BER performance degradation. The loop can be set up to operate in this mode as shown in Table 2.

The loop also has a medium resolution (i.e. medium bandwidth) which is activated only when the MX589 controls are such that the PLL is switching from its acquire to its track mode. In such cases the medium setting is used automatically for a limited time (30 bits) after which the loop goes into its track mode. The medium bandwidth setting offers a compromise between fast acquisition and low jitter requirements.

The PLL can also be placed in a HOLD mode, where the RX Clock phase corrections are completely stopped. This mode of operation can be selected as shown in Table 2.

RX DC Level Measurement

The MX589 provides three user-programmable modes of operation for DC level measurement:

1) **Fast Peak Detect** - the detectors rapidly capture the positive and negative going signal peaks (more susceptible to noise).
2) **Averaging Peak Detect** - gives a slower but more accurate measurement of the signal peak amplitudes.
3) **Hold** - the outputs of the voltage detectors remain essentially at the last reading.

A fourth **"Clamp"** mode operates for one bit-time after a LO to HI transition of the RXDCacq input.

These modes of operation can be selected, one at a time, by applying the appropriate logic levels to the RX Hold and RXDCacq inputs (see Table 2).

RX Data Extraction

The 'RX Data Extraction' circuit decides whether each received bit is a "1" or "0" by sampling the received signal, after filtering, and comparing the sample values to an adaptive threshold derived from the 'Level Measuring' circuit. This threshold is adapted from bit to bit to compensate for intersymbol interference caused by the bandlimiting of the overall transmission path and the Gaussian premodulation filter.

Extracted data is output from the 'RX Data' pin, and should be sampled externally on the rising edge of the 'RX CLK.'

RX Data Formats

The receive section of the MX589 works best with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences (>100 bits) of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided.

For this reason, it is recommended that data is made random in some manner before transmission, for example by 'exclusive-ORing' it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble for BT=0.3 should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the eye of pattern '10101010 ....' has the most gradual slope and will yield poor peak levels for the RX circuits. For BT=0.5 the eye pattern of '10101010...' has reduced intersymbol interference and may be used as the preamble (DC Acq pin should be held high during preamble). See Fig. 10.

RX S/N Detection

The 'RX S/N Detector' system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the 'RX S/N' pin. A high level indicates a series of GOOD crossings; a low level indicates a BAD crossing.

By averaging this output it is possible to derive a measure of the Signal-to-Noise-Ratio and hence the Bit-Error-Rate of the received signal (see Fig. 5).

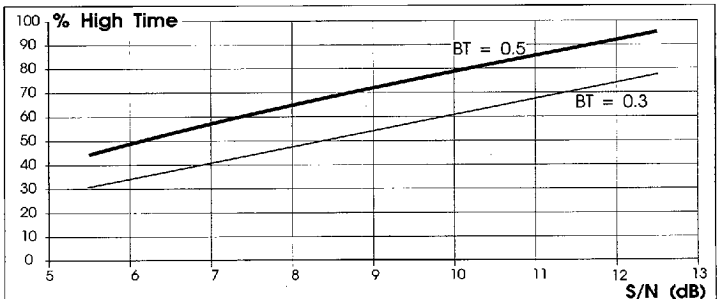


Figure 5 - Typical Rx S/N Output 'High-Time' (%) vs Input S/N

Application Information .....

RX Circuit Control Sequence

As shown in Figure 6, a data transmission generally begins with a preamble of, for example, "1100110011001100," to allow the receive modem to establish timing- and level- lock as quickly as possible. During the time that the preamble is expected, the RXDCacq and PLLacq inputs should be switched from a logic "0 to 1" so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The $\overline{\text{RX Hold}}$ input should normally be held at a logic "1" while data is being received, but may be driven to a logic "0" to freeze the Level Measuring and Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the $\overline{\text{RX Hold}}$ input to a logic "1" at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the RXDCacq to a logic "1" for 10 to 20 bit periods.

$\overline{\text{RX Hold}}$ has no effect on the Level Measuring circuits while RXDCacq is at a logic "1," and has no effect on the PLL while PLLacq is at a logic "1."

A logic "0" on $\overline{\text{RX Hold}}$ does not disable the RX Clock output, and the RX Data Extraction and S/N Detector circuits will continue to operate.

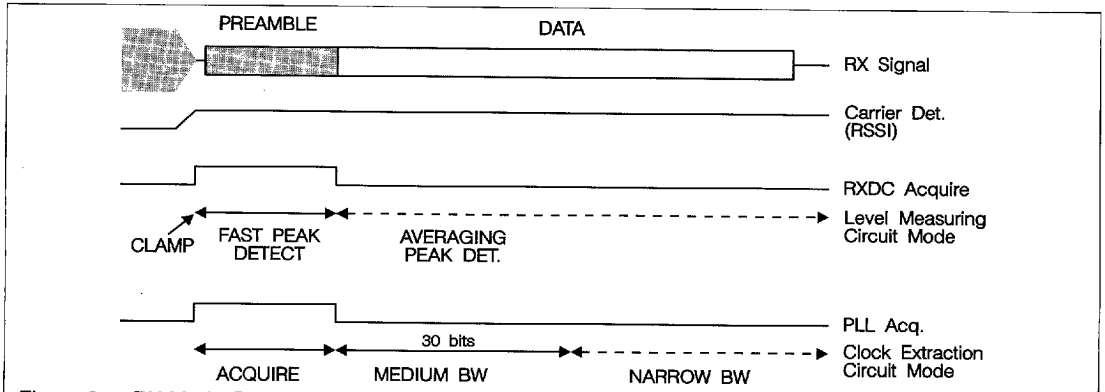


Figure 6 - RX Mode Control Diagram

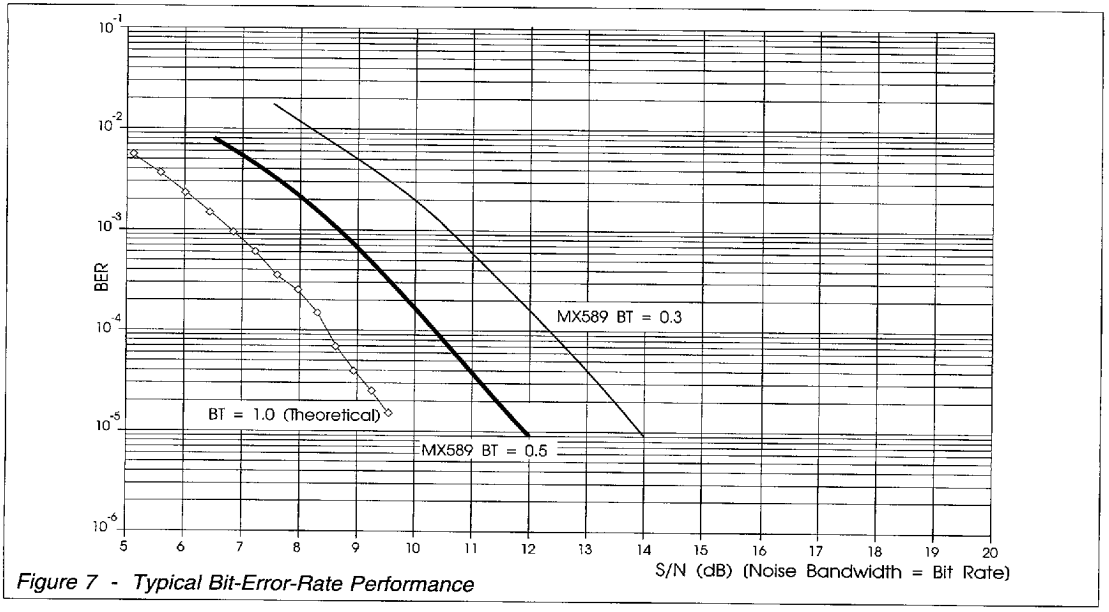


Figure 7 - Typical Bit-Error-Rate Performance

Application Information .....

TX Signal Path Description

The binary data applied to the 'TX Data' input is retimed within the chip on each rising edge of the 'TX Clock' and then converted to a 1-volt peak-to-peak binary signal centered about V_{BIAS} (for V_{DD}= 5.0V)

If the 'TX Enable' input is 'high,' then this internal binary signal will be connected to the input of the lowpass TX Filter, and the output of the filter connected to the 'TX Out' pin.

TX Enable	TX Filter Input	TX Out Pin
'1' (high)	1 volt p-p Data In	Filtered Data
"0" (low)	V_{BIAS}	V_{BIAS} via 500kΩ

A 'low' input to the 'TX Enable' will connect the input of the TX Filter to V_{BIAS}, and disconnect the 'TX Out' pin from the filter, connecting it instead to V_{BIAS} through a high resistance (nominally 500kΩ).

The TX Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimize amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs-frequency response of the transmit filtering provided by the MX589 have been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note that an external RC network is required between the 'TX Out' pin and the input to the Frequency Modulator (see Figures 2 and 3). This network, which can form part of any d.c. level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to capacitor C_1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The component values should be chosen so that the product of the resistance (Ω) and the capacitance (Farads) is:

BT of 0.3 = 0.34/bit rate (bits/second)
BT of 0.5 = 0.22/bit rate (bits/second)
with the following suitable values for common bit rates:

Data Rate	BT	R	C
8000 bps	0.3	91.0kΩ	470pF
4800 bps	0.5	100kΩ	470pF
9600 bps	0.5	47.0kΩ	470pF
19,200 bps	0.5	22.0kΩ	470pF
32,000 bps	0.3	47.0kΩ	220pF
32,000 bps	0.5	47.0kΩ	150pF
38,400 bps	0.3	47.0kΩ	180pF
38,400 bps	0.5	47.0kΩ	120pF

The signal at 'TX Out' is centered around V_{BIAS}, going positive for logic "1" (high) level inputs to the 'TX Data' input and negative for logic "0" (low) inputs.

When the transmit circuits are put into a 'powersave' mode (by a logic "1" to the 'TX PS' pin) the output voltage of the TX Filter will go to V_{SS}. When power is subsequently restored to the TX Filter, its output will take several bit-times to settle. The 'TX Enable' input can be used to prevent these abnormal voltages from appearing at the 'TX Out' pin.

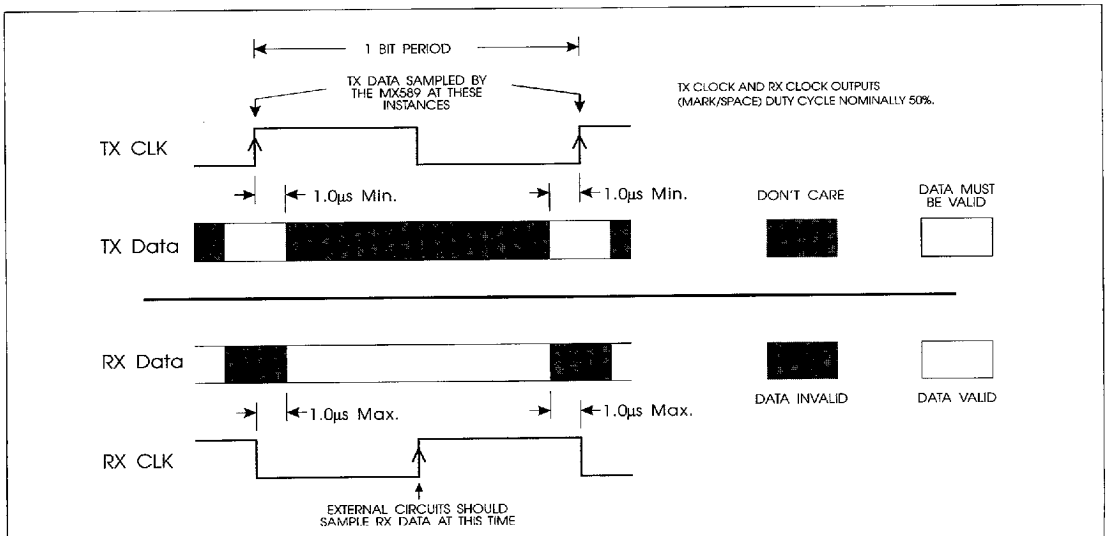


Figure 8 - RX and TX Clock Data Timings

Application Information .....

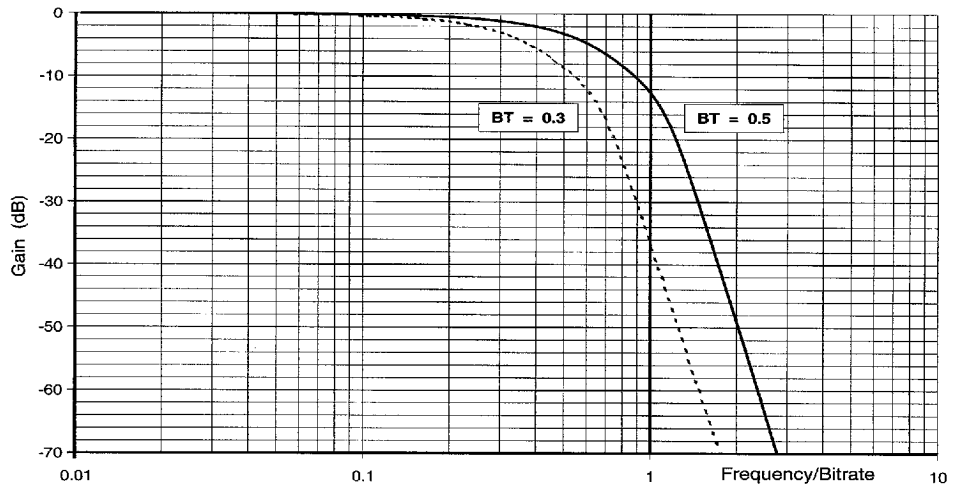


Figure 9 - TX Filter Response

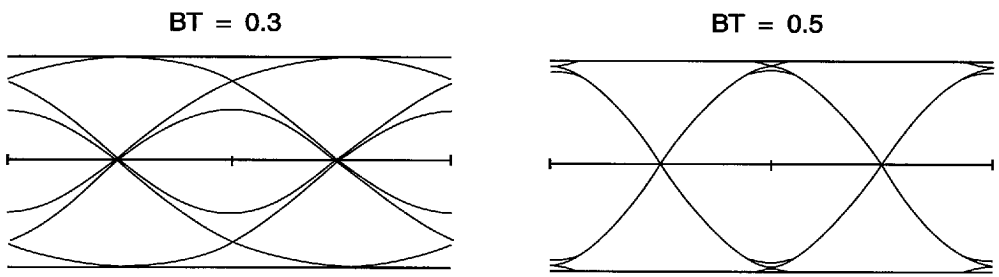


Figure 10 - Typical Transmit Eye Patterns

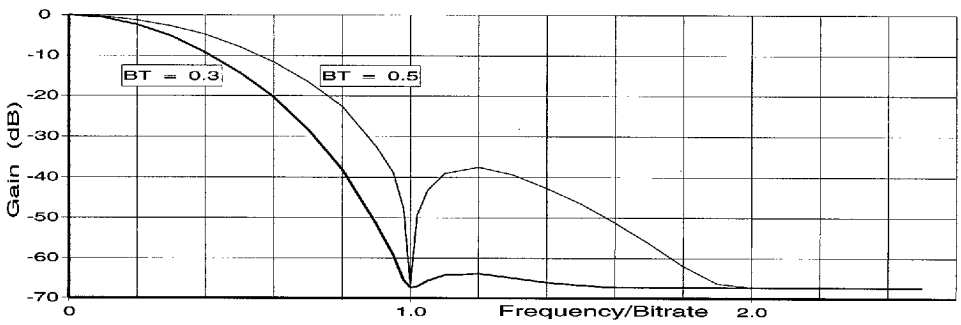


Figure 11 - TX Output Spectrum (Random Data)

Application Information .....

Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index is required.

For optimum channel utilization, (eg. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

Bitrate, BT and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on the following:

- Channel spacing
- Allowable adjacent channel interference
- TX filter bandwidth
- Peak carrier deviation (Modulation Index)
- TX and RX carrier frequency accuracies
- Modulator and Demodulator linearity
- RX IF filter frequency and phase characteristics
- Use of error correction techniques
- Acceptable error-rate

As a guide to MOBITEX operation, a raw data-rate of 8kbps at 12.5kHz channel spacing may be achievable - depending on local regulatory requirements- using a ±2kHz maximum deviation, a BT of 0.3, and no more than 1.5kHz discrepancy between TX & RX carrier frequencies.

Forward error correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4,800bps would allow the BT to be increased to 0.5, improving the error-rate performance.

For CDPD operation, a raw data-rate of 19.2kbps at 30kHz channel spacing may be utilized with a ±8kHz maximum deviation, a BT of 0.5, and no more than 3kHz discrepancy between TX & RX carrier frequencies.

The above values should be used as a guide only. Regulatory compliance of a design should be verified.

FM Modulator, Demodulator and IF

For optimum performance, the 'eye' pattern of the received signal (when receiving random data) applied to the MX589 should be as close as possible to the Transmit 'eye' pattern examples shown in Figure 11.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to -

- Linearity and frequency/phase response of the TX frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few hertz. This is because two-point modulation is necessary for synthesized radios.
- Bandwidth & phase response of the RX IF filters.
- Accuracy of the TX and RX carrier frequencies - any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the RX demodulator should be d.c. coupled to the MX589 'RX Signal In' pin (with a d.c. bias added to center the signal at the RX Feedback pin around $V_{DD}/2$ [V_{BIAS}]). However a.c. coupling can be used provided that:

- The 3 dB cut-off frequency is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).
- The data does not contain long sequences of consecutive ones or zeroes.
- Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the MX589 to settle before the 'RXDCacq' line is strobed.

Application Information .....

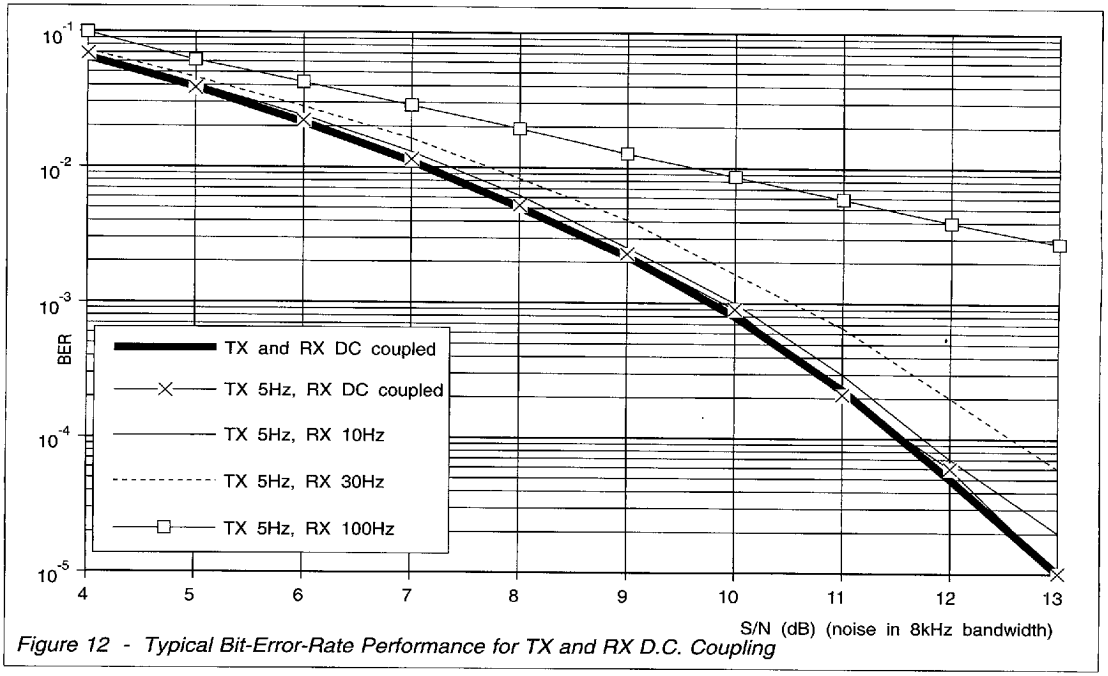


Figure 12 - Typical Bit-Error-Rate Performance for TX and RX D.C. Coupling

A.C. Coupling of TX and RX Signals

Practical applications may require AC coupling from the MX589's TX Output to the frequency modulator and between the receiver's frequency discriminator and the MX589's RX Input. This creates two problems:

1) AC coupling of the signal degrades the Bit Error Rate (BER) performance of the MX589. Figure 12 (above) shows the typical static BER performance of the MX589 at 8kbps (without FEC) for different levels of AC coupling.

2) AC coupling at the RX Input will transform a step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the MX589's level measuring circuits. The time for this step to decay to 37% of its original value is "RC":

$$RC = \frac{1}{2\pi \bullet \text{the 3dB cut-off frequency of the RC network}}$$

and is 8ms (64 bit-times) at 8kbps for a 20Hz network.

For these reasons, the optimum -3dB cut-off frequencies are approximately 5.0Hz in the TX path and 20.0Hz in the RX path under the following conditions:

Data Rate = 8kbps	TX BT = 0.3
V_{DD} = 5.0V	T_{AMB} = 25°C

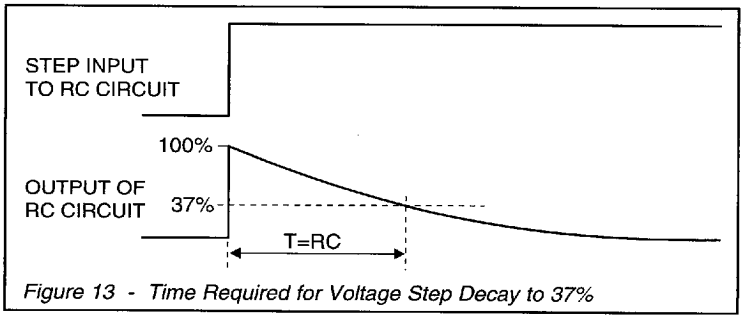


Figure 13 - Time Required for Voltage Step Decay to 37%

Application Information .....

Two Point Modulation

When designing the MX589 into a radio that uses a frequency synthesizer, a two-point modulation technique is recommended. This is both to prevent the radio's PLL circuitry from counteracting the modulation process, and to provide a clean flat modulation response down to d.c.

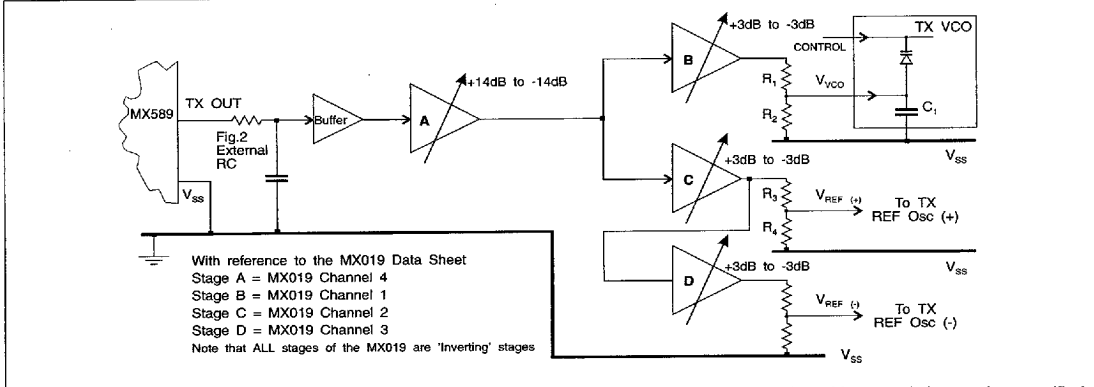
Figure 14 shows a suggested basic configuration to provide a two-point modulation drive from the MX589 TX Output using MX•COM's MX019 Digitally Controlled 'Quad' Amplifier Array. The MX019 elements provide individual set-up, calibration and dynamic control of modulation levels. Level setting control of the amplifiers/ attenuators of the MX019 is via an 8-bit data word.

With reference to Figure 14, the buffer amplifier is required to prevent loading of the MX589 external RC circuit.

Stage B, with R_1/R_2, provides suitable signal and d.c. levels for the VCO varactor; C_1 is RF decoupling. The drive level should be adjusted (digitally) to provide the desired deviation.

Stage C, with R_3/R_4, provides the Reference Oscillator drive (application dependent). This parameter is set by adjusting for minimum a.c. signal on the PLL control voltage with a low-frequency modulating signal (inside the PLL bandwidth) applied.

Stage D could be used with the components shown if a negative reference drive is required. Stage A provides buffering and overall level control.



Note: this example has not been verified.

Figure 14 - An Example of Two-Point Modulation Drive with Individual Adjustment Using the MX019

'Acquisition' and 'Hold' Modes

The 'RXDCacq' and 'PLLacq' inputs must be pulsed 'High' for about 16 bits at the start of reception to ensure that the DC measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken 'Low' again.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on.

The MX589 can tolerate DC offsets in the received signal of at least ±0.5V with respect to V_{BIAS}, (measured at the RX Feedback pin). However, to ensure that the DC offset compensation circuit operates correctly and with minimum delay, the 'Low' to 'High' transition of the 'RXDCacq' and 'PLLacq' inputs should occur after the mean input voltage to the MX589 has settled to within about 0.1V of its final value. (Note that this can place restrictions on the value of any series signal coupling capacitor.)

As well as using the 'RX Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade', it may also be used in systems which use a continuously transmitting control channel to freeze the RX circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX589 'Xtal' clock needs to be accurate enough that the derived 'RXClock' output does not drift by more than about 0.1 bit time from the actual received data-rate during the time that the 'RXHold' input is 'Low'.

The 'RXDCacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RXHold' input is 'Low' for more that a few hundred bit-times.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude. Note however, that these pins are driven from very high-impedance circuits, so that the DC load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current (supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Characteristics

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Data Rate = 8000 bps

Xtal/Clock f_0 = 4.096 MHz

Noise bandwidth = bit rate

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Operating Limits			Remarks	Min.	Max.	Unit
Supply Voltage (V_{DD})				3.0	5.5	V
Operating Temperature				-40	+85	°C
RX & TX Data Rate			$V_{DD} \geq$ 3.0V	4,000	20,000	bps
			$V_{DD} \geq$ 4.5 V	4,000	40,000	bps
Xtal/Clock Frequency			$V_{DD} \geq$ 3.0V	1.0	5.0	MHz
			$V_{DD} \geq$ 4.5 V	1.0	6.5	MHz
"High" Pulse Width			Note 10	60.0	-	ns
"Low" Pulse Width			Note 10	60.0	-	ns
Static Values						
Supply Current						
(for V_{DD}=3.0V)	**TX PS**	**RX PS**	1			
	1	1		-	0.5	- mA
	0	1		-	1.0	- mA
	1	0		-	1.0	- mA
	0	0		-	1.5	- mA
(for V_{DD}=5.0V)	**TX PS**	**RX PS**	1			
	1	1		-	1.0	- mA
	0	1		-	2.0	- mA
	1	0		-	3.0	- mA
	0	0		-	4.0	- mA
Input Logic Levels						
Logic "1"				3.5	-	- V
Logic "0"				-	-	1.5 V
Logic Input Current			2	-5.0	-	5.0 µA
Logic "1"Output Level at IOH = -120µA				4.6	-	- V
Logic "0"Output Level at IOL = 120µA				-	-	0.4 V

Characteristics	See Note	Min.	Typ.	Max.	Unit
Transmit Parameters					
TX Output Impedance	3	-	1.0	-	kΩ
TX Output Level	4,11	0.8	1.0	1.2	V p-p
TX Data Delay (BT = 0.3)	5	-	2.0	2.5	bit-periods
(BT = 0.5)	5	-	1.5	2.0	bit-periods
TX PS to Output-Stable Time	6	-	4.0	-	bit-periods
Receive Parameters					
RX Amplifier -					
Input Impedance		1.0	-	-	MΩ
Output Impedance	7	-	10.0	-	kΩ
Voltage Gain		-	50.0	-	dB
RX Filter Signal Input Level	8,11	0.7	1.0	1.3	V p-p
RX Time Delay	9	-	-	3.0	bit-periods
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}	12	-	50.0	-	kΩ
Voltage Gain	12	-	25.0	-	dB

Notes

1. Not including current drawn from the MX589 pins by external circuitry. See Absolute Maximum Ratings.
2. For V_{IN} in the range V_{SS} to V_{DD}.
3. For a load of 10kΩ or greater. TX PS input at logic "0"; TX Enable = "1".
4. Data pattern of "1111000011110000 .."
5. Measured between the rising edge of 'TX Clock' and the center of the corresponding bit at 'TX Out.'
6. Time between the falling edge of 'TX PS' and the 'Tx Out' voltage stabilising to normal output levels.
7. For a load of 10kΩ or greater. RX PS input at logic "0".
8. For optimium performance, Measured at the 'RX Feedback' pin for a "1111000011110000 ..." pattern.
9. Measured between the center of bit at 'RX Signal In' and corresponding rising edge of the 'RX Clock'.
10. Timing for an external clock input to the Xtal/clock pin.
11. Typical level shown is at V_{DD}=5.0V; actual levels are proportional to applied V_{DD}.
12. Small signal measurement at 1.0kHz with no load on $\overline{Xtal}$ output.

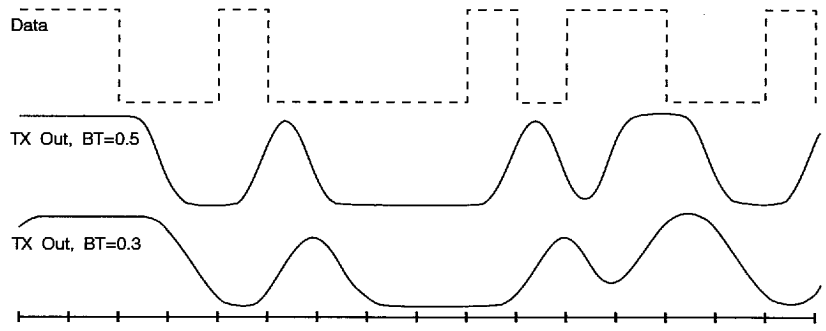

Figure 15 - Typical Signal Waveforms