19-2450; Rev 1; 8/92

MAXIM

CMOS, Quad, 8-Bit D/A Converter

1.0 SCOPE

1.1 This specification covers the detail requirements for a quad, 8-bit, monolithic, CMOS digital-to-analog converter (DAC), with output buffer amplifiers and interface logic. Separate on-chip latches are provided for each of the four DACs. This circuit is processed in accordance with MIL-STD-883 and is fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	MX7226T(X)/883B
-2	MX7226U(X)/883B

1.3 Package

(X)	Package	Description
Q	Q-20	20-Pin Ceramic Dual-In-Line Package (CERDIP)
E	E-20	20-Pin Ceramic Leadless Chip Carrier (LCC)

Note: See *Package Information* section for package drawings and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to AGND ..... -7V, V_{DD}
V_{SS} to DGND ..... -7V, V_{DD}
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
AGND to DGND ..... -0.3V, V_{DD}
VREF to AGND ..... -0.3V, V_{DD}
V_{OUT} to AGND ..... V_{SS}, V_{DD}
Power Dissipation (T_A = +70°C, Tj = +150°C)
  CERDIP (derate 11.11mW/°C above +70°C) 889mW
  LCC (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

1.5 Thermal Resistance Θ_{JC} = 40°C/W for Q-20
Θ_{JC} = 55°C/W for E-20
Θ_{JA} = 90°C/W for Q-20
Θ_{JA} = 110°C/W for E-20

2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Resolution (Note 2)	RES	Guaranteed, but not tested	All	1, 2, 3	8		Bits
Total Unadjusted Error	E_T	V_{DD} = 14V, V_{SS} = -5V, VREF = 10V	-1	1, 2, 3	-2	2	LSB
			-2		-1	1	
Relative Accuracy	RA	V_{DD} = 14V, V_{SS} = -5V, VREF = 10V	-1	1, 2, 3	-1	1	LSB
			-2		-0.5	0.5	
Differential Nonlinearity (Note 3)	DNL	V_{DD} = 14V, V_{SS} = -5V, VREF = 10V	All	1, 2, 3	-1	1	LSB
Full-Scale Error	A_E	V_{DD} = 14V, V_{SS} = -5V, VREF = 10V	-1	1, 2, 3	-1	1	LSB
			-2		-0.5	0.5	
Zero-Code Error		V_{DD} = 11.4V, 14V, 16.5V, V_{SS} = -5V, VREF = V_{DD} - 4V	-1	1, 2, 3	-30	30	mV
			-2	1	-15	15	
				2, 3	-20	20	
Voltage Output Settling Time (Note 4)	T_{SL}	Positive (Full Scale)	All	4		5	µs
		Negative (Full Scale)				7	
Voltage Output Slew Rate	T_{SR}		All	4	2.5		V/µs
Minimum Load Resistance	RL_{MIN}	V_{OUT} = 10V, V_{DD} = 14V	All	4	2		kΩ
Reference Input Resistance	R_{IN}	V_{DD} = 14V	All	1, 2, 3	2		kΩ
Reference Input Capacitance	C_{IN}	DAC loaded with all 1s	All	4		300	pF
		DAC loaded with all 0s	All	4	30		
Digital Input High Voltage	V_{IH}	V_{DD} = 11.4V	All	1, 2, 3	2.4		V
Digital Input Low Voltage	V_{IL}	V_{DD} = 11.4V	All	1, 2, 3		0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}, V_{DD} = 16.5V, V_{SS} = 5.5V	All	1, 2, 3	-1	1	µA
Digital Input Capacitance	C_{IN}		All	4		8	pF

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Write Pulse Width, t_1 (Note 5)	t_{WR}		All	9	200		ns
Address to Write-Setup Time, t_2 (Note 5)	t_{AS}		All	9	0		ns
Address to Write-Hold Time, t_3 (Note 5)	t_{AH}		All	9	10		ns
Data Valid to Write-Setup Time (Note 5)	t_{DS}		All	9	100		ns
Data Valid to Write-Hold Time (Note 5)	t_{DH}		All	9	10		ns
Positive Supply Current	I_{DD}	$V_{IN} = V_{IL}$ or V_{IH}, V_{DD} = 16.5V, V_{SS} = -5.5V VREF = 12.5V	All	1, 2, 3		13	mA
Negative Supply Current	I_{SS}	$V_{IN} = V_{IL}$ or V_{IH}, V_{DD} = 16.5V, V_{SS} = -5.5V VREF = 12.5V	All	1, 2, 3		11	mA

Note 1: Dual supply operation, V_{DD} = +11.4V to +16.5V, V_{SS} = -5V, AGND = DGND = 0V, VREF = +2V to (V_{DD} - 4V), unless otherwise noted.
Note 2: Characteristics supplied for use as a typical design limit, but not production tested.
Note 3: Guaranteed monotonic to 8 bits.
Note 4: Settling time to ±0.5LSB.
Note 5: Timing shown in section 4.3.

TABLE 2. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 6)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Resolution (Note2)	RES		All		8		Bits
Total Unadjusted Error	E_T	V_{DD} = 14V, VREF = 10V	-1	1, 2, 3	-2	2	LSB
			-2		-1	1	
Differential Nonlinearity (Note 3)	DNL	V_{DD} = 14V, VREF = 10V	All	1, 2, 3	-1	1	LSB
Voltage Output Settling Time (Notes 4, 5)	T_{SL}	Positive (Full Scale)	All	4		5	µs
		Negative (Full Scale)	All			20	
Voltage Output Slew Rate (Note 5)	T_{SR}		All	4	2.5		V/µs
Minimum Load Resistance (Note 5)	RL_{MIN}	V_{OUT} = 10V, V_{DD} = 15V	All	4	2		kΩ
Reference Input Resistance	R_{IN}	V_{DD} = 14V	All	1, 2, 3	2		kΩ
Reference Input Capacitance	C_{IN}	DAC loaded with all 1s	All	4		300	pF
		DAC loaded with all 0s	All		30		
Digital Input High Voltage	V_{IH}	V_{DD} = 14.25V	All	1, 2, 3	2.4		V
Digital Input Low Voltage	V_{IL}	V_{DD} = 14.25V	All	1, 2, 3		0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}, V_{DD} = 15.75V	All	1, 2, 3	-1	1	µA
Digital Input Capacitance	C_{IN}		All	4		8	pF
Write Pulse Width, t_1 (Note 5)	t_{WR}		All	9	200		ns
Address to Write-Setup Time (Note 5)	t_{AS}		All	9	0		ns
Address to Write-Hold Time (Note 5)	t_{AH}		All	9	10		ns
Data Valid to Write-Setup Time (Note 5)	t_{DS}		All	9	100		ns
Data Valid to Write-Hold Time (Note 5)	t_{DH}		All	9	10		ns
Power-Supply Current	I_{DD}	V_{IN} = V_{IL} or V_{IH}, V_{DD} = 15.75V, VREF = 10V	All	1, 2, 3		13	mA

Note 2: Characteristics supplied for use as a typical design limit, but not production tested.
Note 3: Guaranteed monotonic to 8 bits.
Note 3: Settling time to ±0.5LSB.
Note 5: Timing shown in section 4.3.
Note 6: Single-supply operation, V_{DD} = +14.25V to +15.75, V_{SS} = AGND = DGND = 0V, VREF = +10V, unless otherwise noted.

3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Interim and final electrical test requirements shall be as specified in Table 3.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 3.
(2) Selected subgroups in Tables 1 and 2, Method 5005 of MIL-STD-883 shall be omitted.

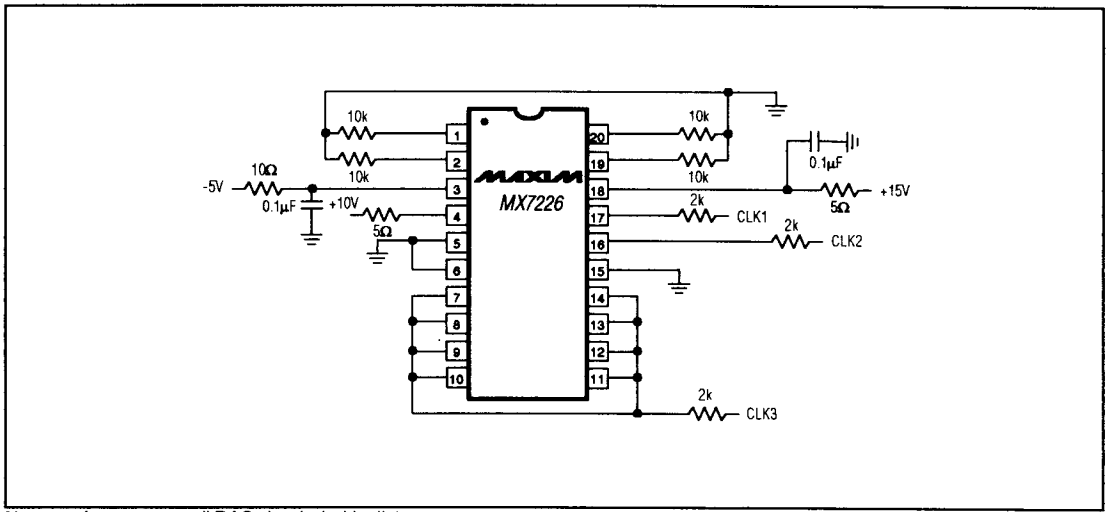
3.4 Groups C and D inspections:
a. End-point electrical parameters shall be specified in Tables 1 and 2.
b. Steady-state life test (Method 1005 of MIL-STD-883):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,* 2, 3
Group A Test Requirements (Method 5005)	1, 2, 3, 4**
Groups C and D End-Point Electrical Parameters (Method 5005)	1

* PDA applies to Subgroup 1 only.
** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 5 units.

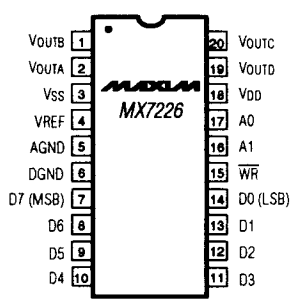
4.0 Life Test/Burn-In Circuit



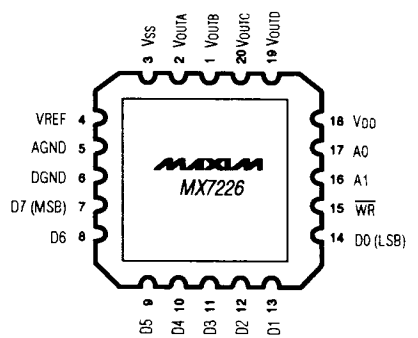
Note: At power-up, all DACs loaded with all 1s.

4.1 Pin Configurations

TOP VIEW

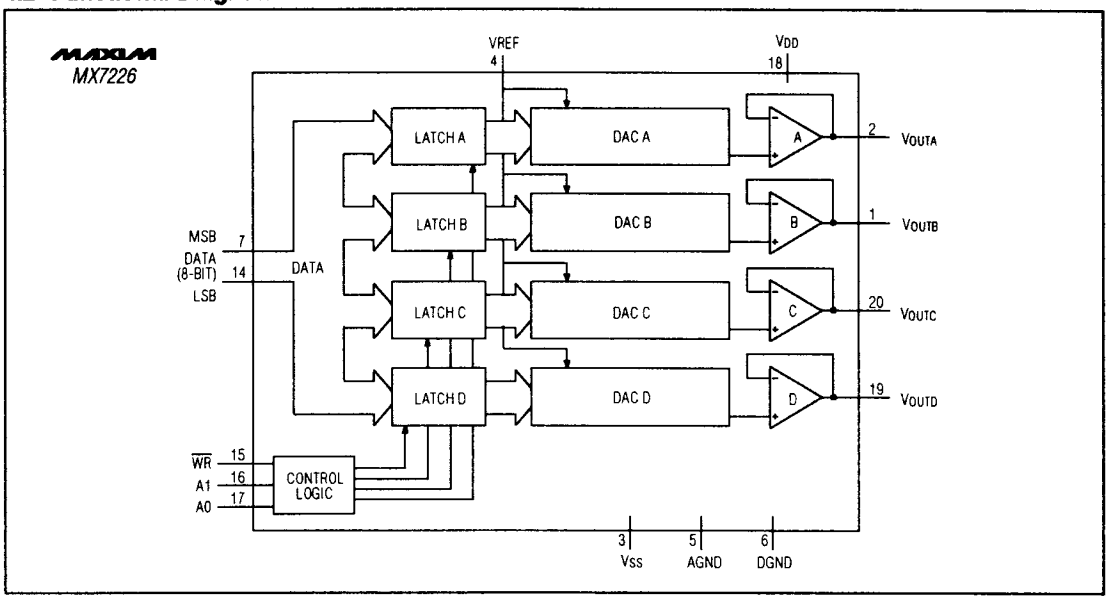


20-PIN CERDIP

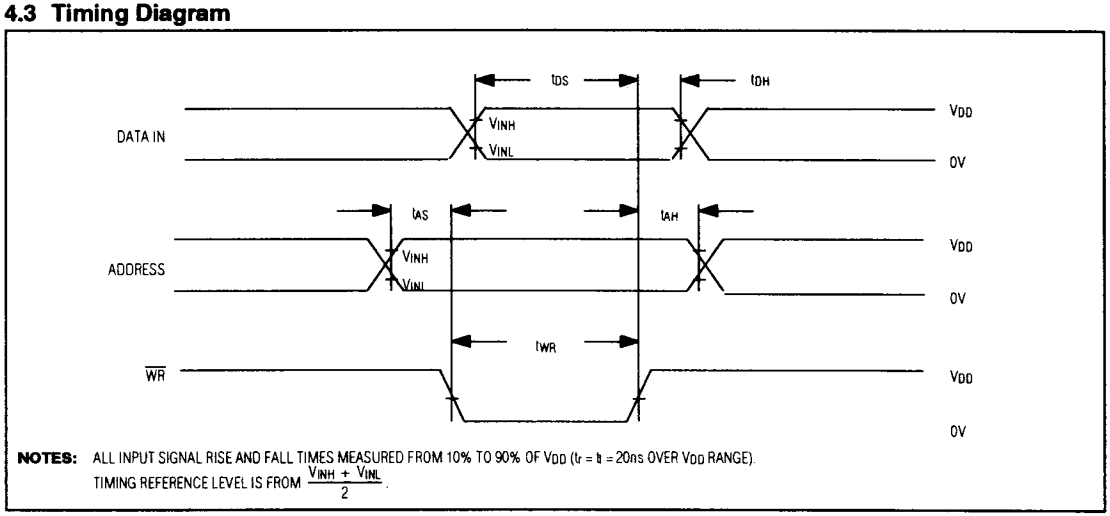


20-PIN LCC

4.2 Functional Diagram



4.3 Timing Diagram



NOTES: ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD} ($t_r = t_f = 20ns$ OVER V_{DD} RANGE).
TIMING REFERENCE LEVEL IS FROM $\frac{V_{INH} + V_{INL}}{2}$.

4.3 Mode Selection Table

LOGIC CONTROL			OPERATION
$\overline{WR}$	A1	A0	
H	X	X	No operation— device not selected
L	L	L	DAC A transparent
↑	L	L	DAC A latched
L	L	H	DAC B transparent
↑	L	H	DAC B latched
L	H	L	DAC C transparent
↑	H	L	DAC C latched
L	H	H	DAC D transparent
↑	H	H	DAC D latched

L = Low State, H = High State, X = Don't Care