19-0092; Rev 0; 12/92

MAXIM

CMOS, 12-Bit, Single-Supply Complete Voltage-Output DACs

1.0 SCOPE

1.1 This specification covers the detail requirements for two 12-bit digital-to-analog converters (DACs). The MX7245 has a parallel-loading structure while the MX7248 has an (8 + 4) loading structure. These circuits are processed in accordance with MIL-STD-883 and are fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	MX7245S(X)/883B
-2	MX7248S(Y)/883B

1.3 Package

(X)	Package	Description
Q	Q-24	24-Pin Ceramic Dual-In-Line Package (CERDIP)
E	E-28	28-Pin Ceramic Leadless Chip Carrier (LCC)

(Y)	Package	Description
Q	Q-20	20-Pin Ceramic Dual-In-Line Package (CERDIP)
E	E-20	20-Pin Ceramic Leadless Chip Carrier (LCC)

Note: See *Package Information* section for package drawings and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{DD} to V_{SS} ..... -0.3V, +34V
REFOUT to AGND (Note 1) ..... 0V, V_{DD}
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
V_{OUT} to V_{SS} (Note 1) ..... 0V, +24V
V_{OUT} to V_{DD} (Note 1) ..... -32V, 0V
Digital Input Voltage to DGND ..... -0.3V, (V_{DD} + 0.3V)
AGND to DGND ..... -0.3V, V_{DD}

Note 1: The outputs may be shorted to voltages in this range, provided the power dissipation of the package is not exceeded.

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1.4 Absolute Maximum Ratings (continued)

Power Dissipation (T_A = +70°C, Tj = +150°C)
- 24-Pin CERDIP (derate 12.50mW/°C above +70°C) 1000mW
- 28-Pin LCC (derate 10.20mW/°C above +70°C) 816mW
- 20-Pin CERDIP (derate 11.11mW/°C above +70°C) 889mW
- 20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

1.5 Thermal Resistance

Θ_{JC} = 40°C/W for Q-24
Θ_{JC} = 50°C/W for E-28
Θ_{JC} = 40°C/W for Q-20
Θ_{JC} = 55°C/W for E-20
Θ_{JA} = 80°C/W for Q-24
Θ_{JA} = 98°C/W for E-28
Θ_{JA} = 90°C/W for Q-20
Θ_{JA} = 110°C/W for E-20

2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS—Dual Supplies (Note 2)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Resolution	N		All	1, 2, 3	12		Bits
Relative Accuracy	INL	V_{DD} = 11.4V, V_{SS} = -11.4V V_{DD} = 14.25V, V_{SS} = -14.25V	All	1, 2, 3	-1	1	LSB
		V_{DD} = 14.25V, V_{SS} = -14.25V V_{DD} = 15.75V, V_{SS} = -15.75V			-1 1/2	1 1/2	
Differential Nonlinearity	DNL	Guaranteed monotonic	All	1, 2, 3	-1	1	LSB
Bipolar Offset Error			All	1	-3	3	LSB
				2, 3	-5	5	
DAC Gain Error (Note 3)	FSE		All	1, 2, 3	-2	2	LSB
Full-Scale Output Voltage Error (Note 4)		V_{DD} = 12V, V_{SS} = -12V V_{DD} = 15V, V_{SS} = -15V	All	1	-0.2	0.2	%FSR
				2, 3	-0.6	0.6	
ΔFull Scale/ΔV_{DD}		V_{DD} = ±5%	All	1	-0.12	0.12	%FSR/V
ΔFull Scale/ΔV_{SS}		V_{SS} = ±5%	All	1	-0.1	0.1	%FSR/V
ΔOffset/ΔV_{DD}		V_{DD} = ±5%	All	1, 2, 3	-2	2	mV
ΔOffset/ΔV_{SS}		V_{SS} = ±5%	All	1, 2, 3	-1	1	mV
Reference Output		V_{DD} = 12V and 15V V_{SS} = -12V and -15V	All	1	4.99	5.01	V

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS–Dual Supplies (Note 2) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
ΔReference/ΔV_{DD}		V_{DD} = ±5%	All	1		6	mV/V
Reference Load Sensitivity		Reference load current change (0μA to 100μA) not including R_{OFS} current	All	1, 2, 3	-1.5	1.5	mV
Digital Input High Voltage	V_{INH}		All	1, 2, 3	2.4		V
Digital Input Low Voltage	V_{INL}		All	1, 2, 3		0.8	V
Digital Input Current – Data Inputs	I_{IN}	V_{IN} = 0V or V_{DD}	All	1, 3	-1	1	μA
				2	-10	10	
Digital Input High Current – Control Inputs (Note 5)	I_{INH}	V_{IN} = V_{DD}	All	1, 3	-1	1	μA
				2	-10	10	
Digital Input Low Current – Control Inputs	I_{INL}	V_{IN} = 0V	All	1, 3		150	μA
				2		200	
Digital Input Capacitance	C_{IN}		-1	4		8	pF
			-2			16	
Output Range Resistors	R_{OUT}		All	1, 2, 3	15	30	kΩ
Output Voltage Ranges (Note 6)		Pin strappable. Minimum load resistance is 2kΩ to GND	All	1, 2, 3	0	5	V
					0	10	
					-5	-10	
Power-Supply Current	I_{DD}	Outputs unloaded	All	1		9	mA
				2, 3		12	
Output Voltage Settling Time (Note 7)	t_S	To ±1LSB, R_L = 5kΩ	All	4		5	μs
Output Voltage Slew Rate	SR		All	4	2		V/μs
Chip-Select Pulse Width	t_1	Figure 1	All	9	80		ns
Write Pulse Width	t_2	Figure 1	All	9	80		ns
Chip-Select to Write-Setup Time	t_3	Figure 1	All	9	0		ns
Chip-Select to Write-Hold Time	t_4	Figure 1	All	9	0		ns
Data Valid to Write-Setup Time	t_5	Figure 1	-1	9	100		ns
			-2		110		
Data Valid to Write-Hold Time	t_6	Figure 1	All	9	10		ns
Load DAC Pulse Width	t_7	Figure 1	All	9	80		ns
Clear Pulse Width	t_8	Figure 1	All	9	80		ns

Note 2: V_{DD} = 11.4V, V_{SS} = -11.4V; V_{DD} = 15.75V, V_{SS} = -15.75V, AGND = DGND = 0V, R_L = 2kΩ to GND, C_L = 100pF to GND, REF unloaded, unless otherwise noted. Characterized at initial design and after any subsequent redesigns.
Note 3: Calculated with respect to the reference voltage and measured with an allowance for the offset error.
Note 4: Calculated with an ideal 4.9988V or 9.9976V, depending on the range.
Note 5: Control inputs are $\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$, and $\overline{CLR}$ for MX7245 and $\overline{CSMSB}$, $\overline{CSLSB}$, $\overline{WR}$, and $\overline{LDAC}$ for MX7248.
Note 6: 0V to 10V applies to V_{DD} = 15V ±5% and V_{SS} = -15V ±5% only.
Note 7: For positive full-scale change, the DAC register is loaded with all 0s, then all 1s. For negaitve full-scale change, the DAC register is loaded with all 1s, then all 0s.

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TABLE 2. ELECTRICAL PERFORMANCE CHARACTERISTICS—Single Supply (Note 8)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Resolution	N		All	1, 2, 3	12		Bits
Relative Accuracy	INL	V_{DD} = 11.4V and 14.25V	All	1, 2, 3	-1	1	LSB
		V_{DD} = 14.25V and 15.75V			-1 1/2	1 1/2	
Differential Nonlinearity	DNL	Guaranteed monotonic	All	1, 2, 3	-1	1	LSB
Unipolar Offset Error			All	1	-3	3	LSB
				2, 3	-5	5	
DAC Gain Error (Note 3)	FSE		All	1, 2, 3	-2	2	LSB
Full-Scale Output Voltage Error (Note 4)		V_{DD} = 12V and 15V	All	1	-0.2	0.2	%FSR
				2, 3	-0.6	0.6	
ΔFull Scale/ΔV_{DD}		V_{DD} = ±5%	All	1	-0.12	0.12	%FSR/V
ΔOffset/ΔV_{DD}		V_{DD} = ±5%	All	1, 2, 3	-2	2	mV
Reference Output		V_{DD} = 12V and 15V	All	1	4.99	5.01	V
ΔReference/ΔV_{DD}		V_{DD} = ±5%	All	1		6	mV/V
Reference Load Sensitivity		Reference load current change (0μA to 100μA) not including R_{OFS} current	All	1, 2, 3	-1.5	1.5	mV
Digital Input High Voltage	V_{INH}		All	1, 2, 3	2.4		V
Digital Input Low Voltage	V_{INL}		All	1, 2, 3		0.8	V
Digital Input Current – Data Inputs	I_{IN}	V_{IN} = 0V or V_{DD}	All	1, 3	-1	1	μA
				2	-10	10	
Digital Input High Current – Control Inputs (Note 5)	I_{INH}	V_{IN} = V_{DD}	All	1, 3	-1	1	μA
				2	-10	10	
Digital Input Low Current – Control Inputs	I_{INL}	V_{IN} = 0V	All	1, 3		150	μA
				2		200	
Digital Input Capacitance	C_{IN}		-1	4		8	pF
			-2			16	
Output Range Resistors	R_{OUT}		All	1, 2, 3	15	30	kΩ
Output Voltage Ranges (Note 6)		Pin strappable. Minimum load resistance is 2kΩ to GND	All	1, 2, 3	0	5	V
					0	10	
Power-Supply Current	I_{DD}	Outputs unloaded	All	1		9	mA
				2, 3		12	
Output Voltage Settling Time (Note 7)	t_S	To ±1LSB, R_L = 5kΩ	All	4		5	μs
Output Voltage Slew Rate	SR		All	4	2		V/μs
Chip-Select Pulse Width	t_1	Figure 1	All	9	105		ns
Write Pulse Width	t_2	Figure 1	All	9	105		ns
Chip-Select to Write-Setup Time	t_3	Figure 1	All	9	0		ns
Chip-Select to Write-Hold Time	t_4	Figure 1	All	9	0		ns

TABLE 2. ELECTRICAL PERFORMANCE CHARACTERISTICS–Single Supply (Note 8) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Data Valid to Write-Setup Time	t_5	Figure 1	-1	9	155		ns
			-2	9	180		
Data Valid to Write-Hold Time	t_6	Figure 1	All	9	0		ns
Load DAC Pulse Width	t_7	Figure 1	All	9	90		ns
Clear Pulse Width	t_8	Figure 1	All	9	140		ns

Note 3: Calculated with respect to the reference voltage and measured with an allowance for the offset error.
Note 4: Calculated with an ideal 4.9988V or 9.9976V, depending on the range.
Note 5: Control inputs are $\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$, and $\overline{CLR}$ for MX7245 and $\overline{CSMSB}$, $\overline{CSLSB}$, $\overline{WR}$, and $\overline{LDAC}$ for MX7248.
Note 6: 0V to 10V applies to V_{DD} = 15V ±5%.
Note 7: For positive full-scale change, the DAC register is loaded with all 0s, then all 1s. For negaitve full-scale change, the DAC register is loaded with all 1s, then all 0s.
Note 8: V_{DD} = 11.4V and 15.75V, AGND = DGND = 0V, R_L = 2kΩ to GND, C_L = 100pF to GND, REF unloaded, unless otherwise noted. Characterized at initial design and after any subsequent redesigns.

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3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Interim and final electrical test requirements shall be as specified in Table 3.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 3.
(2) Selected subgroups in Tables 1 and 2, Method 5005 of MIL-STD-883 shall be omitted.

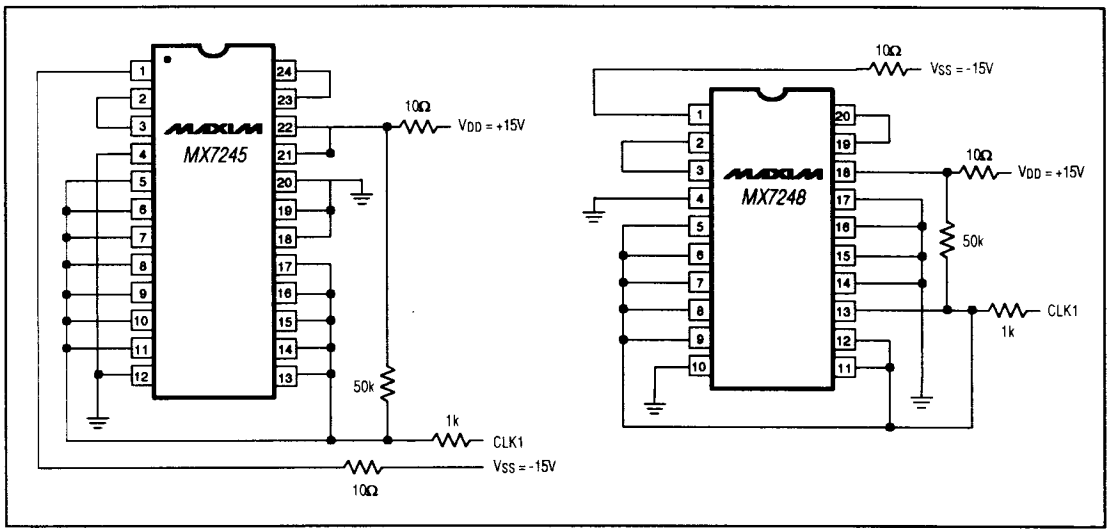
3.4 Groups C and D inspections:
a. End-point electrical parameters shall be specified in Tables 1 and 2.
b. Steady-state life test (Method 1005 of MIL-STD-883):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 3. ELECTRICAL TEST REQUIREMENTS

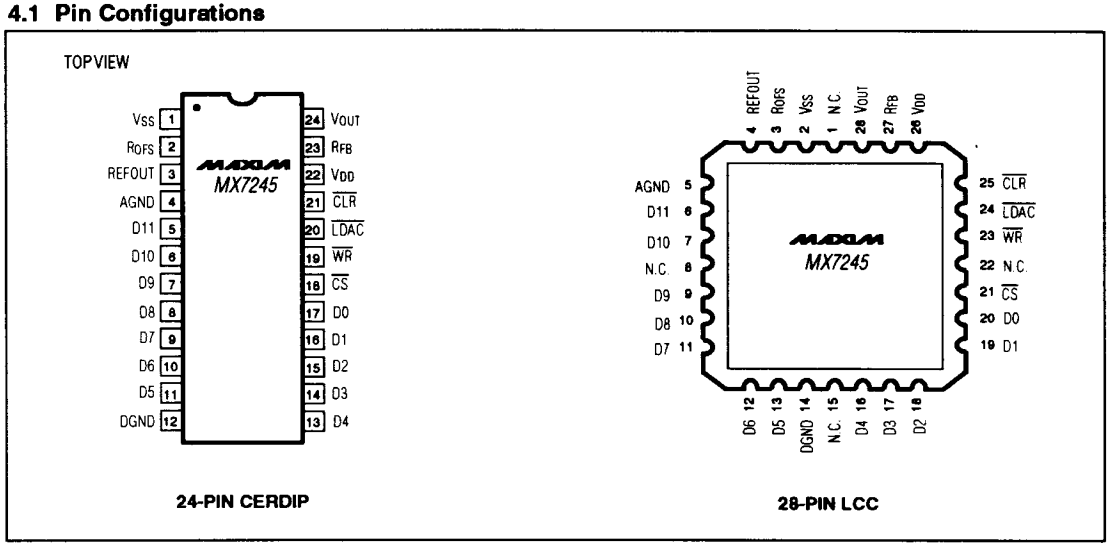
MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Tables 1 and 2)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1*, 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 4,** 9, 10,*** 11***
Groups C and D End-Point Electrical Parameters (Method 5005)	1

* PDA applies to Subgroup 1 only.
** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 5 units.
*** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table 1.

4.0 Life Test/Burn-In Circuits



4.1 Pin Configurations



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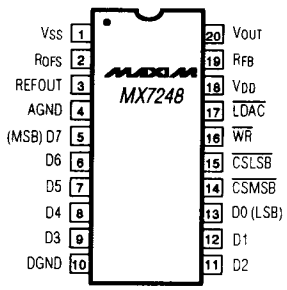
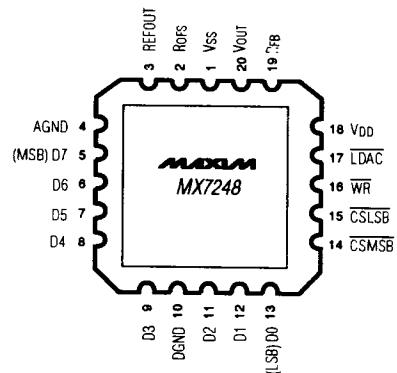
4.1 Pin Configurations (continued)

TOPVIEW

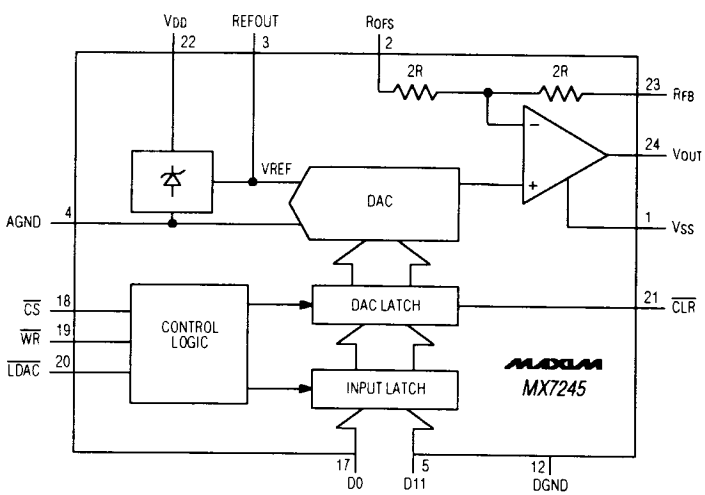


20-PIN CERDIP

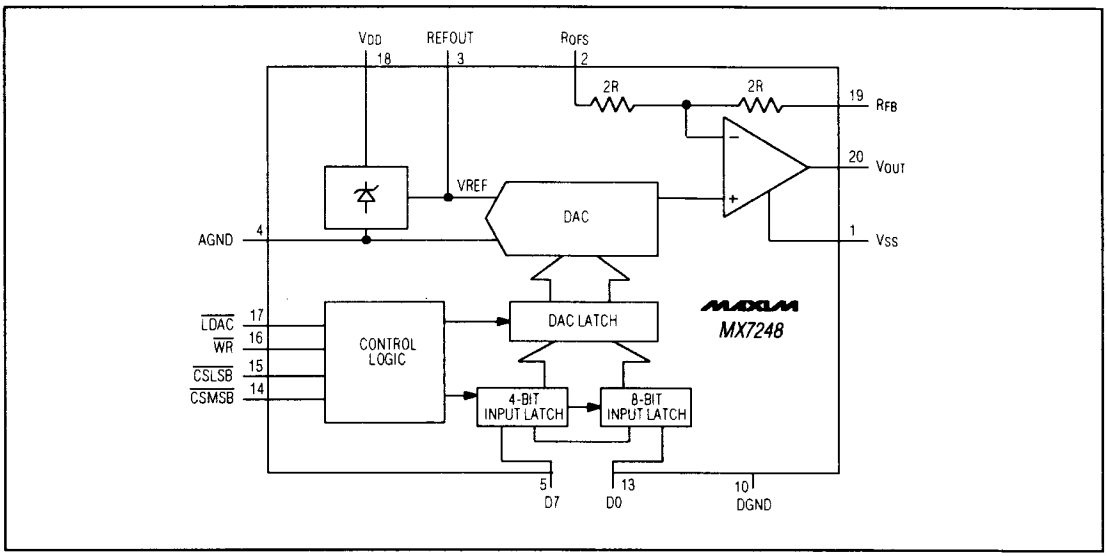


20-PIN LCC

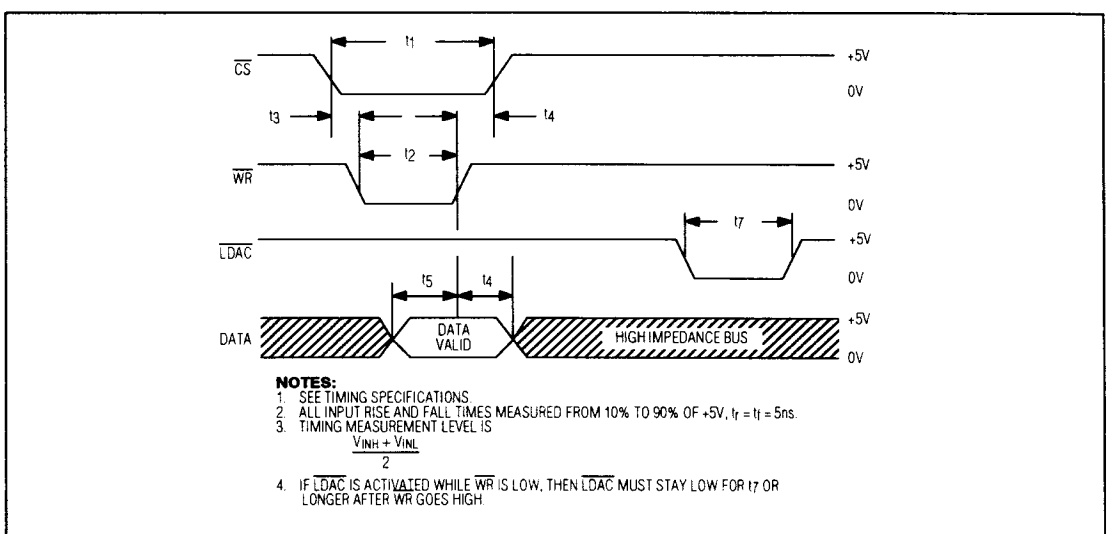
4.2 Functional Diagrams



4.2 Functional Diagrams (continued)



4.3 Timing Diagrams



NOTES:
1. SEE TIMING SPECIFICATIONS.
2. ALL INPUT RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V, $t_r = t_f = 5ns$.
3. TIMING MEASUREMENT LEVEL IS
$$\frac{V_{INH} + V_{INL}}{2}$$
4. IF $\overline{LDAC}$ IS ACTIVATED WHILE $\overline{WR}$ IS LOW, THEN $\overline{LDAC}$ MUST STAY LOW FOR t7 OR LONGER AFTER WR GOES HIGH.

Figure 1a. MX7245 Write-Cycle Timing Diagram

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4.3 Timing Diagrams (continued)

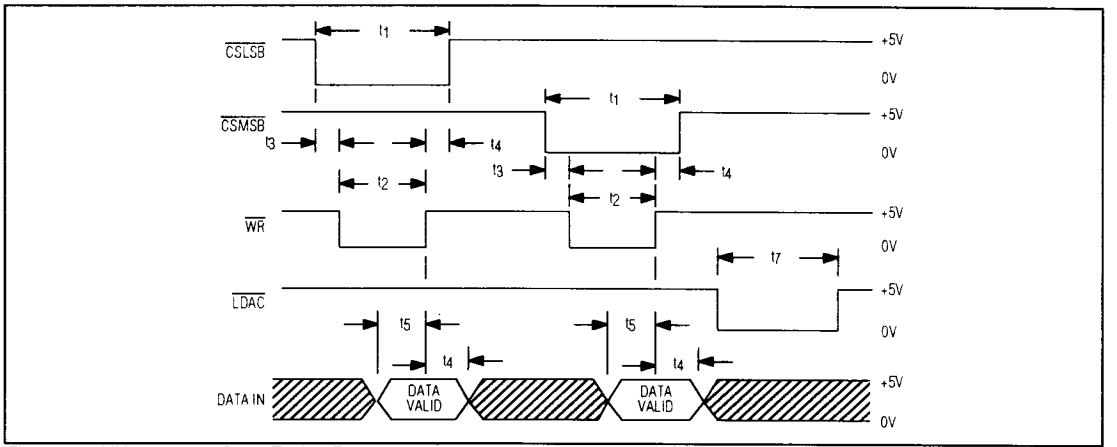

Figure 1b. MX7248 Write-Cycle Timing Diagram

4.4 Mode Control Tables

MX7245				
$\overline{CLR}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both latches transparent
H	H	H	X	Both latches latched
H	H	X	H	Both latches latched
H	H	L	L	Input latches transparent
H	H		L	Input latches latched
H	L	H	H	DAC latches transparent
H		H	H	DAC latches latched

MX7248				
$\overline{CSLSB}$	$\overline{CSMSB}$	$\overline{WR}$	$\overline{LDAC}$	Function
L	H	L	H	Loads LS byte into input latch
L	H		H	Latches LS byte into input latch
	H	L	H	Latches LS byte into input latch
H	L	L	H	Loads MS nibble into input latch
H	L		H	Latches MS nibble into input latch
H		L	H	Latches MS nibble into input latch
H	H	H	L	Loads input latch into DAC latch