19-2439; Rev 1; 8/92

MAXIM

CMOS, µP-Compatible, 12-Bit D/A Converter

1.0 SCOPE

1.1 This specification covers the detail requirements for a monolithic, CMOS, 12-bit, multiplying digital-to-analog converter (DAC) with three 4-bit data registers and a 12-bit DAC register on-chip. The MX7542 interfaces directly with 4- or 8-bit microprocessors. This circuit is processed in accordance with MIL-STD-883 and is fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	MX7542S(X)/883B
-2	MX7542T(X)/883B
-3	MX7542GT(X)/883B

1.3 Package

(X)	Package	Description
Q	Q-16	16-Pin Ceramic Dual-In-Line Package (CERDIP)
D	D-16	16-Pin Side-Brazed Ceramic Package (Ceramic SB)
E	E-20	20-Pin Ceramic Leadless Chip Carrier (LCC)

Note: See *Package Information* section for package drawings and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +7V
V_{DD} to DGND ..... 0V, +7V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{OUT1}, V_{OUT2} to AGND ..... -0.3V, V_{DD}
VREF to AGND ..... -25V to +25V
V_{RFB} to AGND ..... -25V to +25V
Power Dissipation (T_A = +70°C, Tj = +150°C)
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
16-Pin Ceramic SB (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

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1.5 Thermal Resistance

Θ_{JC} = 45°C/W for D-16
Θ_{JC} = 50°C/W for Q-16
Θ_{JC} = 55°C/W for E-20
Θ_{JA} = 95°C/W for D-16
Θ_{JA} = 100°C/W for Q-16
Θ_{JA} = 110°C/W for E-20

2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Resolution (Note 2)	RES		All	1, 2, 3	12		Bits
Relative Accuracy	RA		-1	1, 2, 3	-1	1	LSB
			-2, -3		-0.5	0.5	
Differential Nonlinearity	DNL	Monotonic to 11 bits	-1	1, 2, 3	-2	2	LSB
		Monotonic to 12 bits	-2, -3		-1	1	
Gain Error (Note 3)	AE		-1, -2	1	-12.3	12.3	LSB
				2, 3	-14.5	14.5	
			-3	1	-1	1	
				2, 3	-2	2	
Gain Tempco (Note 2)	TC_{AE}		All	1, 2, 3	-5	5	ppm/°C
Power-Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	V_{DD} = 4.75V to 5.25V	All	1	-0.005	0.005	%/%
				2, 3	-0.01	0.01	
OUT1 Leakage Current	I_{OUT1}	DAC register loaded with all 0s	All	1	-1	1	nA
				2, 3	-200	200	
OUT2 Leakage Current	I_{OUT2}	DAC register loaded with all 1s	All	1	-1	1	nA
				2, 3	-200	200	
Output Current Settling Time	t_{SL}	To ±0.5LSB, OUT1 load is 100Ω || 13pF, output measured from trailing edge of $\overline{WR}$.	All	4		2	µs
Feedthrough Error (Note 4)	FTE	VREF = 10V, 10kHz sine wave	All	4		2.5	mV_{P-P}
Reference Input Resistance	R_{IN}		All	1, 2, 3	8	25	kΩ
Digital Input High Voltage	V_{IH}		All	1, 2, 3	3.0		V
Digital Input Low Voltage	V_{IL}		All	1, 2, 3		0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}	All	1, 2, 3	-1	1	µA
Digital Input Capacitance	C_{IN}		All	4		8	pF

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TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS MAX	UNITS
Output Capacitance	C_{OUT1}	Digital inputs at V_{IH}, DAC register loaded with all 1s	All	4		260	pF
		Digital inputs at V_{IL}, DAC register loaded with all 0s				75	
	C_{OUT2}	Digital inputs at V_{IH}, DAC register loaded with all 1s				75	pF
		Digital inputs at V_{IL}, DAC register loaded with all 0s				260	
Write Pulse Width (Note 5)	t_{WR}		All	9	220		ns
Address to Write-Hold Time (Note 5)	t_{AWH}		All	9	80		ns
Chip Select to Write-Hold Time (Note 5)	t_{CWH}		All	9	100		ns
Minimum Clear Pulse Width (Note 5)	t_{CLR}		All	9	300		ns
Chip Select to Write-Setup Time (Note 5)	t_{CWS}	Byte loading	All	9	130		ns
Address Valid to Write-Setup Time (Note 5)	t_{AWS}	Byte loading	All	9	180		ns
Data-Setup Time (Note 5)	t_{DS}		All	9	350		ns
Data-Hold Time (Note 5)	t_{DH}		All	9	65		ns
Chip Select to Write-Setup Time (Note 5)	t_{CWS}	DAC loading	All	9	150		ns
Address Valid to Write-Setup Time (Note 5)	t_{AWS}	DAC loading	All	9	240		ns
Supply Current	I_{DD}	Digital inputs = V_{IH} or V_{IL}	All	1, 2, 3		2.5	mA

Note 1: V_{DD} = +5V, V_{OUT1} = V_{OUT2} = 0V, VREF = +10V, unless otherwise noted.
Note 2: Characteristics supplied for use as a typical design limit, but not production tested.
Note 3: Measured using internal feedback resistor; includes effects of leakage current and gain TC.
Note 4: Feedthrough error can be reduced by connecting the lid of the ceramic SB package to ground.
Note 5: Timing shown in section 4.3.

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3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 2.

3.4 Groups C and D inspections:
a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test (Method 1005 of MIL-STD-883):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,* 2, 3
Group A Test Requirements (Method 5005)	1, 2, 3, 4,** 9
Groups C and D End-Point Electrical Parameters (Method 5005)	1

* PDA applies to Subgroup 1 only.
** Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 5 units.

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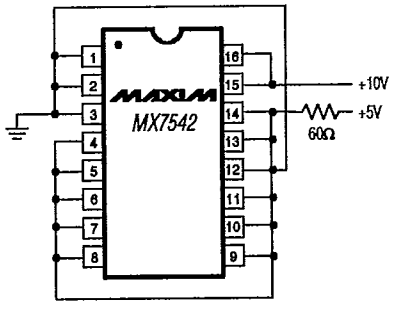
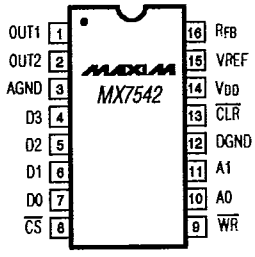
4.0 Life Test/Burn-In Circuit

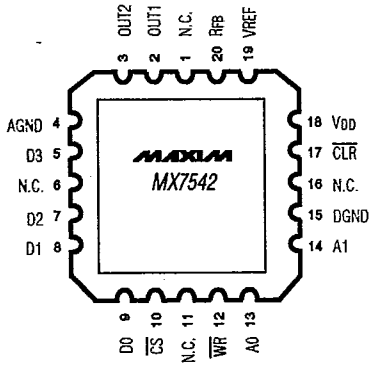


4.1 Pin Configurations

TOP VIEW



16-PIN CERAMIC SB/CERDIP



20-PIN LCC

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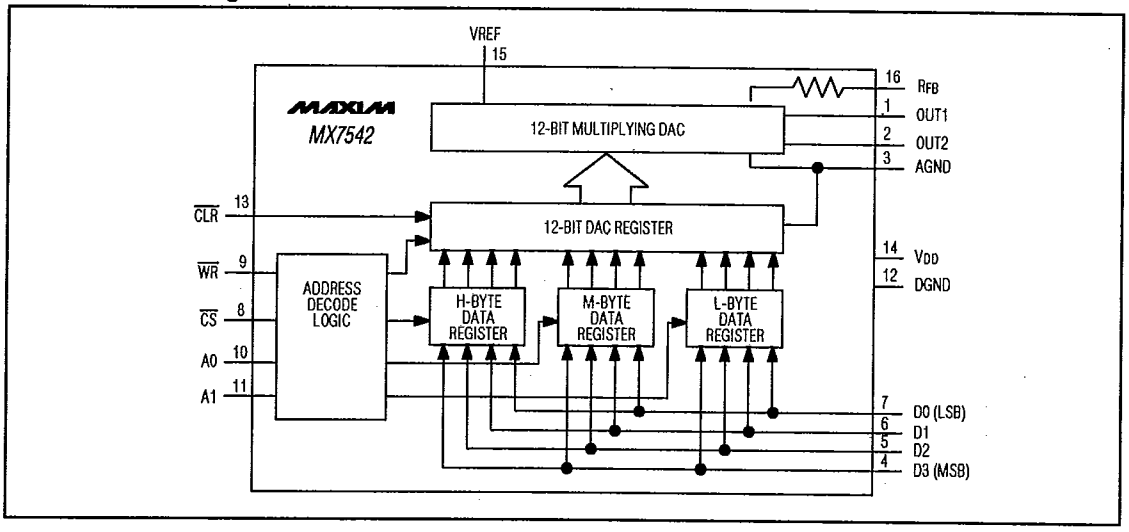
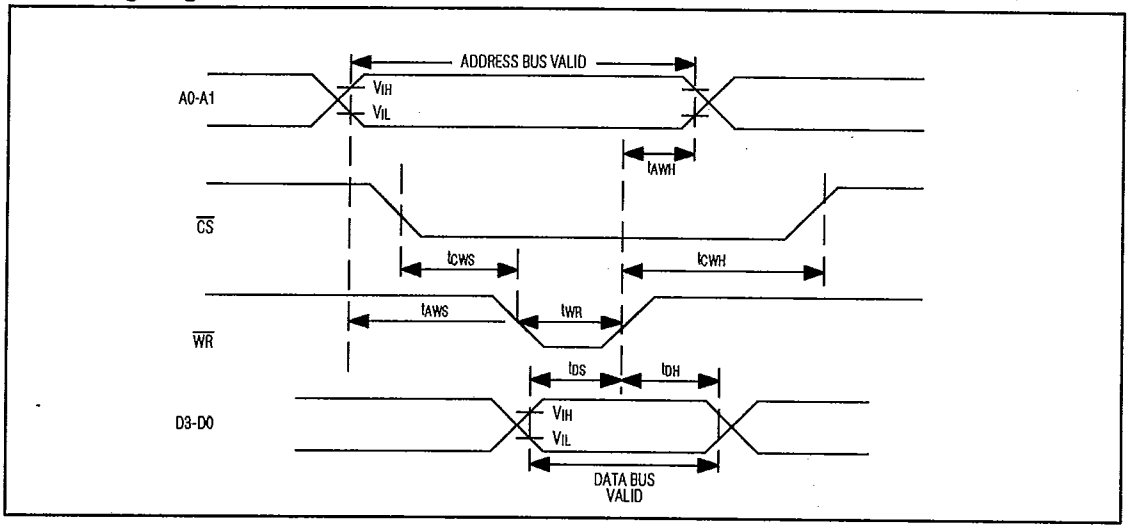
4.2 Functional Diagram



4.3 Timing Diagram



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4.4 Mode Control Table

MX7542 Control Inputs					MX7542 Operation	
A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Resets DAC 12-bit register to code all 0s	
X	X	1	X	1	No operation — device not selected	
0	0	0	↑	1	Load low-byte data register on edge as shown	Load applicable data register with data at D0-D3
0	1	0	↑	1	Load middle-byte data register on edge as shown	
1	0	0	↑	1	Load high-byte data register on edge as shown	
1	1	0	⊓	1	Load 12-bit DAC register with data in low-byte, middle-byte, and high-byte data registers	

X = Don't care, ↑ = Logic 0 to 1 transition

NOTE: MSB → $\frac{XXXX}{HIGHBYTE}$ $\frac{XXXX}{MIDDLEBYTE}$ $\frac{XXXX}{LOWBYTE}$ ← LSB

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