Index of /ds/FS/

Name	Last modified	Size	Description
Parent Directory			
FSB560.pdf	22-Dec-99 00:08	208K	
FSB560A.pdf	22-Dec-99 00:08	208K	
FSB619.pdf	22-Dec-99 00:08	27K	
FSB660.pdf	22-Dec-99 00:08	209K	
FSB660A.pdf	22-Dec-99 00:08	209K	
FSB6726.pdf	22-Dec-99 00:08	23K	
FSBCW30.pdf	22-Dec-99 00:08	43K	
FST16209.pdf	31-Dec-99 00:00	134K	
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FSTD16211.pdf	21-Dec-99 00:00	227K
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FSTU6800.pdf	31-Dec-99 00:00	181K
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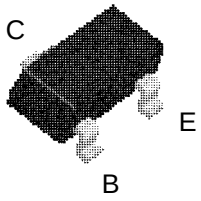
FAIRCHILD SEMICONDUCTOR TM

July 1998

FSB560 / FSB560A



SuperSOT™-3 (SOT-23)

NPN Low Saturation Transistor

These devices are designed with high current gain and low saturation voltage with collector currents up to 2A continuous.

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	FSB560/FSB560A	Units
V_{CEO}	Collector-Emitter Voltage	60	V
V_{CBO}	Collector-Base Voltage	80	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current - Continuous	2	A
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150°C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max	Units
		FSB560/FSB560A	
P_D	Total Device Dissipation	500	mW
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	250	°C/W

NPN Low Saturation Transistor
(continued)

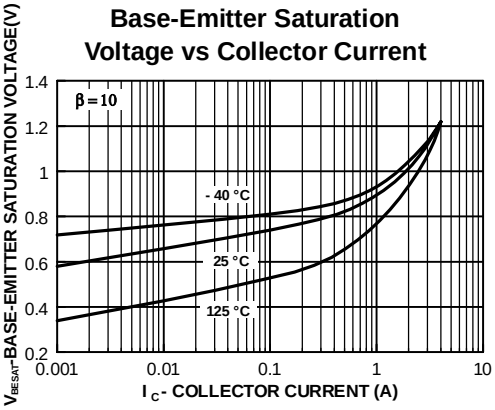
Electrical Characteristics
$T_{A = 25°C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 10 mA	60		V
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 100 µA	80		V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = 100 µA	5		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 30 V V_{CB} = 30 V, T_A=100°C		100 10	nA uA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 4V		100	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	I_C = 100 mA, V_{CE} = 2 V I_C=500mA, V_{CE} =2V **FSB560** **FSB560A** I_C = 1 A, V_{CE} = 2 V I_C = 2 A, V_{CE} = 2 V	70 100 250 80 40	 300 550	-
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 1 A, I_B = 100 mA I_C = 2 A, I_B=200 mA **FSB560** **FSB560A**		300 350 300	mV
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 1 A, I_B = 100 mA		1.25	V
$V_{BE(on)}$	Base-Emitter On Voltage	I_C = 1 A, V_{CE} = 2 V		1	V
SMALL SIGNAL CHARACTERISTICS					
C_{obo}	Output Capacitance	V_{CB} = 10 V, I_E = 0, f = 1MHz		30	pF
f_T	Transition Frequency	I_C = 100 mA,V_{CE} = 5 V, f=100MHz	75		-

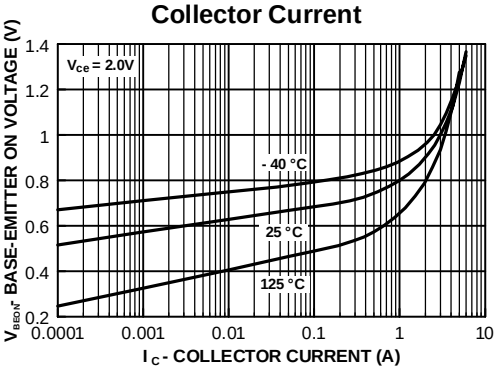
*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

Typical Characteristics

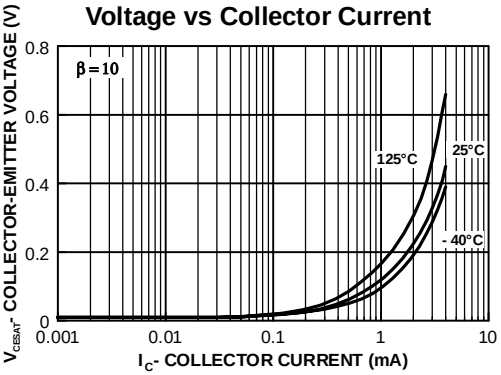
Base-Emitter Saturation Voltage vs Collector Current



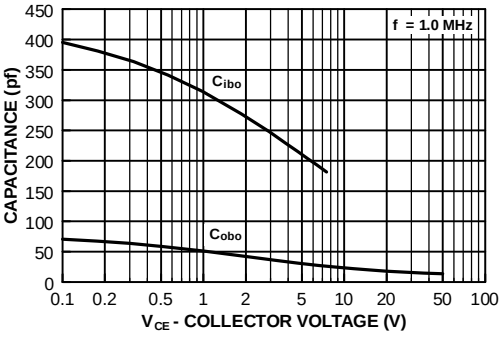
Base-Emitter On Voltage vs. Collector Current



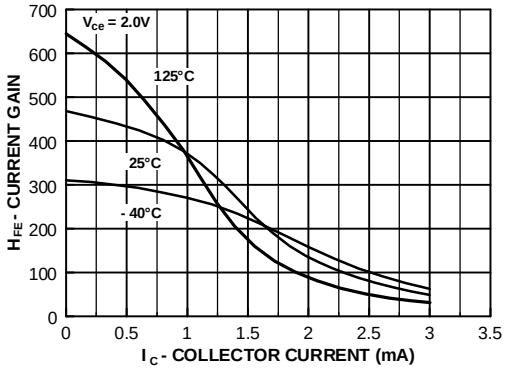
Collector-Emitter Saturation Voltage vs Collector Current



Input/Output Capacitance vs. Reverse Bias Voltage



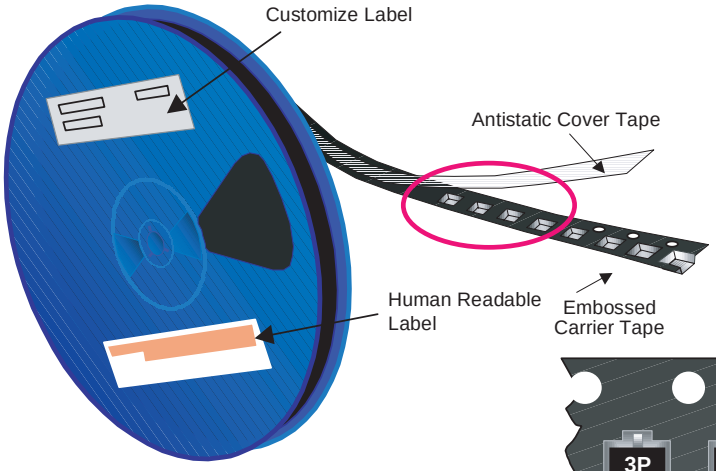
Current Gain vs. Collector Current



SuperSOT™-3 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

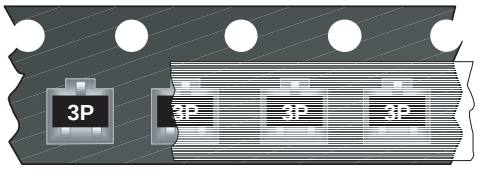
SSOT-3 Packaging Configuration: Figure 1.0



Packaging Description:

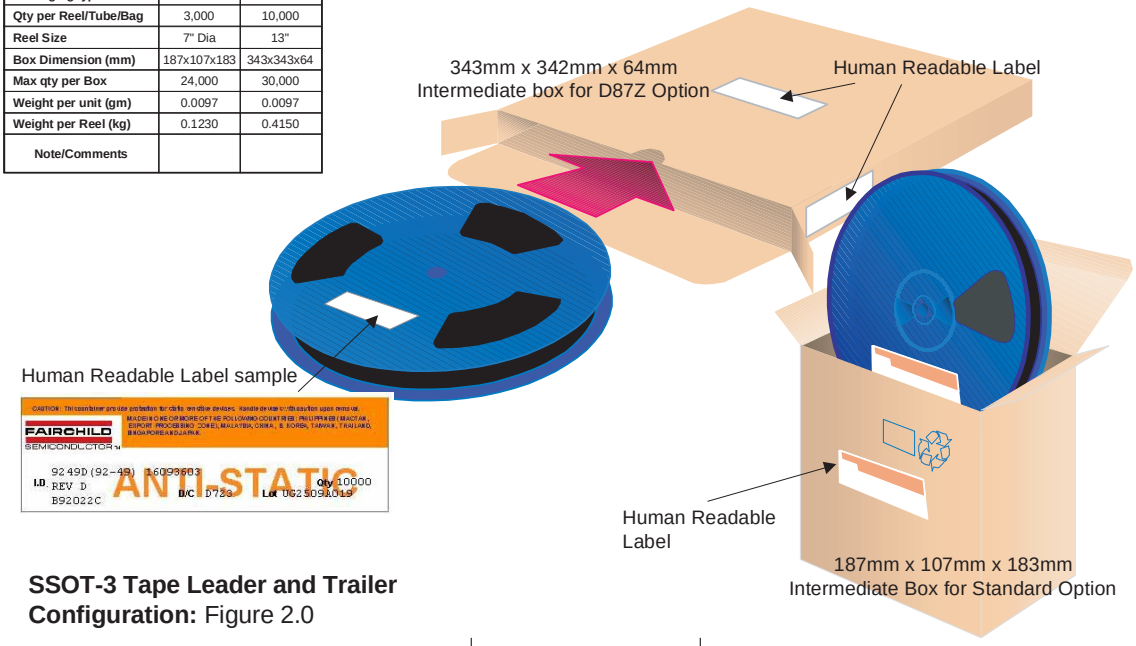
SSOT-3 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 177cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 10,000 units per 13" or 330cm diameter reel. This and some other options are described in the Packaging Information table.

These full reels are individually labeled and placed inside a standard intermediate made of recyclable corrugated brown paper with a Fairchild logo printing. One pizza box contains eight reels maximum. And these intermediate boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

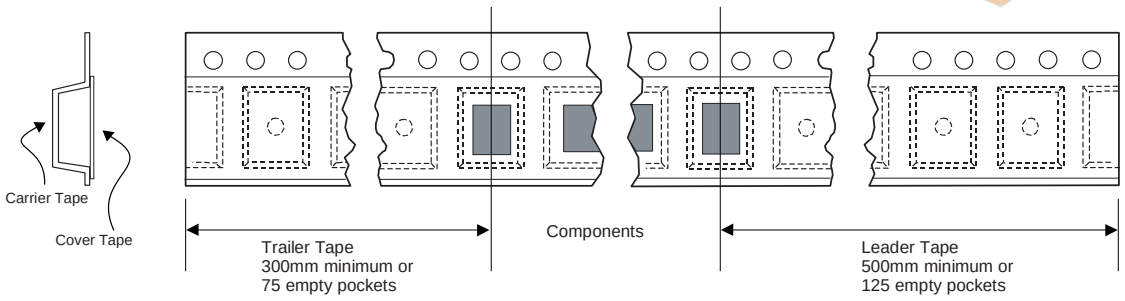


SSOT-3 Std Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	187x107x183	343x343x64
Max qty per Box	24,000	30,000
Weight per unit (gm)	0.0097	0.0097
Weight per Reel (kg)	0.1230	0.4150
Note/Comments		

SSOT-3 Std Unit Orientation

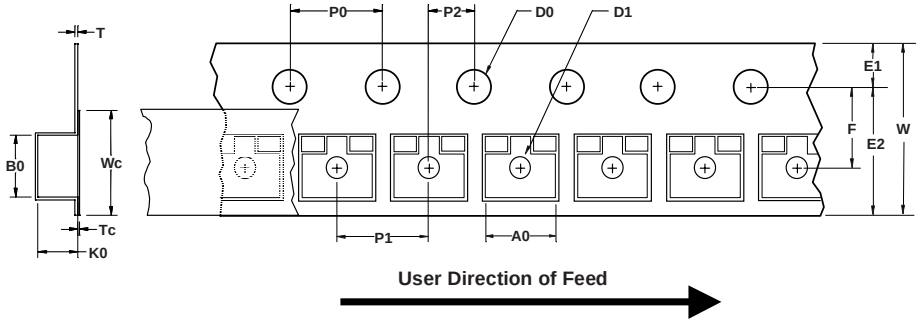


SSOT-3 Tape Leader and Trailer Configuration: Figure 2.0



SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

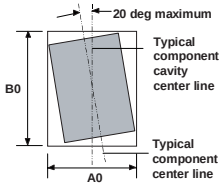
SSOT-3 Embossed Carrier Tape
Configuration: Figure 3.0



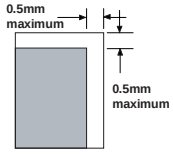
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SSOT-3 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation

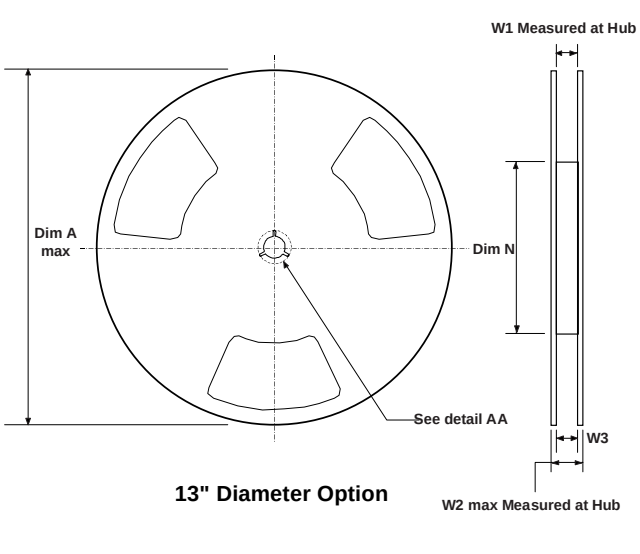


Sketch B (Top View)
Component Rotation

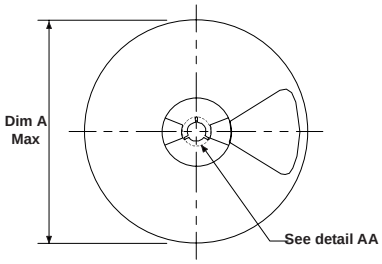


Sketch C (Top View)
Component lateral movement

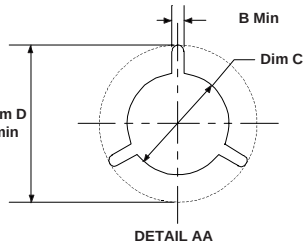
SSOT-3 Reel Configuration: Figure 4.0



13" Diameter Option



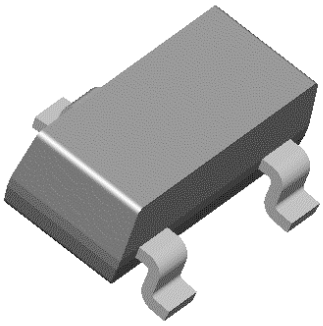
7" Diameter Option

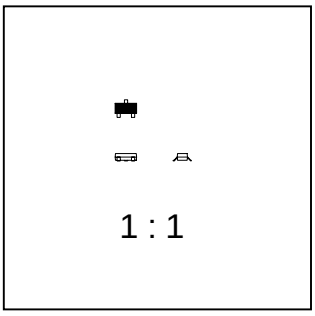


Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9

SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

SuperSOT™-3 (FS PKG Code 32)

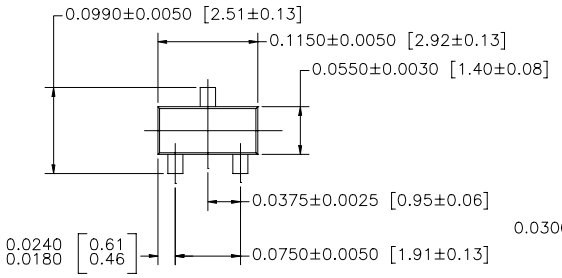


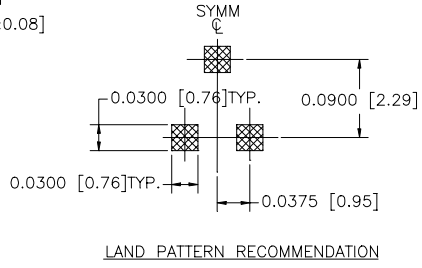


Scale 1:1 on letter size paper

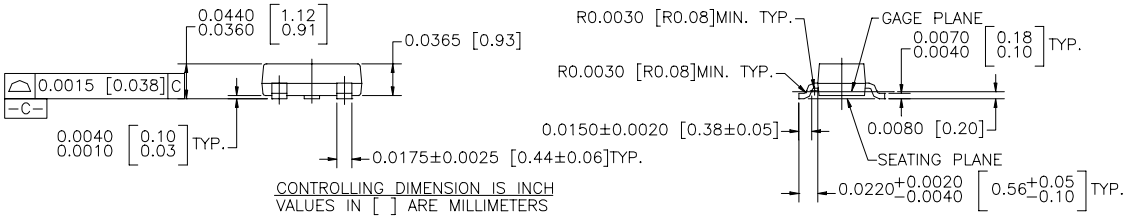
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0097





LAND PATTERN RECOMMENDATION



NOTES : UNLESS OTHERWISE SPECIFIED

SUPER SOT , 3 LEADS

1. STANDARD LEAD FINISH TO BE 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.
2. NO JEDEC REGISTRATION AS OF DEC. 1995.

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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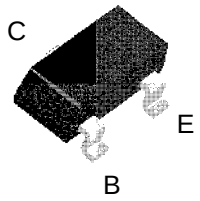
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAIRCHILD SEMICONDUCTOR™

Discrete Power & Signal Technologies

July 1998

FSB619



SuperSOT™-3 (SOT-23)

NPN Low Saturation Transistor

These devices are designed with high current gain and low saturation voltage with collector currents up to 3A continuous.

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	FSB619	Units
V_{CEO}	Collector-Emitter Voltage	50	V
V_{CBO}	Collector-Base Voltage	50	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current - Continuous	2	A
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150°C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max	Units
		FSB619	
P_D	Total Device Dissipation* Derate above 25°C	500 4	mW mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	250	°C/W

*Device mounted on FR-4 PCB 4.5" X 5"; mounting pad 0.02 in^2 of 2oz copper.

NPN Low Saturation Transistor

(continued)

Electrical Characteristics

$T_{A = 25°C \text{ unless otherwise noted}}$

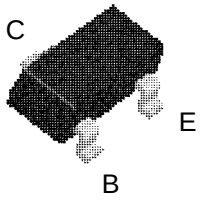
Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 10 mA	50		V
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 100 μA	50		V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = 100 μA	5		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 40 V		100	nA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 4V		100	nA
I_{CES}	Collector Emitter Cutoff Current	V_{CES} = 40 V		100	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	I_C = 10 mA, V_{CE} = 2V I_C = 200 mA, V_{CE} = 2V I_C = 1A, V_{CE} = 2V I_C = 2A, V_{CE} = 2V	200 300 200 100		-
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 100 mA, I_B = 10 mA I_C = 1 A, I_B = 10 mA I_C = 2 A, I_B = 50 mA		20 235 320	mV
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 2 A, I_B = 50 mA		1	V
$V_{BE(on)}$	Base-Emitter On Voltage	I_C = 2 A, V_{CE} = 2 V		1	V
SMALL SIGNAL CHARACTERISTICS					
C_{obo}	Output Capacitance	V_{CB} = 10 V, I_E = 0, f = 1MHz		30	pF
f_T	Transition Frequency	I_C = 50 mA,V_{CE} = 10 V, f=100MHz	100		-

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FAIRCHILD SEMICONDUCTOR TM

July 1998

FSB660 / FSB660A



SuperSOT™-3 (SOT-23)

PNP Low Saturation Transistor

These devices are designed with high current gain and low saturation voltage with collector currents up to 2A continuous.

Absolute Maximum Ratings*

$T_{A = 25°C}$ unless otherwise noted

Symbol	Parameter	FSB660/FSB660A	Units
V_{CEO}	Collector-Emitter Voltage	60	V
V_{CBO}	Collector-Base Voltage	80	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current - Continuous	2	A
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150°C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

$T_{A = 25°C}$ unless otherwise noted

Symbol	Characteristic	Max	Units
		FSB660/FSB660A	
P_D	Total Device Dissipation	500	mW
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	250	°C/W

PNP Low Saturation Transistor
(continued)

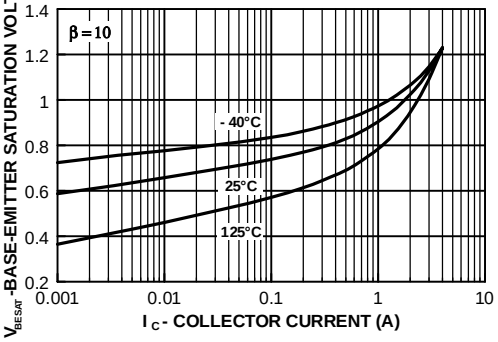
Electrical Characteristics
$T_{A = 25°C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 10 mA	60		V
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 100 µA	80		V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = 100 µA	5		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 30 V V_{CB} = 30 V, T_A=100°C		100 10	nA uA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 4V		100	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	I_C = 100 mA, V_{CE} = 2 V I_C=500mA, V_{CE} =2V **FSB660** **FSB660A** I_C = 1 A, V_{CE} = 2 V I_C = 2 A, V_{CE} = 2 V	70 100 250 80 40	 300 550	-
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 1 A, I_B = 100 mA I_C = 2 A, I_B=200 mA **FSB660** **FSB660A**		300 350 300	mV
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 1 A, I_B = 100 mA		1.25	V
$V_{BE(on)}$	Base-Emitter On Voltage	I_C = 1 A, V_{CE} = 2 V		1	V
SMALL SIGNAL CHARACTERISTICS					
C_{obo}	Output Capacitance	V_{CB} = 10 V, I_E = 0, f = 1MHz		30	pF
f_T	Transition Frequency	I_C = 100 mA,V_{CE} = 5 V, f=100MHz	75		-

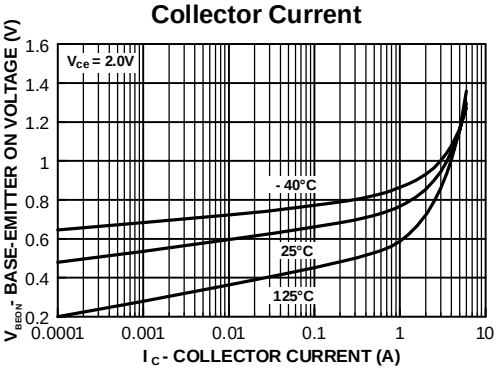
*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

Typical Characteristics

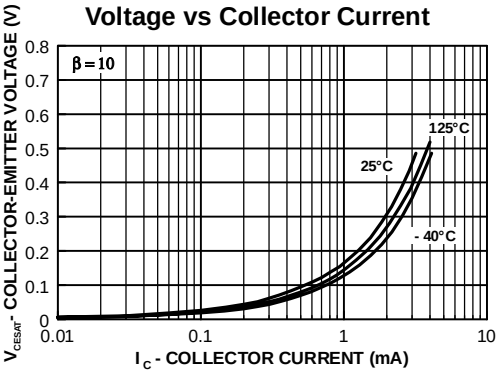
Base-Emitter Saturation Voltage vs Collector Current



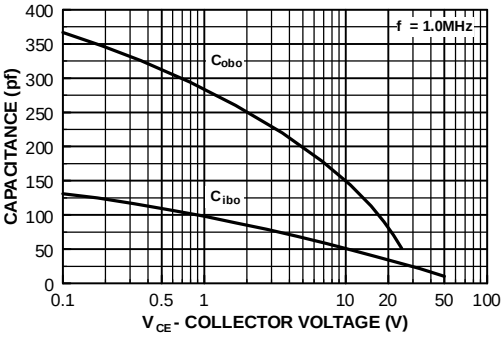
Base-Emitter On Voltage vs. Collector Current



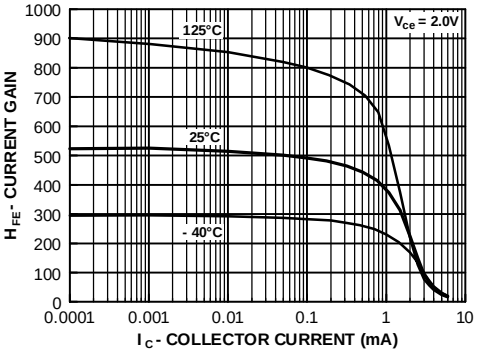
Collector-Emitter Saturation Voltage vs Collector Current



Input/Output Capacitance vs. Reverse Bias Voltage



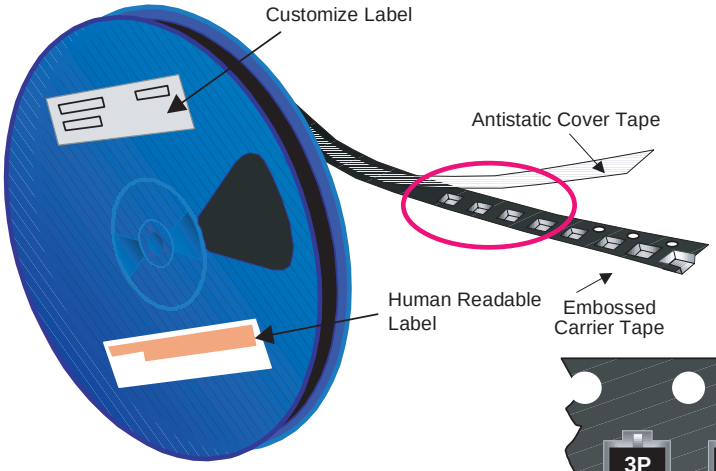
Current Gain vs. Collector Current



SuperSOT™-3 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

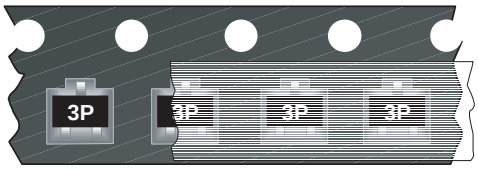
SSOT-3 Packaging Configuration: Figure 1.0



Packaging Description:

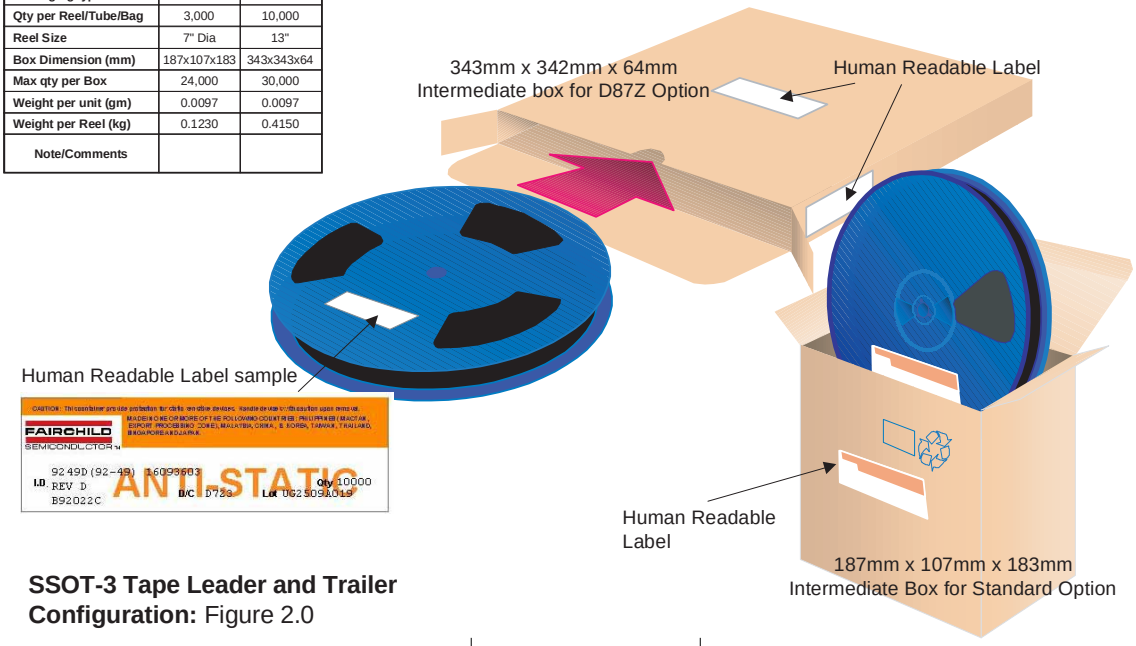
SSOT-3 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 177cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 10,000 units per 13" or 330cm diameter reel. This and some other options are described in the Packaging Information table.

These full reels are individually labeled and placed inside a standard intermediate made of recyclable corrugated brown paper with a Fairchild logo printing. One pizza box contains eight reels maximum. And these intermediate boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

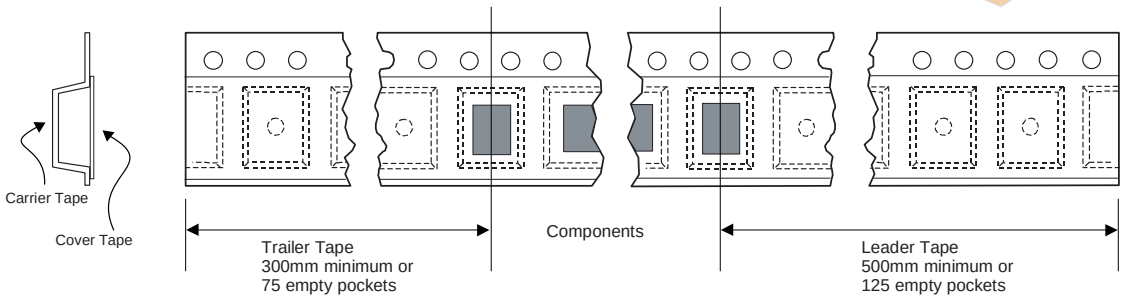


SSOT-3 Std Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	187x107x183	343x343x64
Max qty per Box	24,000	30,000
Weight per unit (gm)	0.0097	0.0097
Weight per Reel (kg)	0.1230	0.4150
Note/Comments		

SSOT-3 Std Unit Orientation

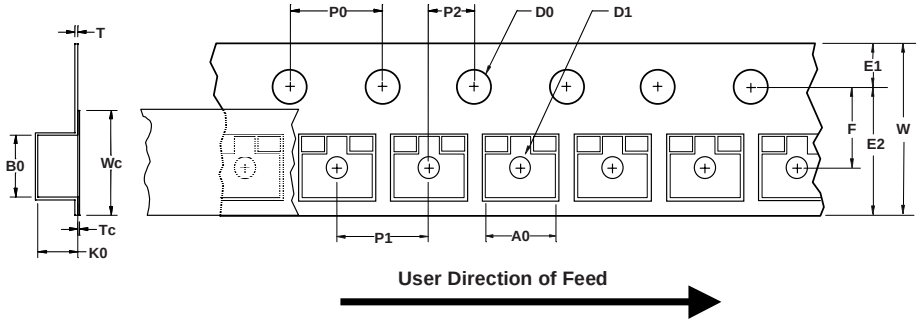


SSOT-3 Tape Leader and Trailer Configuration: Figure 2.0



SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

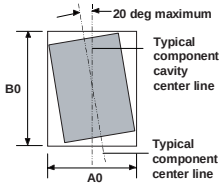
SSOT-3 Embossed Carrier Tape
Configuration: Figure 3.0



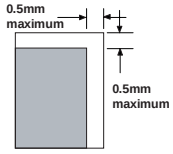
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SSOT-3 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation

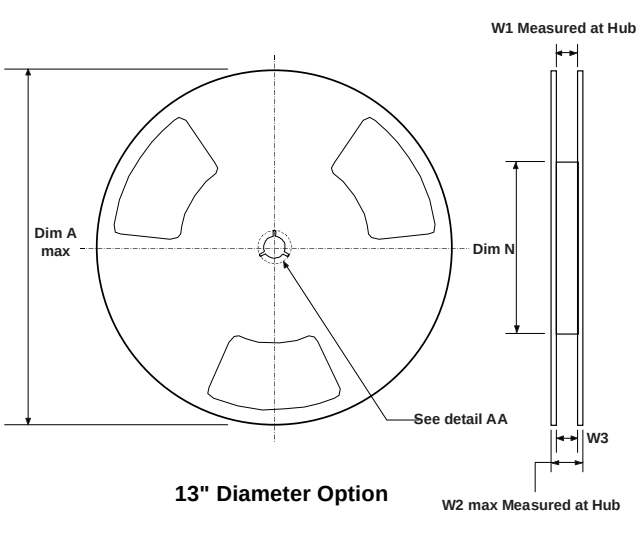


Sketch B (Top View)
Component Rotation

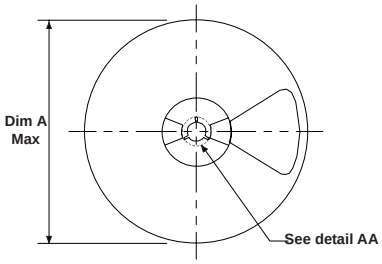


Sketch C (Top View)
Component lateral movement

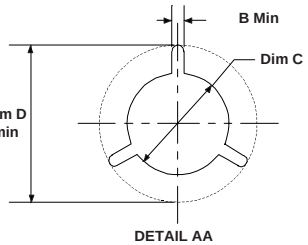
SSOT-3 Reel Configuration: Figure 4.0



13" Diameter Option



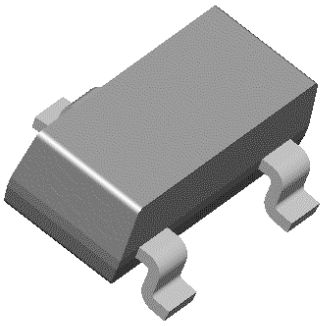
7" Diameter Option

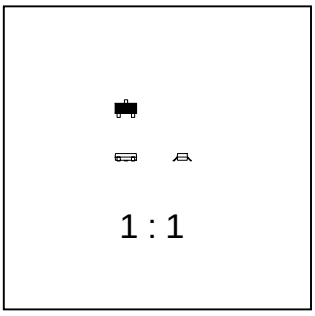


Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9

SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

SuperSOT™-3 (FS PKG Code 32)

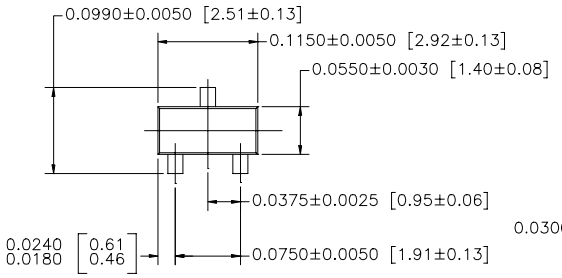


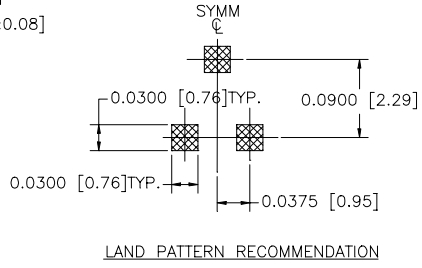


Scale 1:1 on letter size paper

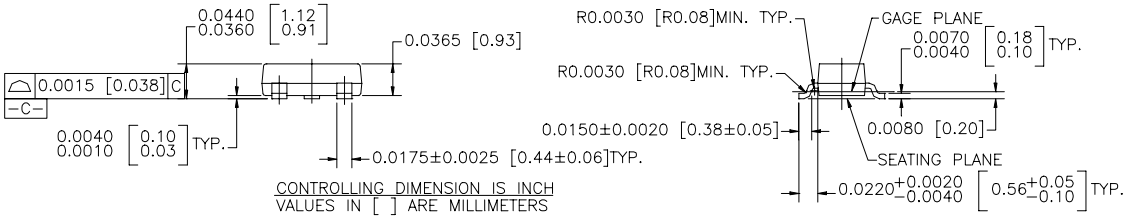
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0097





LAND PATTERN RECOMMENDATION



NOTES : UNLESS OTHERWISE SPECIFIED

SUPER SOT , 3 LEADS

1. STANDARD LEAD FINISH TO BE 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.
2. NO JEDEC REGISTRATION AS OF DEC. 1995.

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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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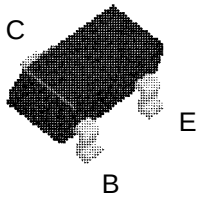

SuperSOT™-3

PNP General Purpose Amplifier

This device is designed for general purpose medium power amplifiers and switches requiring collector currents to 1.0 A. Sourced from Process 77.

Absolute Maximum Ratings* $T_{A = 25°C \text{ unless otherwise noted}}$

Symbol	Parameter	FSB660/FSB660A	Units
V_{CEO}	Collector-Emitter Voltage	30	V
V_{CBO}	Collector-Base Voltage	40	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current - Continuous	1.5	A
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150°C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics $T_{A = 25°C \text{ unless otherwise noted}}$

Symbol	Characteristic	Max	Units
		FSB6726	
P_D	Total Device Dissipation	500	mW
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	250	°C/W

PNP General Purpose Amplifier
(continued)

Electrical Characteristics
$T_{A = 25°C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 10 mA	30		V
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 100 μA	40		V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = 100 μA	5		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 40 V		100	nA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 5V		100	nA
ON CHARACTERISTICS*					
h_{FE}	DC Current Gain	I_C = 100 mA, V_{CE} = 1 V I_C = 1 A, V_{CE} = 1V	60 50	 250	- -
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 1 A, I_B = 100 mA		500	mV
$V_{BE(on)}$	Base-Emitter On Voltage	I_C = 1 A, V_{CE} = 1 V		1.2	V
SMALL SIGNAL CHARACTERISTICS					
C_{cb}	Collector-Base Capacitance	V_{CB} = 10 V, f = 1MHz		30	pF
hfe	Small Signal Current Gain	I_C= 50 mA,V_{CE} = 10V, f=20MHz	2.5	25	-

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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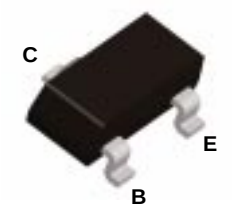
Discrete POWER & Signal Technologies

FSBCW30



SuperSOT™-3

PNP General Purpose Amplifier

This device is designed for general purpose medium power amplifiers and switches requiring collector currents to 300 mA. Sourced from Process 68. See BC857A for characteristics.

Absolute Maximum Ratings* TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	32	V
V_{CBO}	Collector-Base Voltage	32	V
V_{EBO}	Emitter-Base Voltage	5.0	V
I_C	Collector Current - Continuous	500	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics TA = 25°C unless otherwise noted

Symbol	Characteristic	Max	Units
		FSBCW30	
P_D	Total Device Dissipation Derate above 25°C	500 4	mW mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	250	°C/W

*Device mounted on FR-4 PCB 4.5" x 5"; mounting pad 0.02 in^2 of 2oz copper.

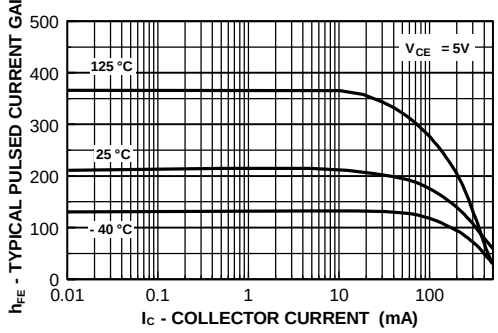
PNP General Purpose Amplifier
(continued)

Electrical Characteristics
TA = 25°C unless otherwise noted

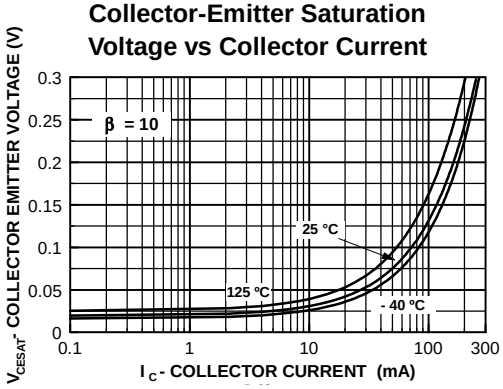
Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 2.0 mA, I_B = 0	32		V
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 10 µA, I_E = 0	32		V
BV_{CES}	Collector-Emitter Breakdown Voltage	I_C = 10 µA, I_E = 0	32		V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = 10 µA, I_C = 0	5.0		V
I_{CBO}	Collector-Cutoff Current	V_{CB} = 32 V, I_E = 0 V_{CB} = 32 V, I_E = 0, T_A = +100 °C		100 10	nA µA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain	V_{CE} = 5.0 V, I_C = 2.0 mA	215	500	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 0.5 mA		0.30	V
$V_{BE(on)}$	Base-Emitter On Voltage	V_{CE} = 5.0 V, I_C = 2.0 mA	0.60	0.75	V
SMALL SIGNAL CHARACTERISTICS					
NF	Noise Figure	V_{CE} = 5.0 V, I_C = 200 µA, R_S = 2.0 kΩ, f = 1.0 kHz, B_W = 200 Hz		10	dB

Typical Characteristics

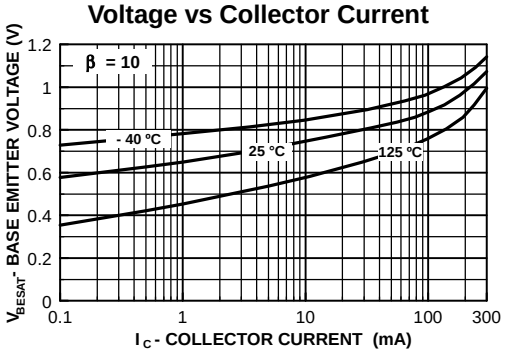
Typical Pulsed Current Gain vs Collector Current



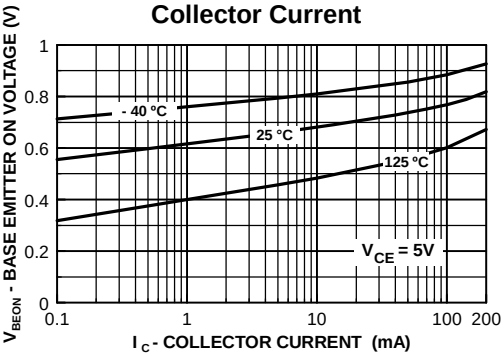
Collector-Emitter Saturation Voltage vs Collector Current



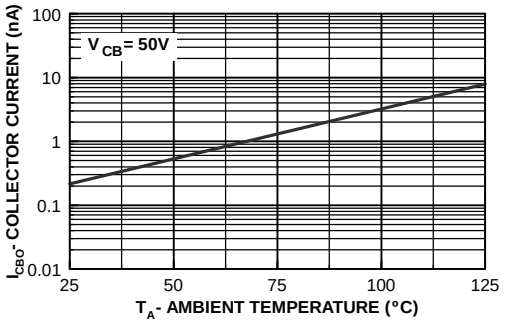
Base-Emitter Saturation Voltage vs Collector Current



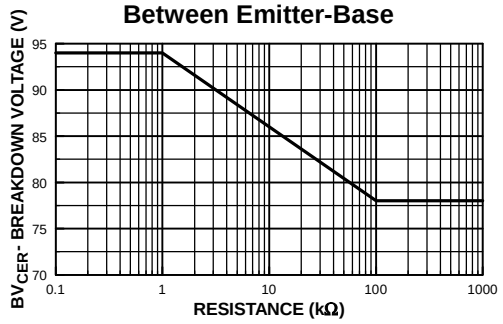
Base Emitter ON Voltage vs Collector Current



Collector-Cutoff Current vs. Ambient Temperature

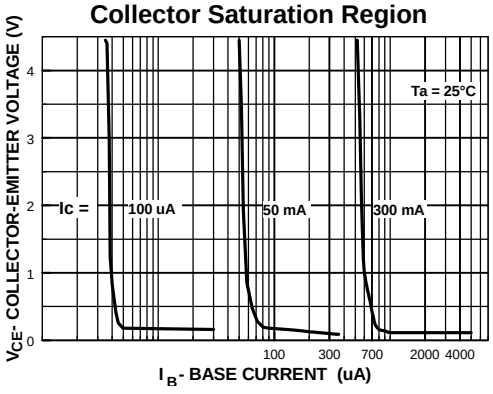


Collector-Emitter Breakdown Voltage with Resistance Between Emitter-Base

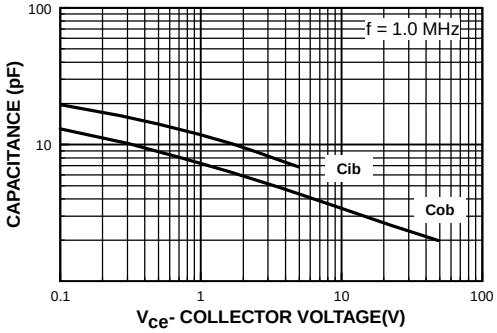


Typical Characteristics (continued)

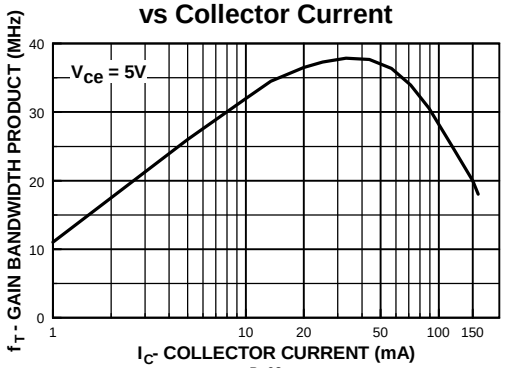
Collector Saturation Region



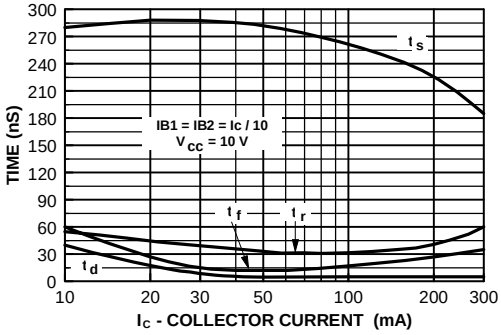
Input and Output Capacitance vs Reverse Voltage



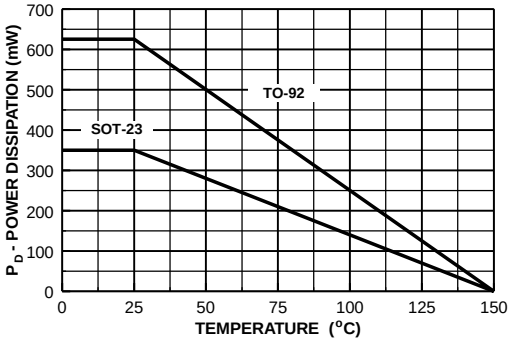
Gain Bandwidth Product vs Collector Current



Switching Times vs Collector Current



Power Dissipation vs Ambient Temperature



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAIRCHILD SEMICONDUCTOR™

September 1997
Revised December 1999

FST16209
18-Bit Bus Exchange Switch

General Description

The Fairchild Switch FST16209 provides 18-bits of high-speed CMOS TTL-compatible bus switching or exchanging. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device operates as a 18-bit bus switch or a 9-bit bus exchanger, which allows data exchange between the four signal ports via the data-select terminals.

Features

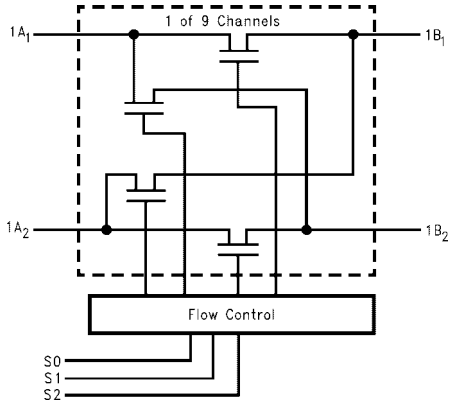
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

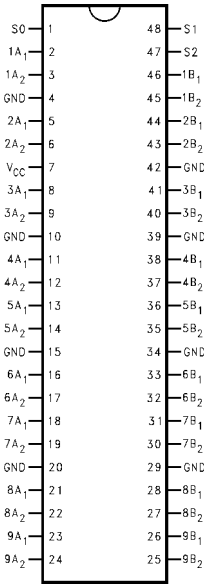
Order Number	Package Number	Package Description
FST16209MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16209MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Truth Table

S2	S1	S0	A_1	A_2	Function
L	L	L	Z	Z	Disconnect
L	L	H	B_1	Z	$A_1 = B_1$
L	H	L	B_2	Z	$A_1 = B_2$
L	H	H	Z	B_1	$A_2 = B_1$
H	L	L	Z	B_2	$A_2 = B_2$
H	L	H	Z	Z	Disconnect
H	H	L	B_1	B_2	$A_1 = B_1$, $A_2 = B_2$
H	H	H	B_2	B_1	$A_1 = B_2$, $A_2 = B_1$

Pin Descriptions

Pin Name	Description
S2, S1, S0	Data-select inputs
A_1, A_2	Bus A
B_1, B_2	Bus B

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN})(Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OFF}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		14	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,^\circ C$ to $+85\,^\circ C$, $C_L = 50pF$, $R_U = R_D = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PHL}, t_{PLH}	Prop Delay S to Bus	1.5	7.0		7.0	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time, S to A or B	1.5	7.5		8.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time S to A or B	1.0	8.5		9.0	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

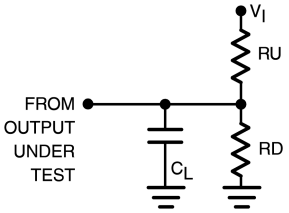
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	10		pF	V_{CC} = 5.0V, S0, S1, and S2 = GND

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

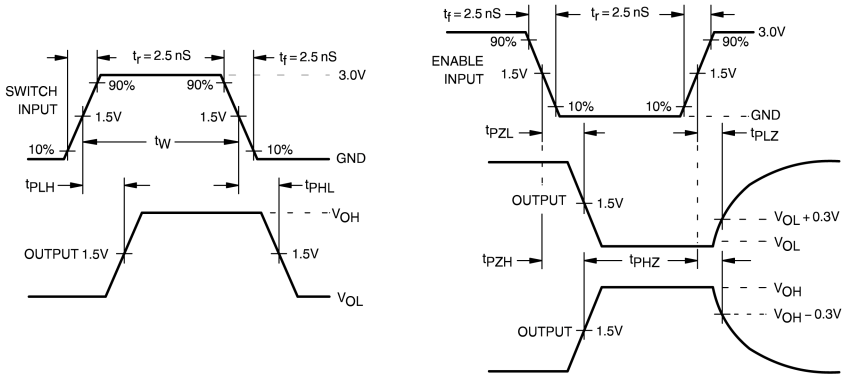
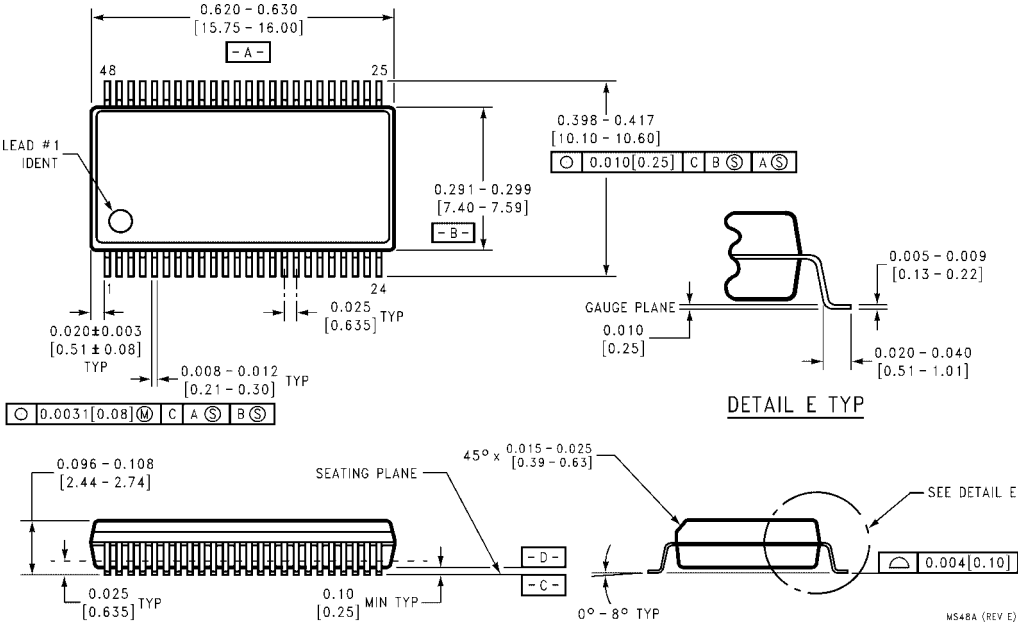


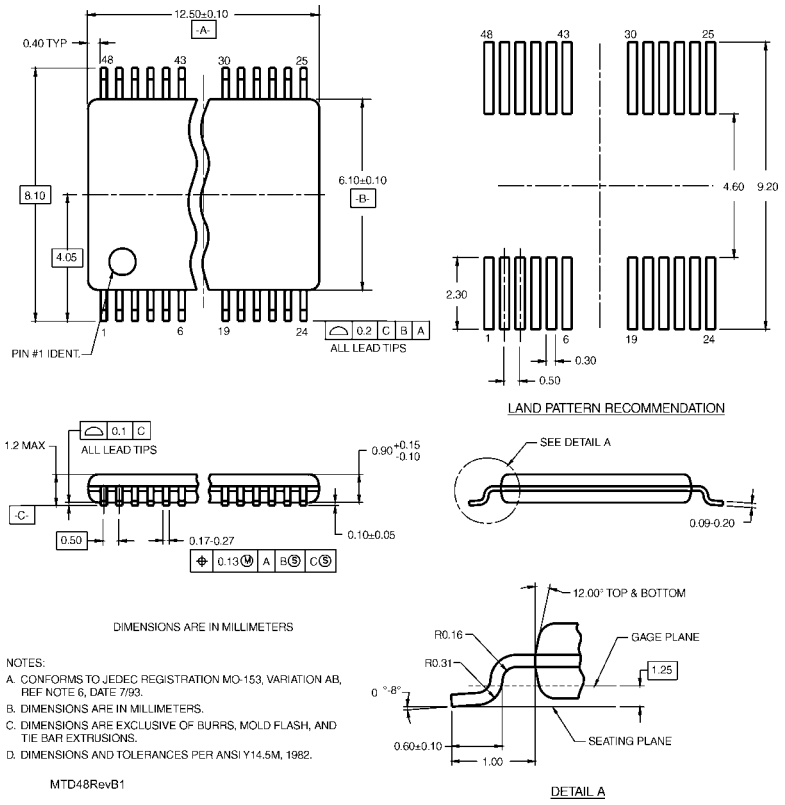
FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

November 1998
Revised December 1999

FST16210
20-Bit Bus Switch

General Description

The Fairchild Switch FST16210 provides 20-Bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 10-bit or 20-Bit bus switch. When $\overline{OE}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, Port 2A is connected to Port 2B.

Features

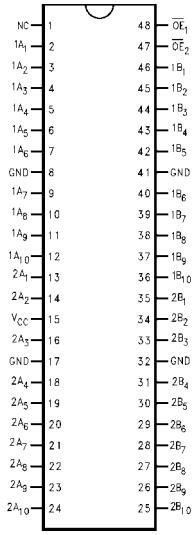
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

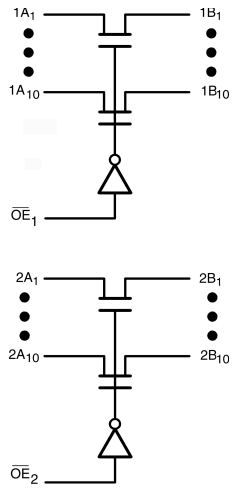
Order Number	Package Number	Package Description
FST16210MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Logic Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating ($V_{CC)}$)	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held high or low. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
Δ I_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\ °C$ to $+85\ °C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1, Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	6.0		6.5	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1, Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	7.0		7.2	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1, Figure 2

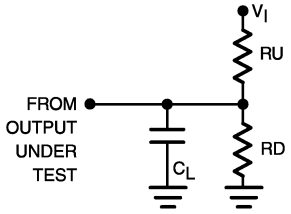
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	6		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

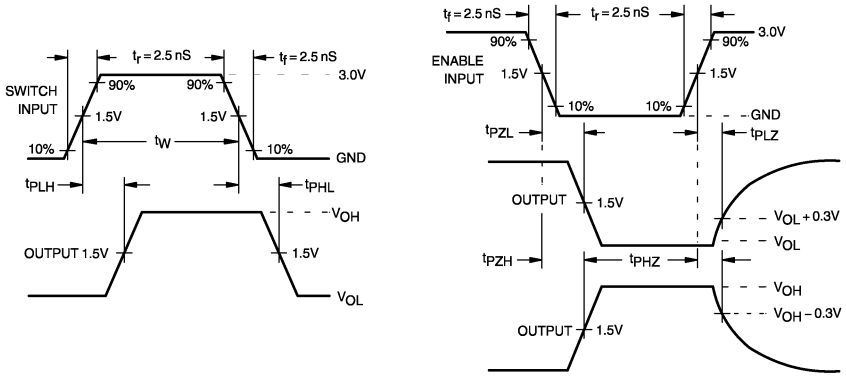
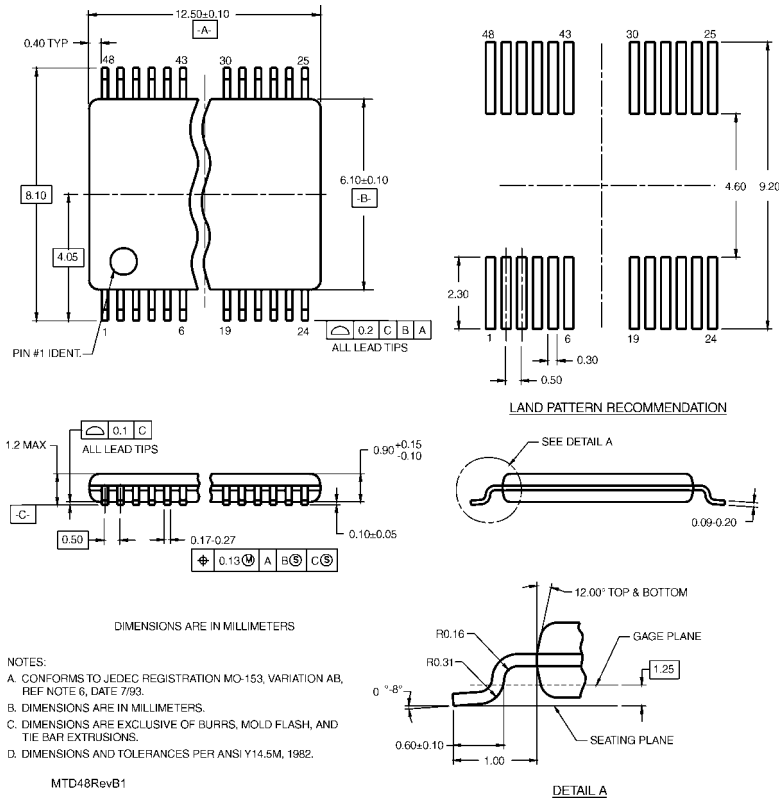


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384(FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

July 1997
Revised December 1999

FST16211
24-Bit Bus Switch

General Description

The Fairchild Switch FST16211 provides 24-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 12-bit or 24-bit bus switch. When $\overline{OE}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, Port 2A is connected to Port 2B.

Features

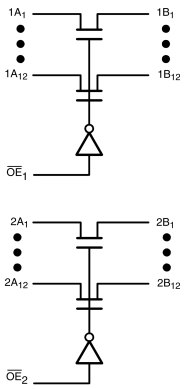
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

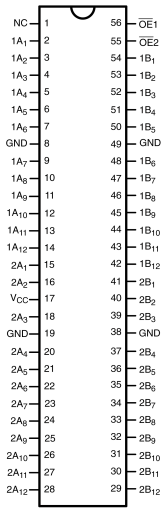
Order Number	Package Number	Package Description
FST16211MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16211MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,^\circ C$ to $+85\,^\circ C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	6.0		6.5	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	7.0		7.2	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

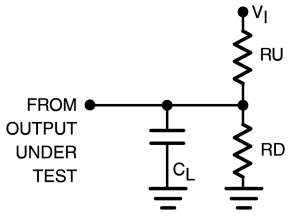
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	6		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

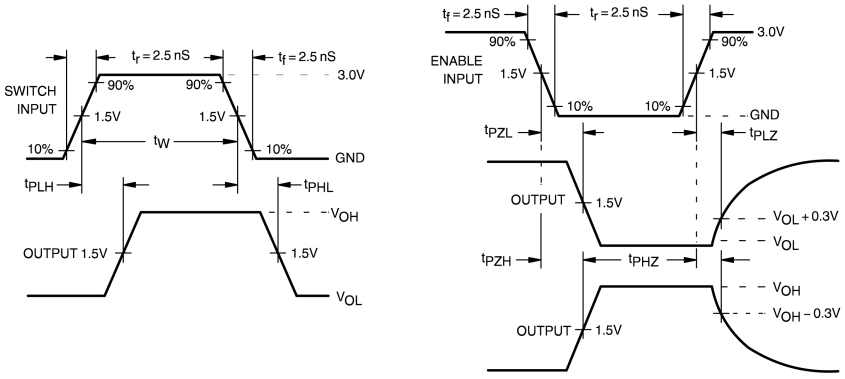
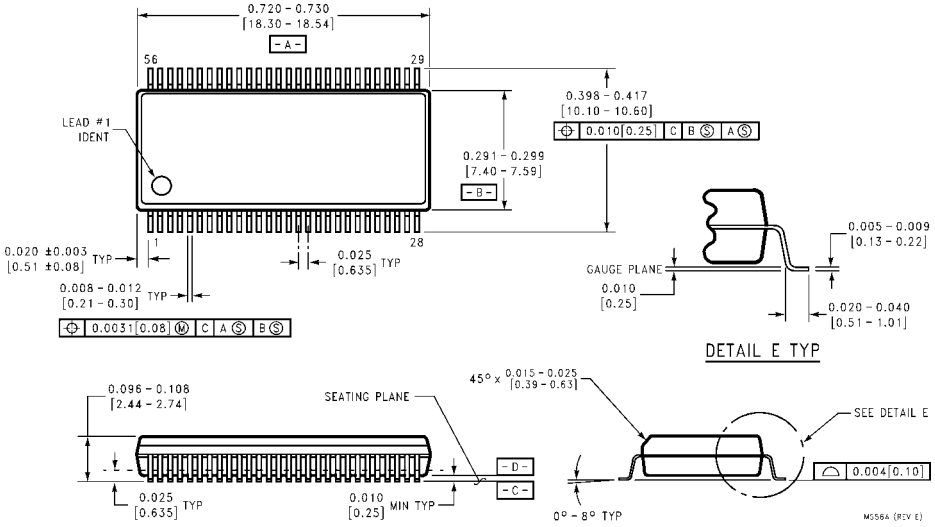


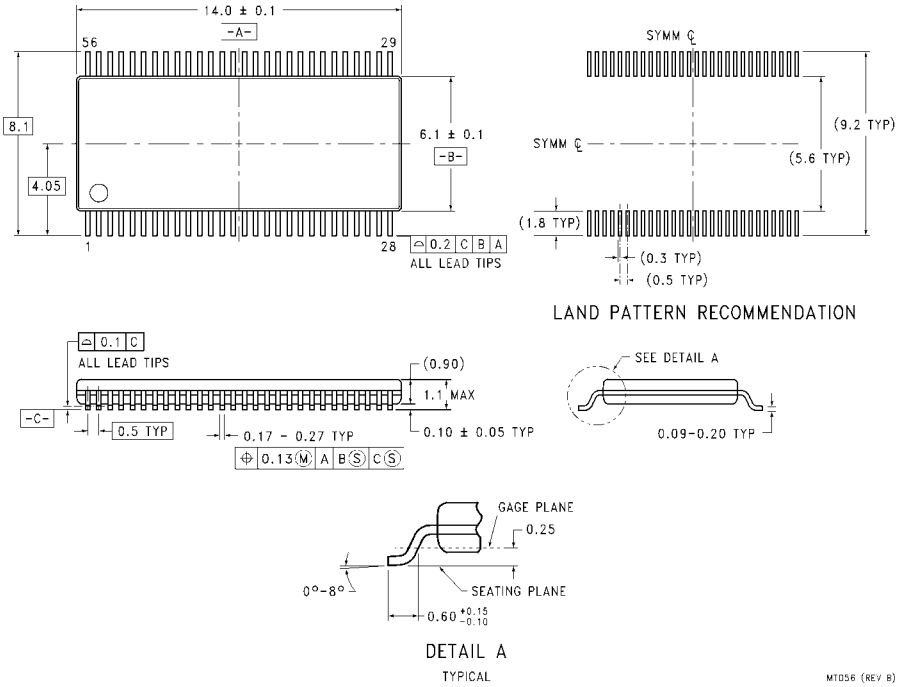
FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

July 1997
Revised December 1999

FST16212
24-Bit Bus Exchange Switch

General Description

The Fairchild Switch FST16212 provides 24-bits of high-speed CMOS TTL-compatible bus switching or exchanging. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which allows data exchange between the four signal ports via the data-select terminals.

Features

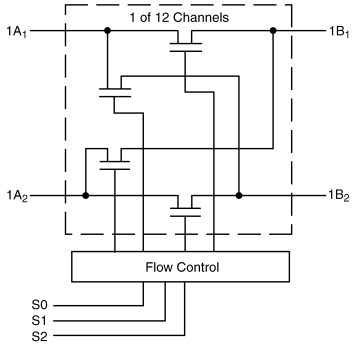
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

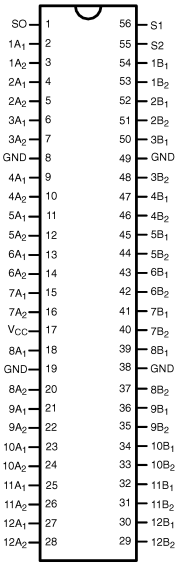
Order Number	Package Number	Package Description
FST16212MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16212MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Truth Table

S2	S1	S0	A_1	A_2	Function
L	L	L	Z	Z	Disconnect
L	L	H	B_1	Z	$A_1 = B_1$
L	H	L	B_2	Z	$A_1 = B_2$
L	H	H	Z	B_1	$A_2 = B_1$
H	L	L	Z	B_2	$A_2 = B_2$
H	L	H	Z	Z	Disconnect
H	H	L	B_1	B_2	$A_1 = B_1$, $A_2 = B_2$
H	H	H	B_2	B_1	$A_1 = B_2$, $A_2 = B_1$

Pin Descriptions

Pin Name	Description
S2, S1, S0	Data-select inputs
A_1, A_2	Bus A
B_1, B_2	Bus B

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held high or low. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		14	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A=+25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PHL},t_{PLH}	Prop Delay S to Bus	1.5	7.0		7.5	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time, S to A or B	1.5	7.5		8.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time S to A or B	1.0	8.5		9.0	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

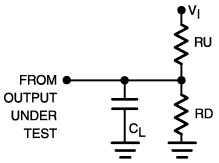
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	10		pF	V_{CC} = 5.0V, S0, S1, or S2 =GND

Note 7: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

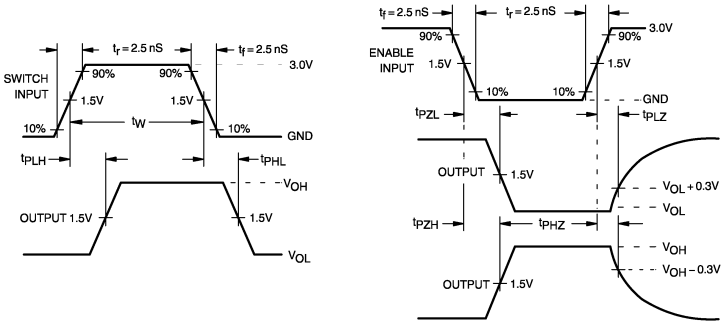
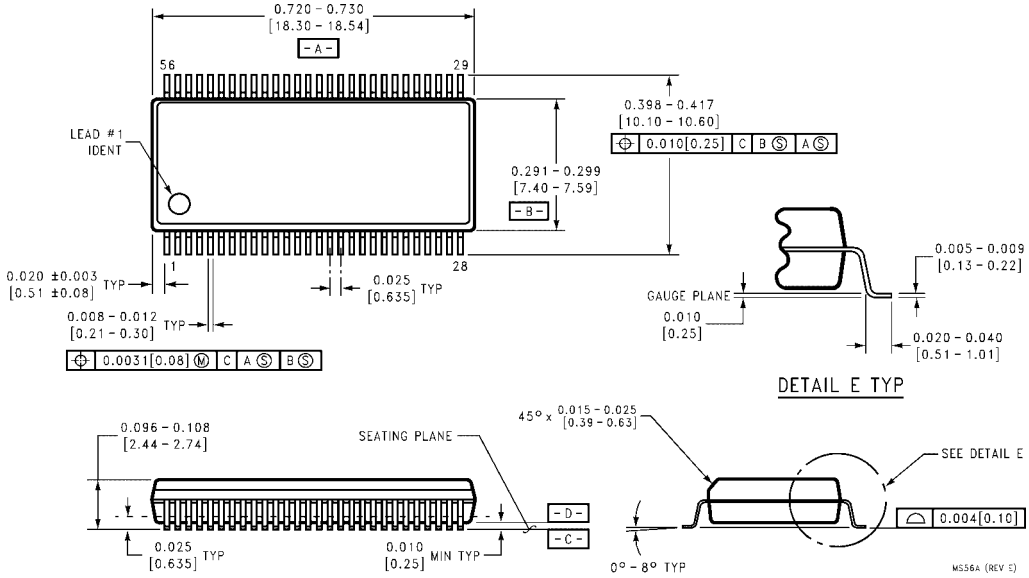


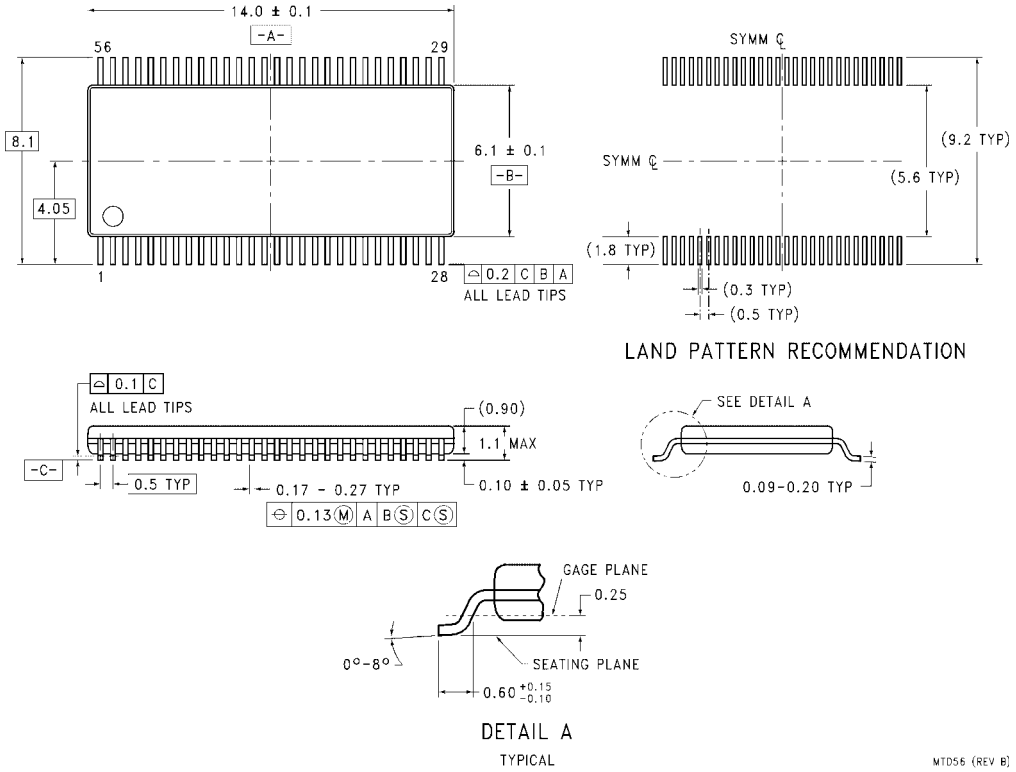
FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

July 1997
Revised December 1999

FST16213
24-Bit Bus Exchange Switch

General Description

The Fairchild Switch FST16213 provides 24-bits of high-speed CMOS TTL-compatible bus switching or exchanging. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which allows data exchange between the four signal ports via the data-select terminals.

Features

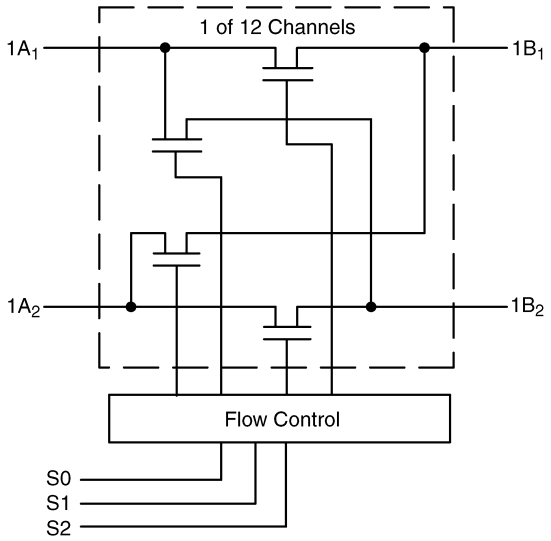
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

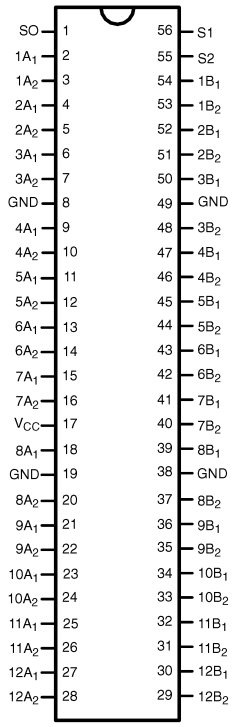
Order Number	Package Number	Package Description
FST16213MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16213MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
S2, S1, S0	Data-select inputs
A_1, A_2	Bus A
B_1, B_2	Bus B

Truth Table

S2	S1	S0	A_1	A_2	Function
L	L	L	Z	Z	Disconnect
L	L	H	B_1	Z	$A_1 = B_1$
L	H	L	B_2	Z	$A_1 = B_2$
L	H	H	Z	B_1	$A_2 = B_1$
H	L	L	Z	B_2	$A_2 = B_2$
H	L	H	A_2 and B_2	A_1 and B_2	$A_1 = A_2 = B_2$
H	H	L	B_1	B_2	$A_1 = B_1$, $A_2 = B_2$
H	H	H	B_2	B_1	$A_1 = B_2$, $A_2 = B_1$

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held high or low. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	A to B or B to A	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
	(Note 5)	4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
	Switch On Resistance	4.5		10	14	Ω	V_{IN} = 0V, I_{IN} = 64mA
	A1 to A2	4.5		10	14	Ω	V_{IN} = 0V, I_{IN} = 30mA
	(Note 5)	4.5		16	22	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		22	30	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PHL},t_{PLH}	Prop Delay A1 to A2		0.5		0.5	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time, S to A or B	1.5	7.5		8.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time S to A or B	1.0	8.5		9.0	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time, S0 to A2 and B2	1.5	9.5		10.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time, S0 to A2 and B2	1.5	9.0		10.0	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

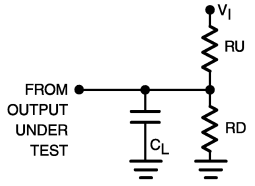
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	10		pF	V_{CC} = 5.0V S0, S1, or S2 = GND

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

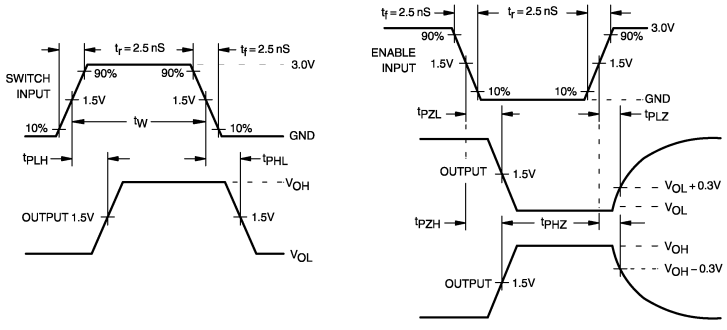
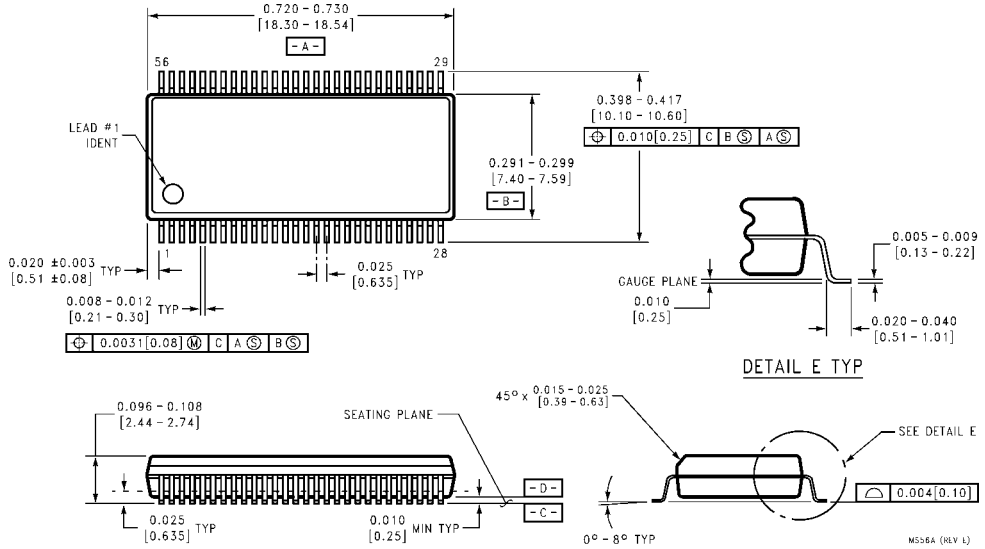


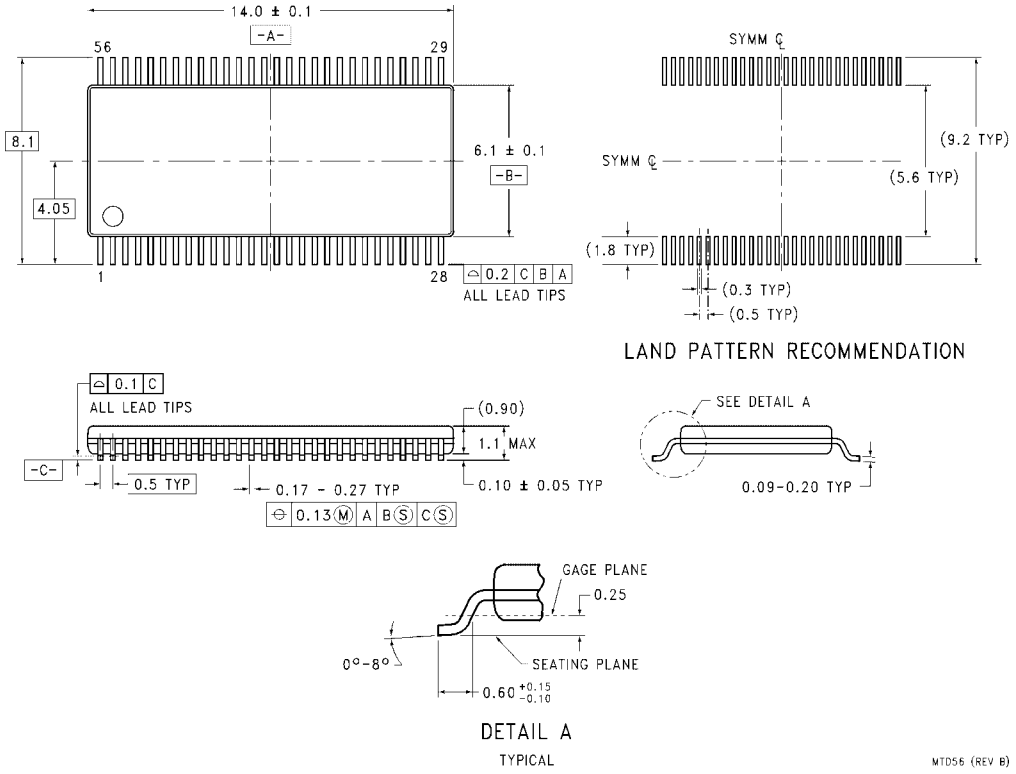
FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

July 1997
Revised December 1999

FST16232
Synchronous 16-Bit to 32-Bit Multiplexer/Demultiplexer Bus Switch

General Description

The Fairchild Switch FST16232 is a 16-bit to 32-bit high-speed CMOS TTL-compatible synchronous multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device allows two separate datapaths to be multiplexed onto, or demultiplexed from, a single path. Two control select pins (S_1, S_0) are synchronous and clocked on the rising edge of CLK when $\overline{\text{CLKEN}}$ is LOW.

Features

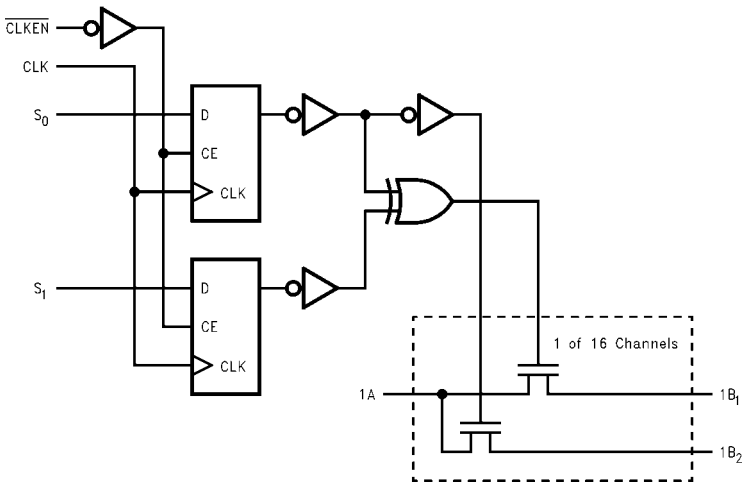
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

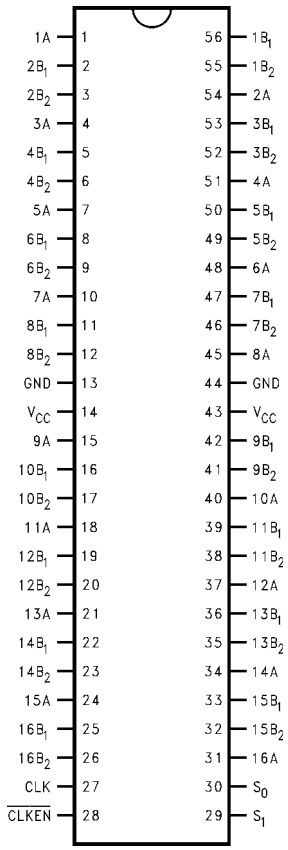
Order Number	Package Number	Package Description
FST16232MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16232MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
S_1, S_0	Control Pins
CLK	Clock Input
$\overline{\text{CLKEN}}$	Clock Enable Input
1A, 2A	Bus A
1B, 2B	Bus B

Truth Table

Inputs				Function
S_1	S_0	CLK	$\overline{\text{CLKEN}}$	
X	X	X	H	Last State
L	L	↑	L	Disconnect
L	H	↑	L	A = B_1 and A = B_2
H	L	↑	L	A = B_1
H	H	↑	L	A = B_2

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_{IN})(Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OFF}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,°C$ to $+85\,°C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
f_{MAX}	Maximum Clock Frequency	150		150		MHz	V_I = OPEN	Figure 1 Figure 2
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PHL}, t_{PLH}	Prop Delay CLK to B or A	2.0	6.3		6.0	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time CLK to A = B_1 = B_2	1.7	8.5		9.0	ns	V_I = 7V for t_{PZL}, V_I = OPEN for t_{PZH}	Figure 1 Figure 2
	Output Enable Time CLK to A or B_1 or B_2	2.0	6.5		6.5	ns	V_I = 7V for t_{PZL}, V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time CLK to A or B	1.0	8.5		9.0	ns	V_I = 7V for t_{PLZ}, V_I = OPEN for t_{PHZ}	Figure 1 Figure 2
t_S	Setup Time S_1, S_0 before CLK ↑	2.5		2.8		ns		Figure 1 Figure 2
	Setup Time $\overline{CLKEN}$ before CLK ↑	1.8		2.0				
t_H	Hold Time S_1, S_0 after CLK ↑	1.0		1.0		ns		Figure 1 Figure 2
	Hold Time $\overline{CLKEN}$ after CLK ↑	1.5		1.5				
t_W	Pulse Width	3.1		3.1		ns	Clock HIGH or LOW	Figure 1 Figure 2

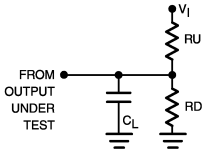
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	4		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	7		pF	V_{CC} = 5.0V, S_0, S_1 = 0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

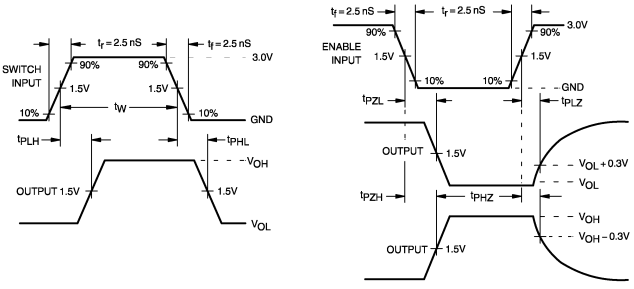
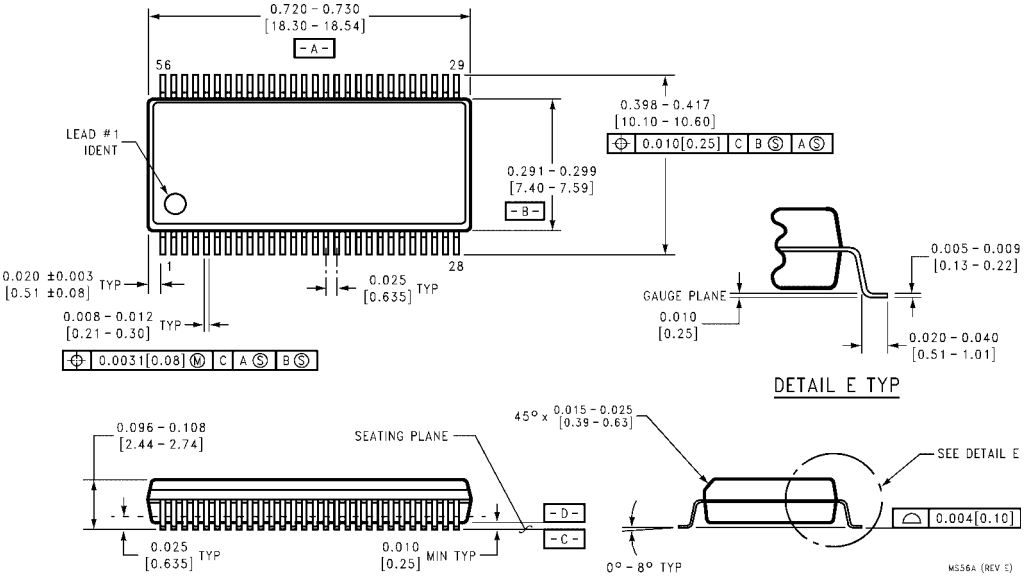


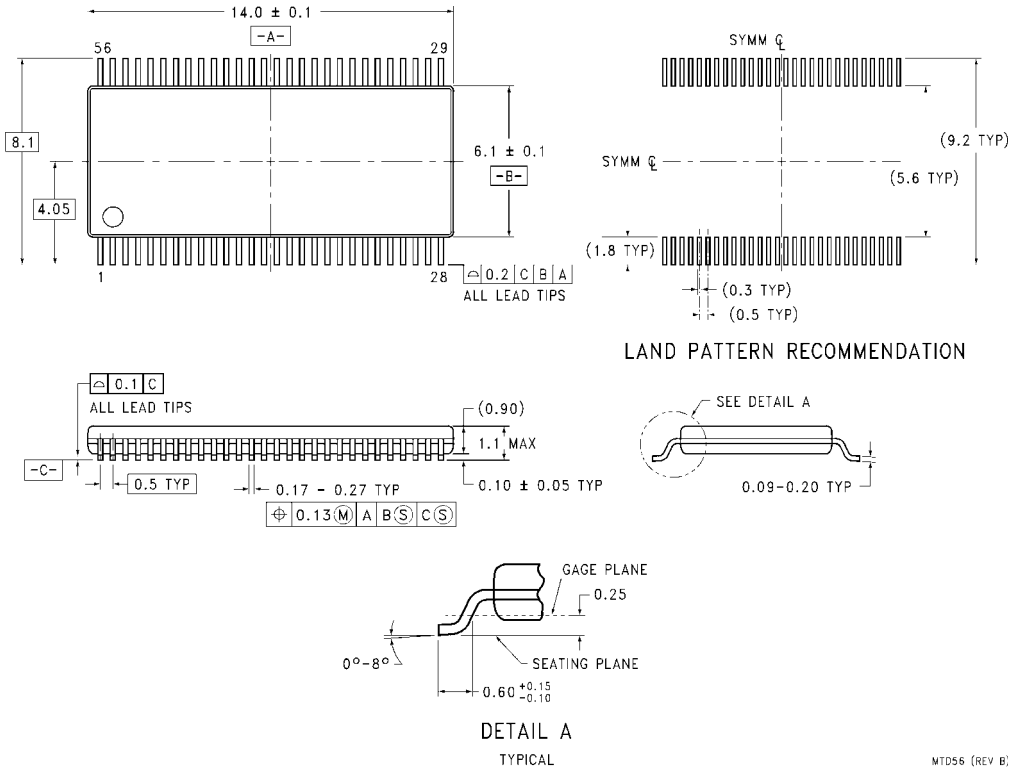
FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

September 1997
Revised December 1999

FST16233
16-Bit to 32-Bit Multiplexer/Demultiplexer Bus Switch

General Description

The Fairchild Switch FST16233 is a 16-bit to 32-bit high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device can be used in applications where two buses need to be addressed simultaneously. The FST16233 can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select (SEL_1, SEL_0) and two test ($TEST_0$, $TEST_1$) inputs provide switch enable and multiplexer select control.

The FST16233 is designed to prevent through-current when switching buses.

Features

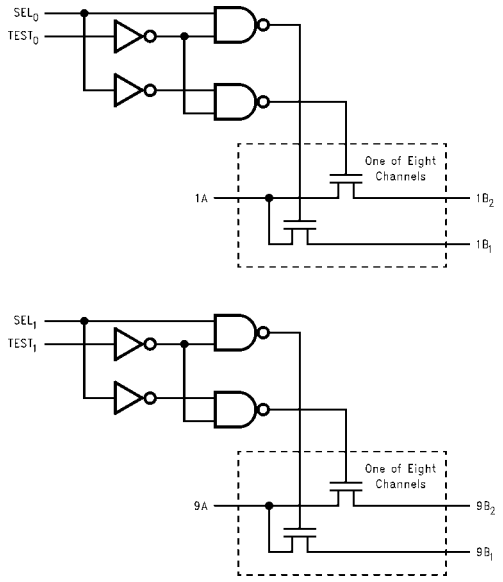
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

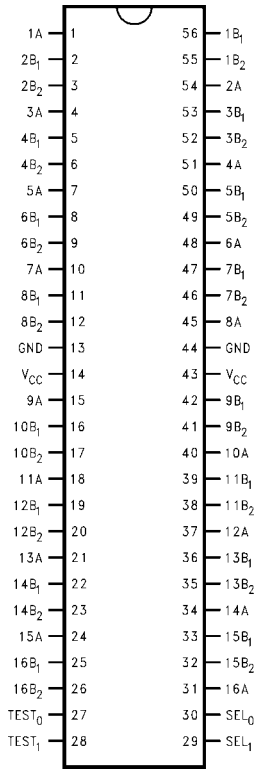
Order Number	Package Number	Package Description
FST16233MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16233MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
SEL_0, SEL_1	Select Inputs
$TEST_0$, $TEST_1$	Test Inputs
A	Bus A
B_1, B_2	Bus B

Truth Table

Inputs		Function
SEL	TEST	
L	L	$A = B_1$
H	L	$A = B_2$
X	H	$A = B_1$ and $A = B_2$

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OFF}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
Δ I_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\ °C$ to $+85\ °C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	A or B, to B or A (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PHL},t_{PLH}	SEL to A	1.5	6.1		6.8	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time, SEL or TEST to B	1.0	6.5		7.2	ns	V_I = 7V for t_{PZL}, V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time, SEL or TEST to B	1.5	7.8		8.5	ns	V_I = 7V for t_{PLZ}, V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

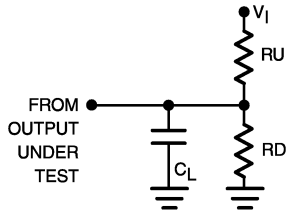
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	4		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	6		pF	V_{CC} = 5.0V, Switch OFF

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

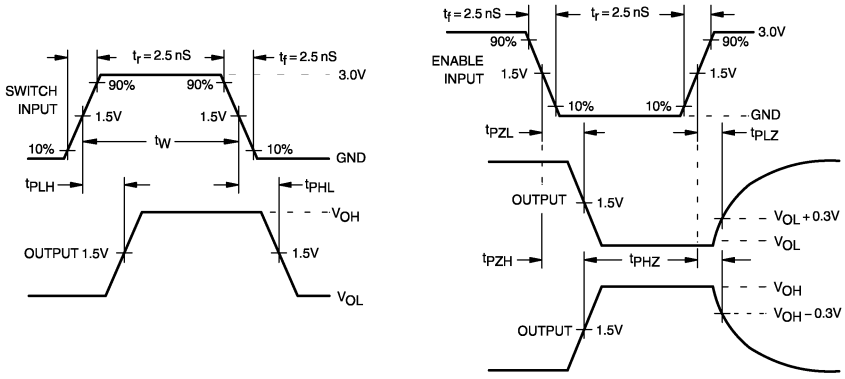
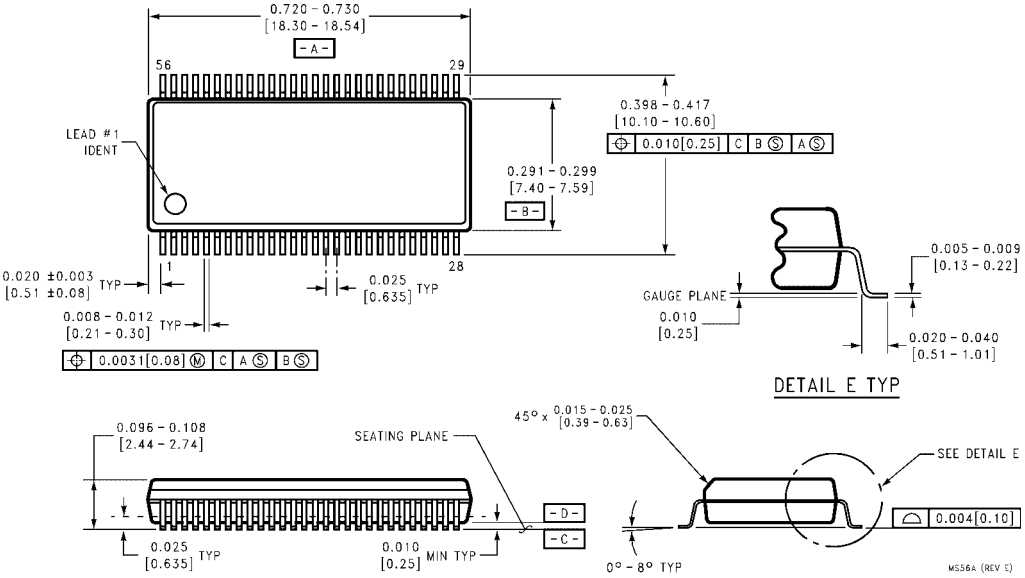


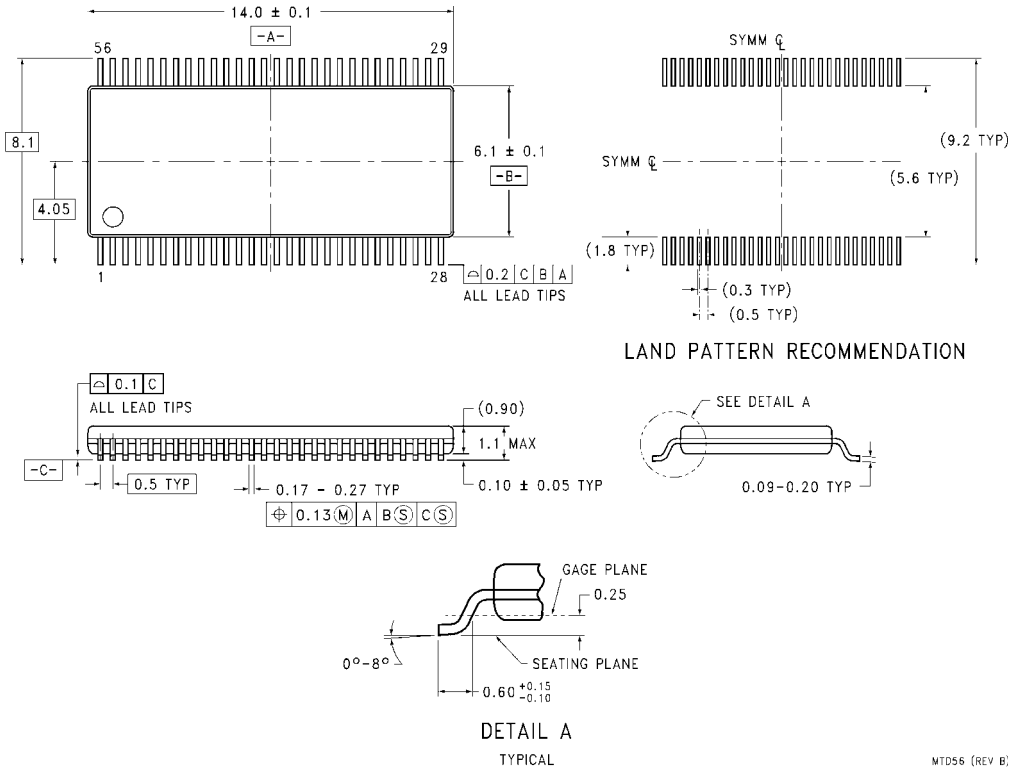
FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

September 1999
Revised December 1999

FST162861
20-Bit Bus Switch with 25Ω Series Resistors in Outputs (Preliminary)

General Description

The Fairchild Switch FST162861 provides 20-Bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 10-bit or 20-Bit bus switch. When $\overline{OE}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, Port 2A is connected to Port 2B. When $\overline{OE}_X$ is HIGH, a high impedance state exists between the A and B ports. The FST162861 has an equivalent 25Ω series resistors to reduce signal-reflection noise, eliminating the need for external terminating resistors.

Features

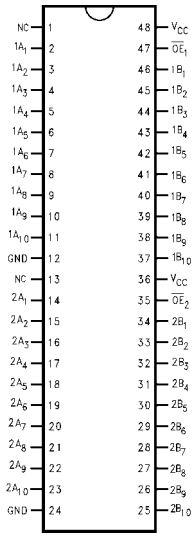
- 25Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

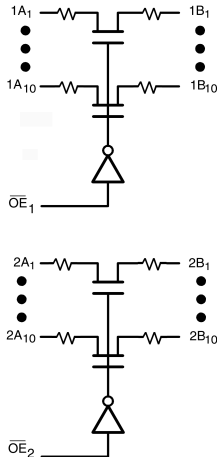
Order Number	Package Number	Package Description
FST162861MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Logic Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	–0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 3)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either the A or B Port across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held high or low. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch ON Resistance	4.5	20	26	38	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 6)	4.5	20	28	40	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5	20	35	48	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		TBD	TBD	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\ °C$ to $+85\ °C$, $C_L = 50$ pF, RU = RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 7)		1.25		1.25	ns	V_I = OPEN	Figure 1, Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	6.0		6.5	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1, Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	6.0		6.5	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1, Figure 2

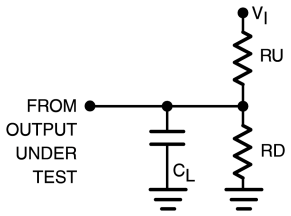
Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V, V_{IN} = 0V
$C_{I/O}$	Input/Output Capacitance “OFF State”	6		pF	V_{CC}, $\overline{OE}$ = 5.0V, V_{IN} = 0V
	Input/Output Capacitance “ON State”	12		pF	V_{CC} = 5.0V, $\overline{OE}$ = 0.0V, V_{IN} = 0V

Note 8: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

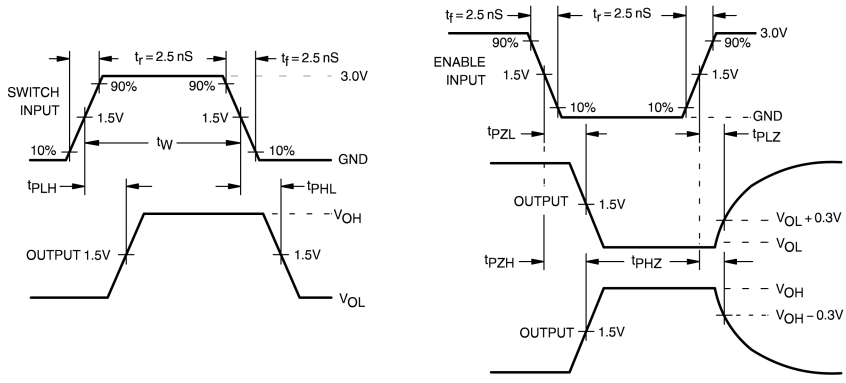
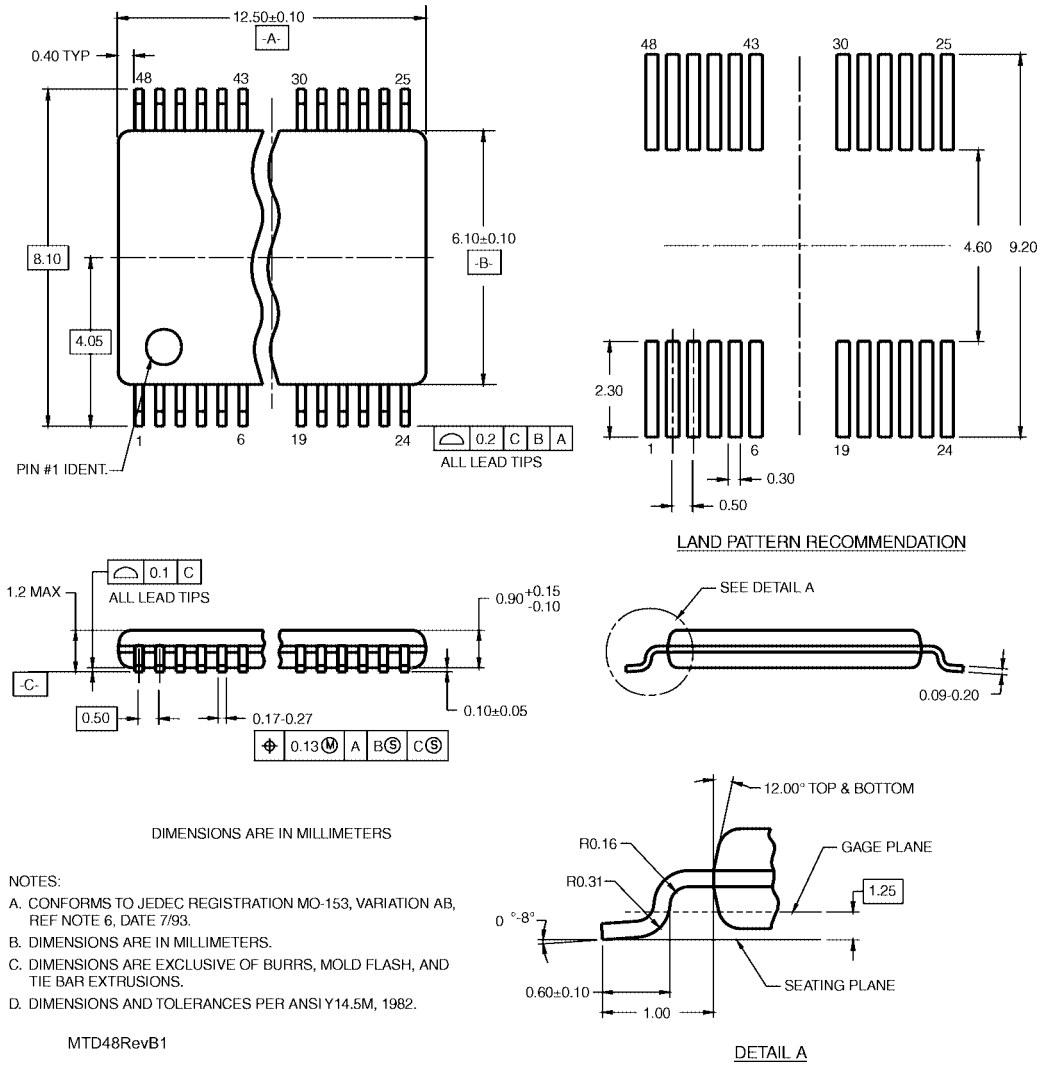


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384(FST3384) bus switch product.

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

July 1997
Revised December 1999

FST16292
12-Bit to 24-Bit Multiplexer/Demultiplexer Bus Switch

General Description

The Fairchild Switch FST16292 provides twelve 2:1 high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The select pin connects the A Port to the selected B Port output. The A_2 Ports are not externally connected, thus have a 500Ω pull-down resistor to ground.

Features

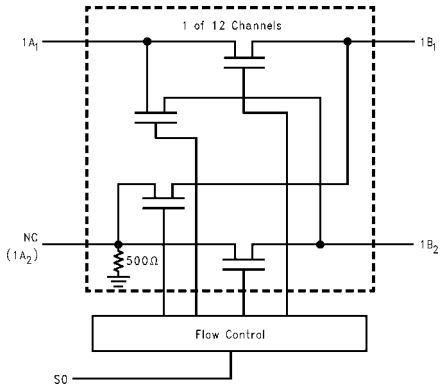
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.
- Internal 500Ω pull-down resistor on A_2 port.

Ordering Code:

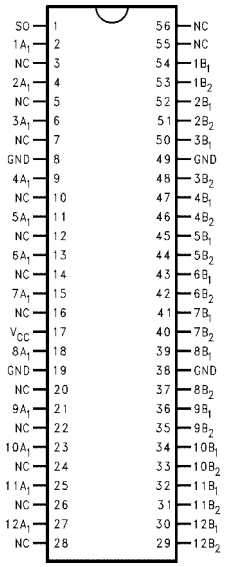
Order Number	Package Number	Package Description
FST16292MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16292MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
SO	Data-select input
A_1	Bus A
B_1, B_2	Bus B

Truth Table

S0	A_1	A_2	Function
L	B_1	B_2	$A_1 = B_1$, $A_2 = B_2$
H	B_2	B_1	$A_1 = B_2$, $A_2 = B_1$

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0ns/V to 5ns/V
Switch I/O	0ns/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 3)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance (Note 4)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		14	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 3: Typical values are at V_{CC} = 5.0V and T_A =+25°C

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\ °C$ to $+85\ °C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 5)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PHL},t_{PLH}	Prop Delay S0 to A_1	1.5	7.0		7.4	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZL}, t_{PZH}	Output Enable Time S0 to B_1 or B_2	1.0	6.7		7.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PLZ}, t_{PHZ}	Output Disable Time S0 to B_1 or B_2	1.0	7.5		7.8	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

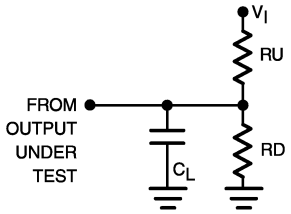
Note 5: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 6)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	10		pF	V_{CC} = 5.0V, S0 =GND

Note 6: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

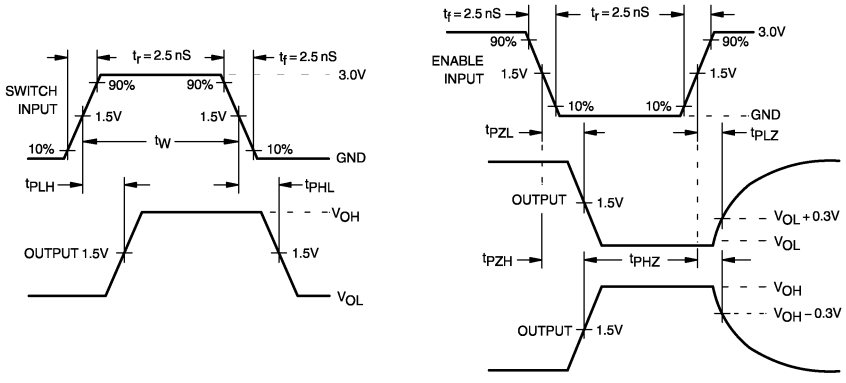
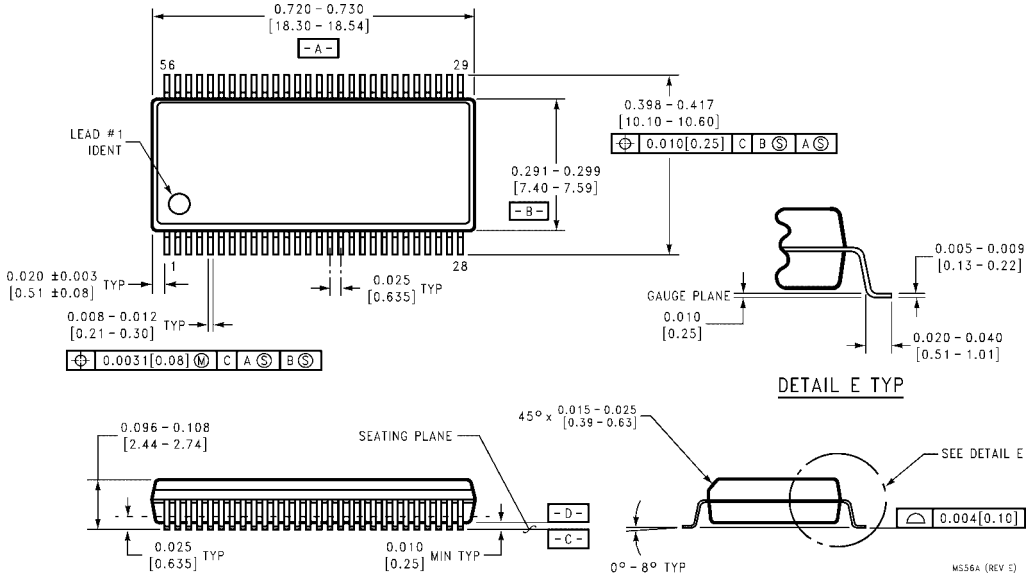


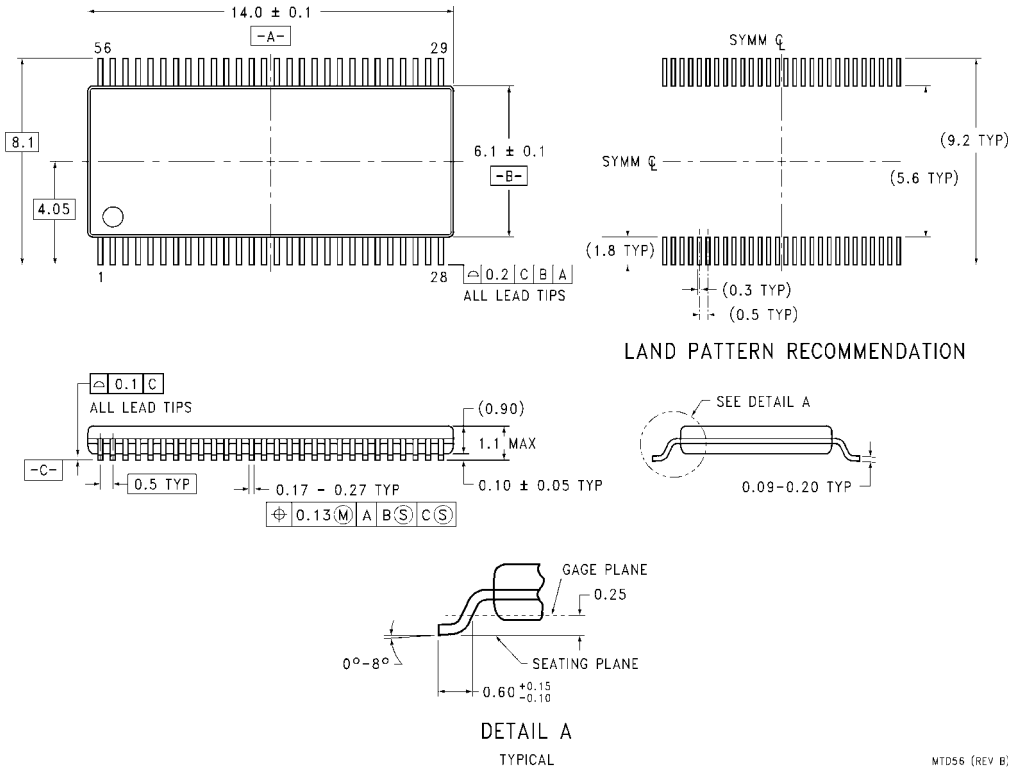
FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

September 1999
Revised December 1999

FST16861
20-Bit Bus Switch (Preliminary)

General Description

The Fairchild Switch FST16861 provides 20-Bits of high-speed CMOS TTL-compatible bus switching. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 10-bit or 20-Bit bus switch. When $\overline{OE}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, Port 2A is connected to Port 2B. When $\overline{OE}_X$ is HIGH, a high impedance state exists between the A and B Ports.

Features

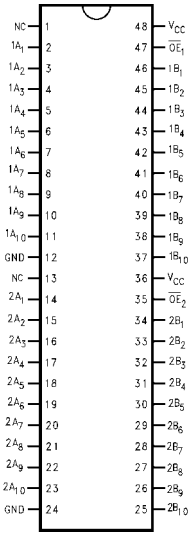
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

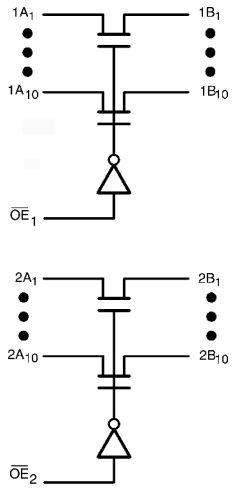
Order Number	Package Number	Package Description
FST16861MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Logic Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 3)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT}) Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held high or low. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 6)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\ °C$ to $+85\ °C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus-to-Bus (Note 7)		0.25		0.25	ns	V_I = OPEN	Figure 1, Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	6.0		6.5	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1, Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	6.0		6.5	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1, Figure 2

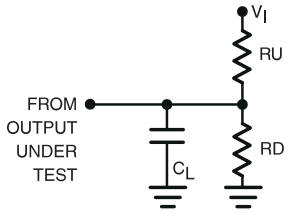
Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V, V_{IN} = 0V
$C_{I/O}$	Input/Output Capacitance “OFF State”	6		pF	V_{CC}, $\overline{OE}$ = 5.0V, V_{IN} = 0V
	Input/Output Capacitance “ON State”	12		pF	V_{CC} = 5.0V, $\overline{OE}$ = 0.0V, V_{IN} = 0V

Note 8: T_A = +25°C, f = 1 Mhz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, T_W = 500 ns

FIGURE 1. AC Test Circuit

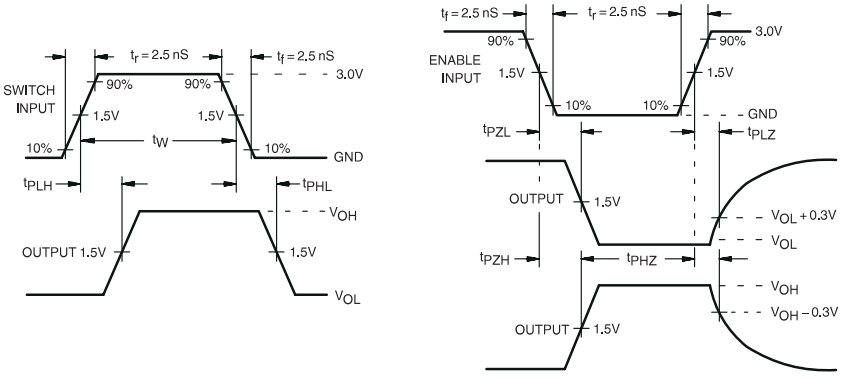
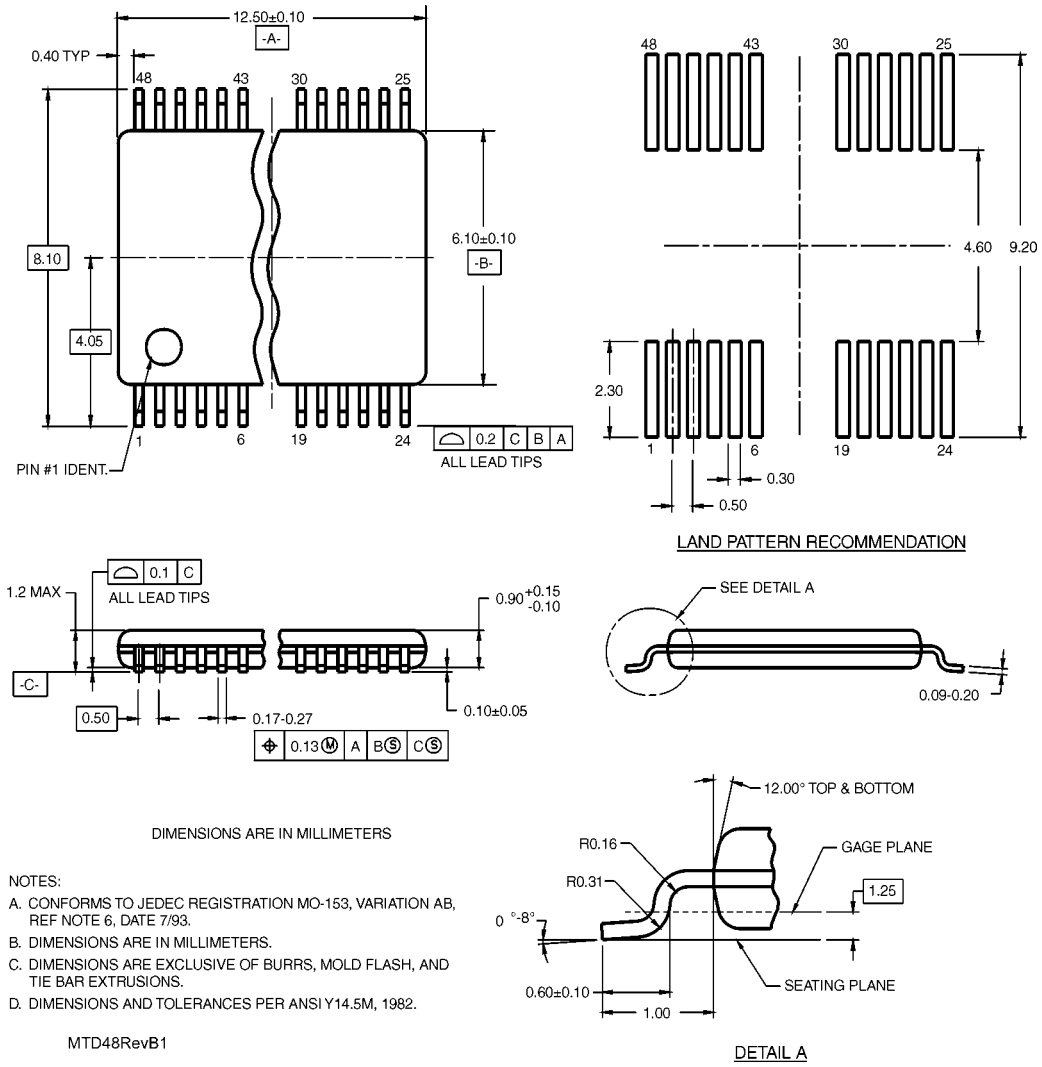


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

NOTES:

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B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384(FST3384) bus switch product.

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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August 1997
Revised December 1999

FST3125
Quad Bus Switch

General Description

The Fairchild Switch FST3125 provides four high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as four 1-bit switches with separate $\overline{OE}$ inputs. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

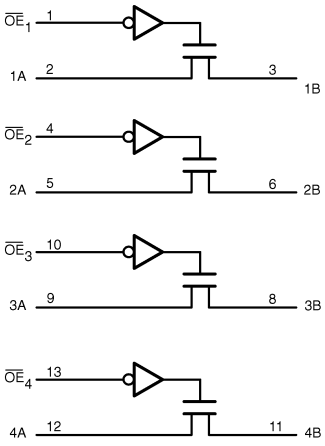
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

Order Number	Package Number	Package Description
FST3125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
FST3125QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

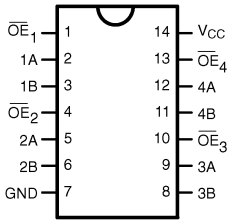
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram

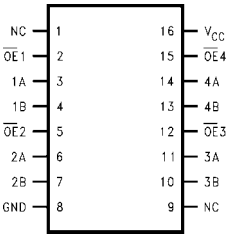


Connection Diagrams

Pin Assignment for SOIC and TSSOP



Pin Assignment for QSOP



Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$, $\overline{OE}_4$	Bus Switch Enables
1A, 2A, 3A, 4A	Bus A
1B, 2B, 3B, 4B	Bus B
NC	Not Connected

Truth Table

Inputs	Inputs/Outputs
$\overline{OE}$	A,B
L	A = B
H	Z

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN})(Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0ns/V to 5ns/V
Switch I/O	0ns/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held high or low. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	High Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	Low Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance (Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V. Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\ °C$ to $+85\ °C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.0	5.0		5.5	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	5.3		5.6	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

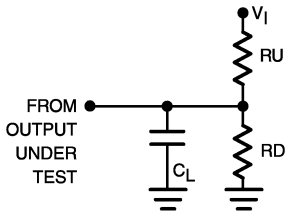
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	5		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500ns

FIGURE 1. AC Test Circuit

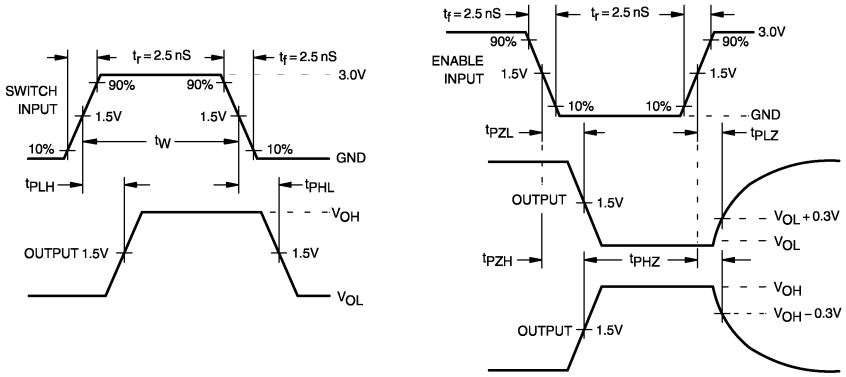
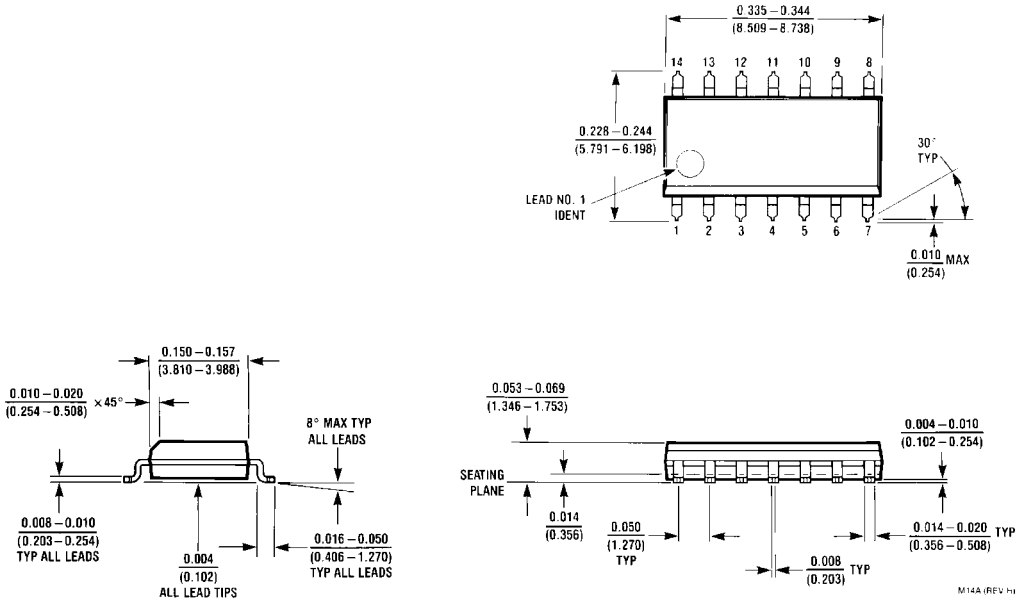
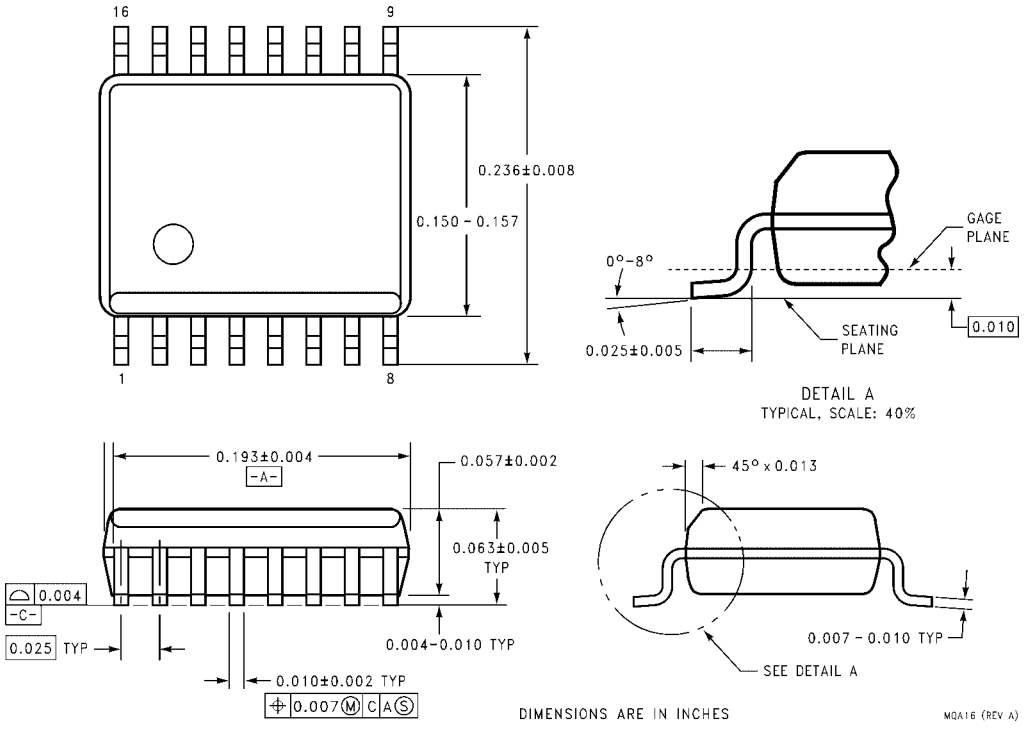


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

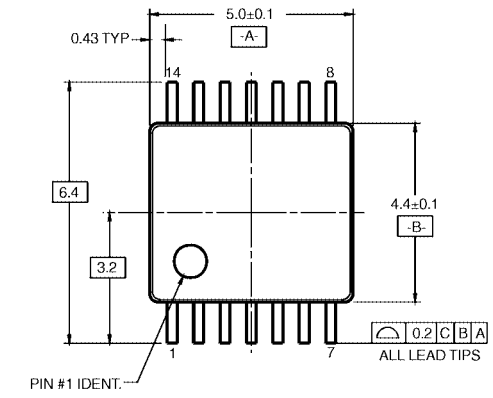


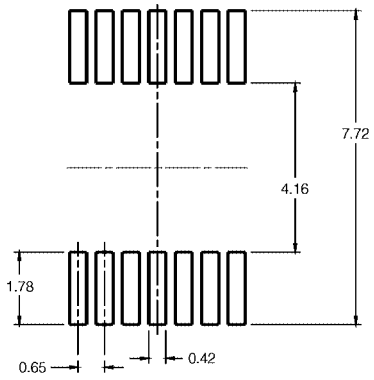
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A



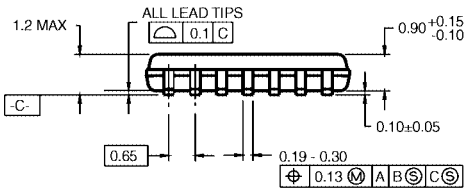
16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA16

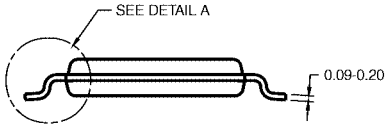
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

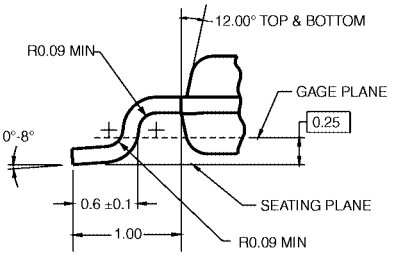




LAND PATTERN RECOMMENDATION







DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

August 1997
Revised December 1999

FST3126
Quad Bus Switch

General Description

The Fairchild Switch FST3126 provides four high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as four 1-bit switches with separate OE inputs. When OE is HIGH, the switch is ON and Port A is connected to Port B. When OE is LOW, the switch is OPEN and a high-impedance state exists between the two ports.

Features

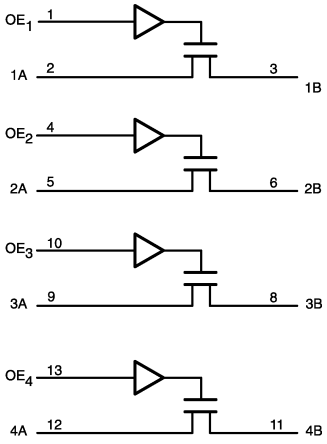
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

Order Number	Package Number	Package Description
FST3126M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
FST3126QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3126MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

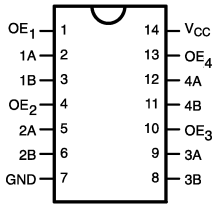
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram

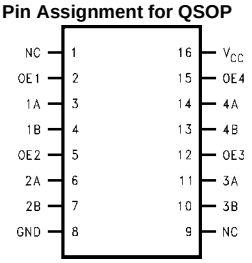


Connection Diagrams

Pin Assignment for SOIC and TSSOP



Pin Assignment for QSOP



Pin Descriptions

Pin Name	Description
OE_1, OE_2, OE_3, OE_4	Bus Switch Enables
1A, 2A, 3A, 4A	Bus A
1B, 2B, 3B, 4B	Bus B
NC	Not Connected

Truth Table

Inputs	Inputs/Outputs
OE	A,B
L	Z
H	A = B

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held high or low. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V. Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I=OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.0	4.5		5.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	5.7		6.2	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

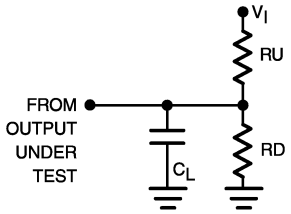
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	5		pF	V_{CC} = 5.0V, OE = 0V

Note 7: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0MHz, t_W = 500ns

FIGURE 1. AC Test Circuit

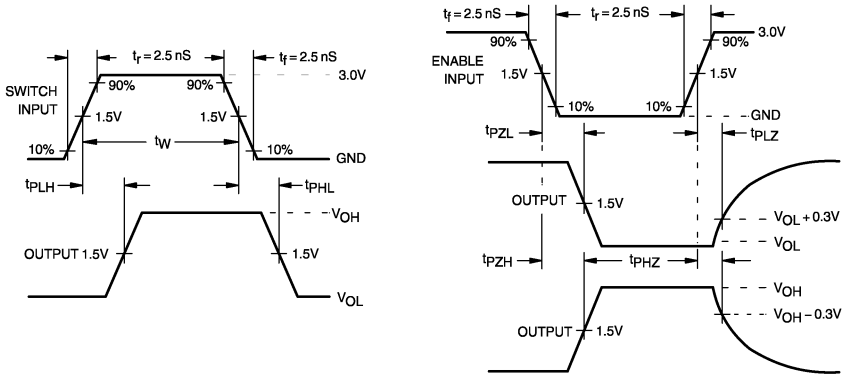
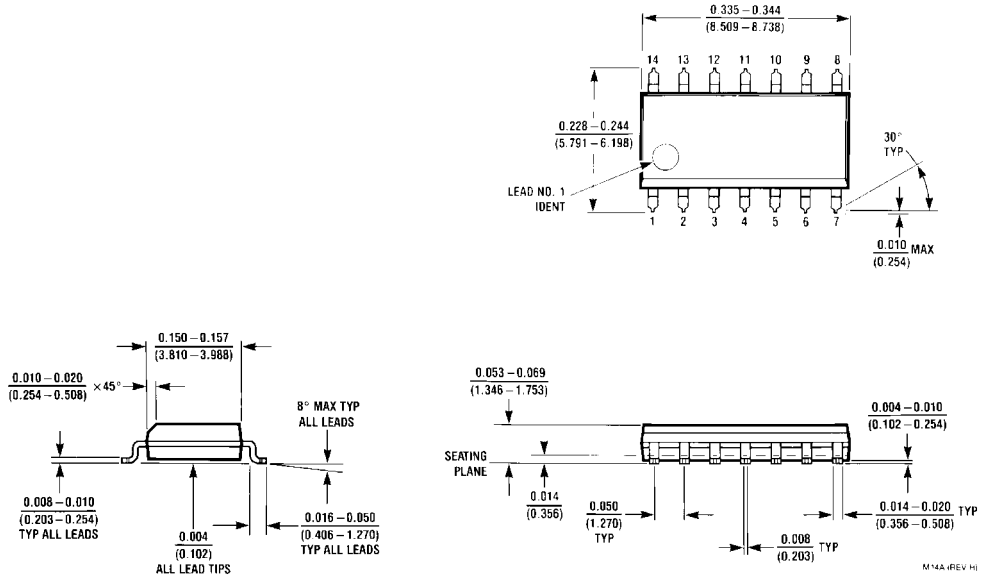
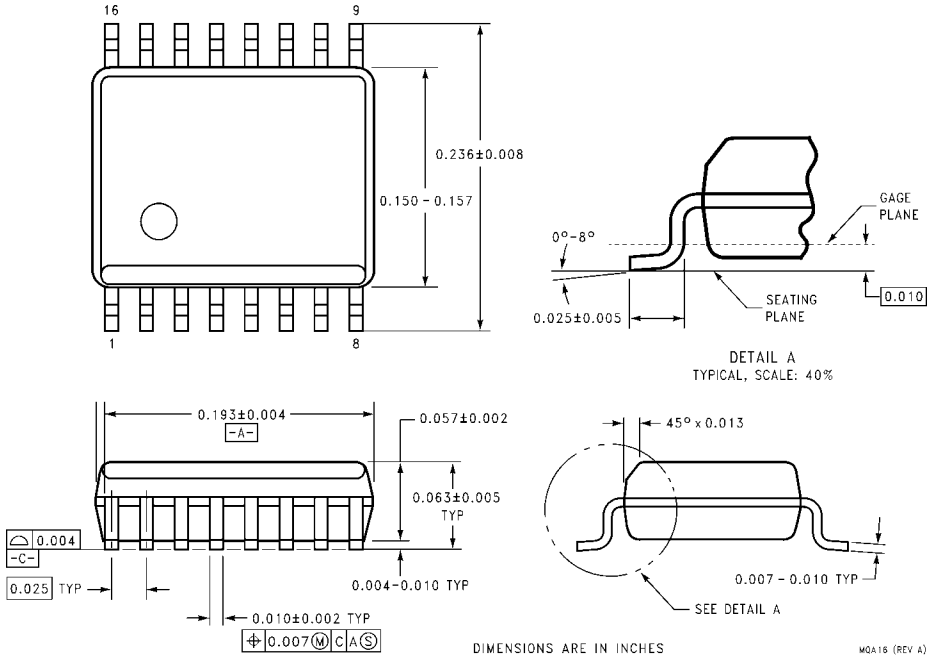


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

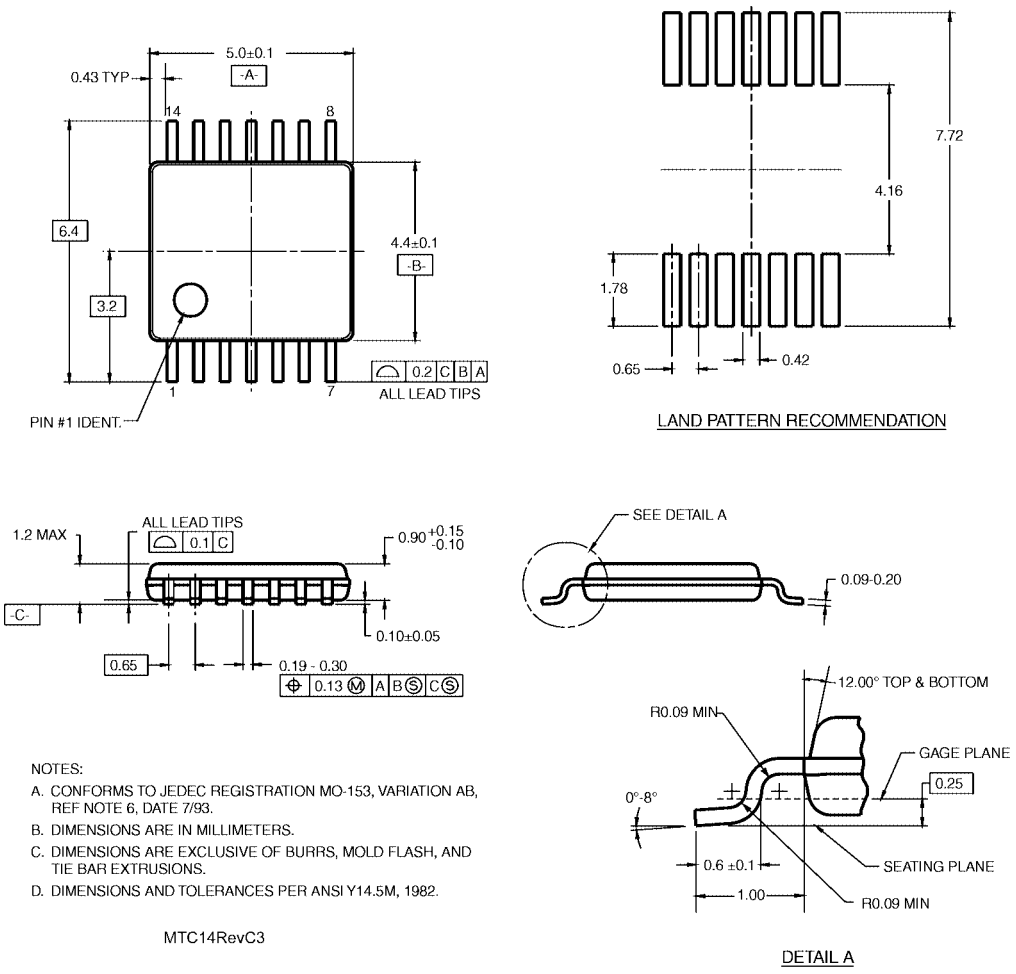


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A



16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

June 1997
Revised December 1999

FST3244
Octal Bus Switch

General Description

The Fairchild Switch FST3244 provides 8-bits of high-speed CMOS TTL-compatible bus switching in a standard '244 pin-out. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as two 4-bit switches with separate $\overline{OE}$ inputs. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

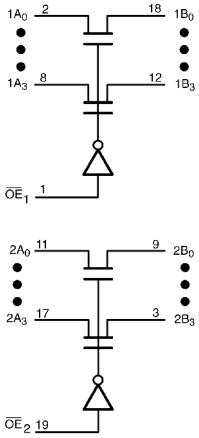
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

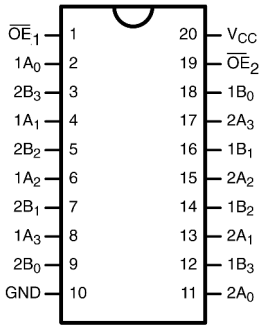
Order Number	Package Number	Package Description
FST3244WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
FST3244QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enable
1A, 2A	Bus A
1B, 2B	Bus B

Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	High Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	Low Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance (Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus(Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.0	5.6		6.1	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.0	6.2		5.6	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

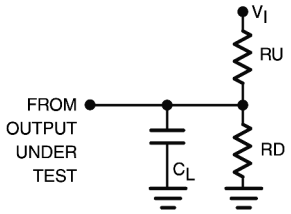
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	5		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 nS

FIGURE 1. AC Test Circuit

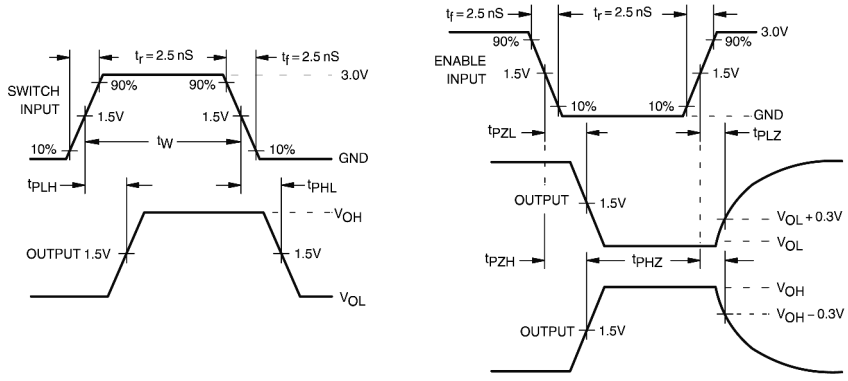
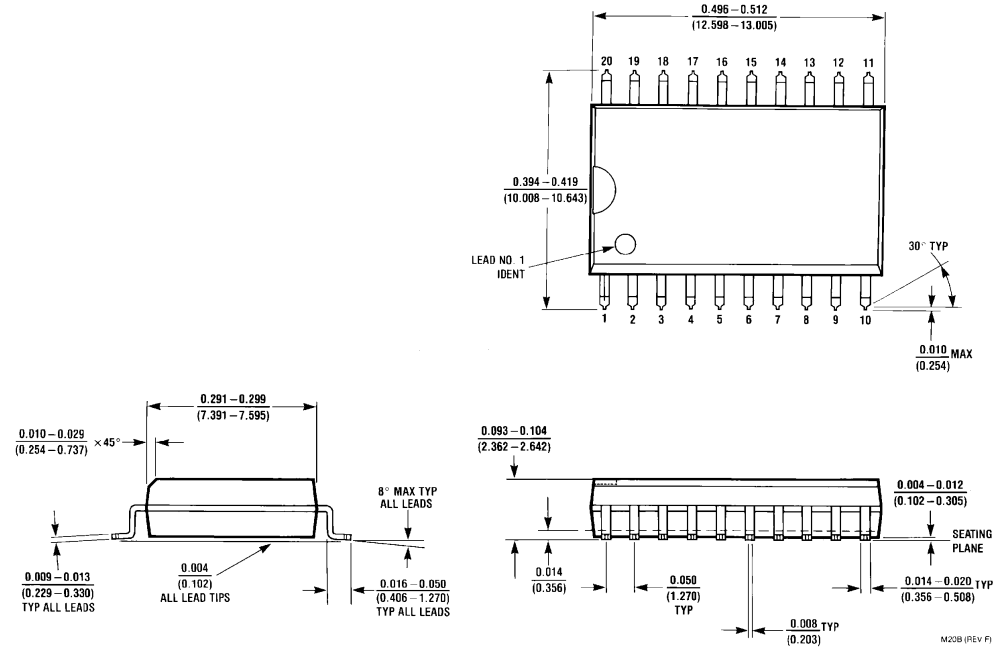
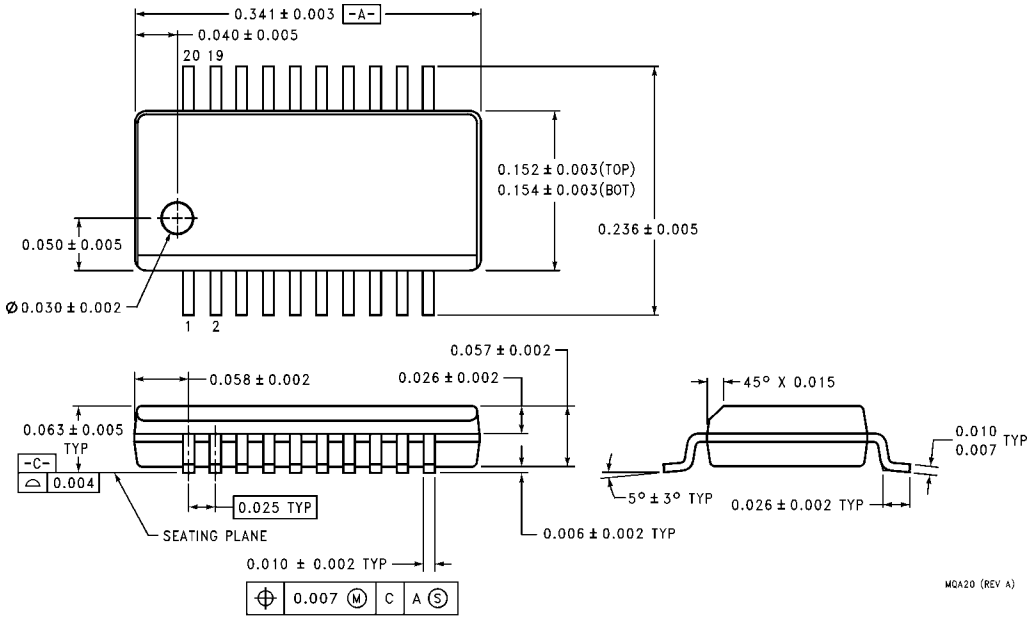


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

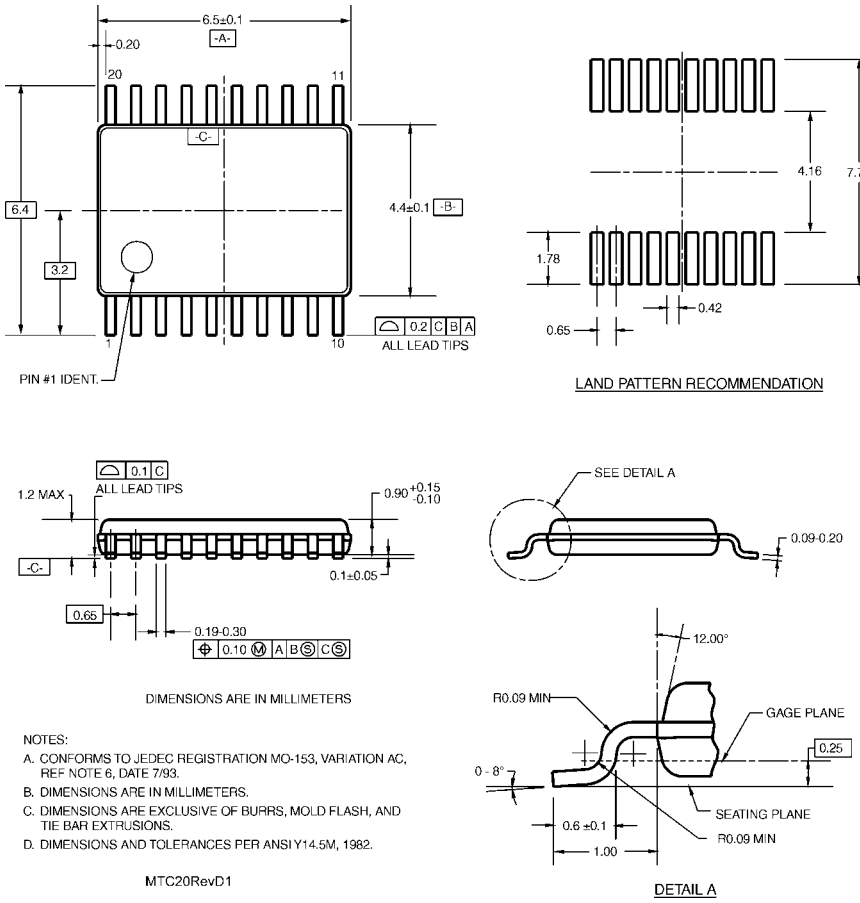


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B



20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

June 1997
Revised December 1999

FST3245
Octal Bus Switch

General Description

The Fairchild Switch FST3245 provides 8-bits of high-speed CMOS TTL-compatible bus switching in a standard '245 pin-out. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as an 8-bit switch. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

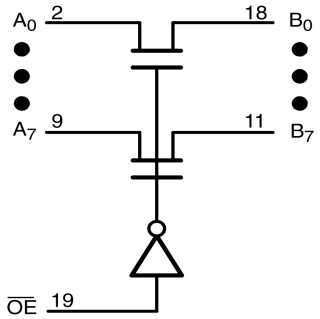
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

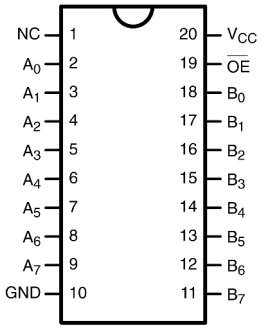
Order Number	Package Number	Package Description
FST3245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
FST3245QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
A	Bus A
B	Bus B

Truth Table

Input $\overline{OE}$	Function
L	Connect
H	Disconnect

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18 mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤ 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤ V_{CC}
R_{ON}	Switch On Resistance (Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64 mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30 mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,^\circ C$ to $+85\,^\circ C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	5.9		6.4	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	6.0		5.7	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

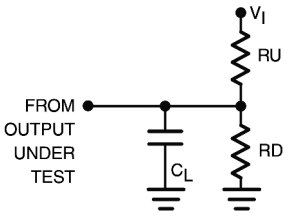
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	5		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz t_W = 500 ns

FIGURE 1. AC Test Circuit

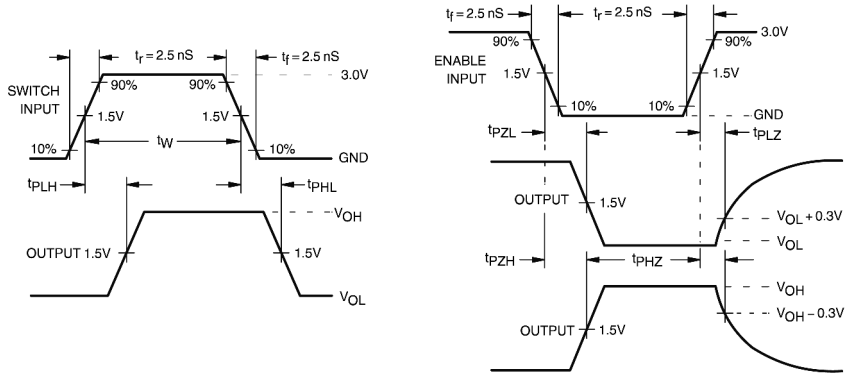
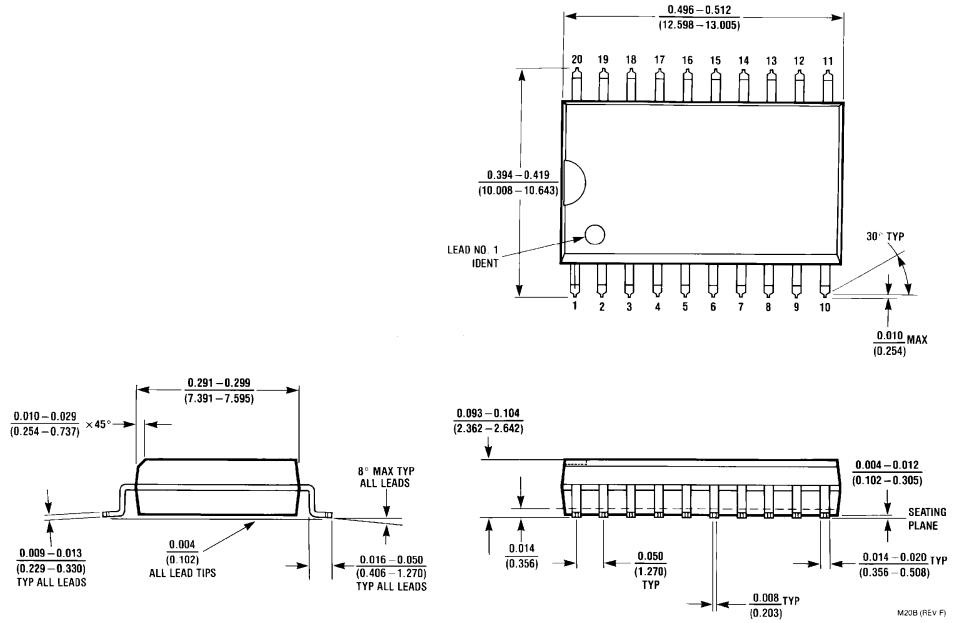
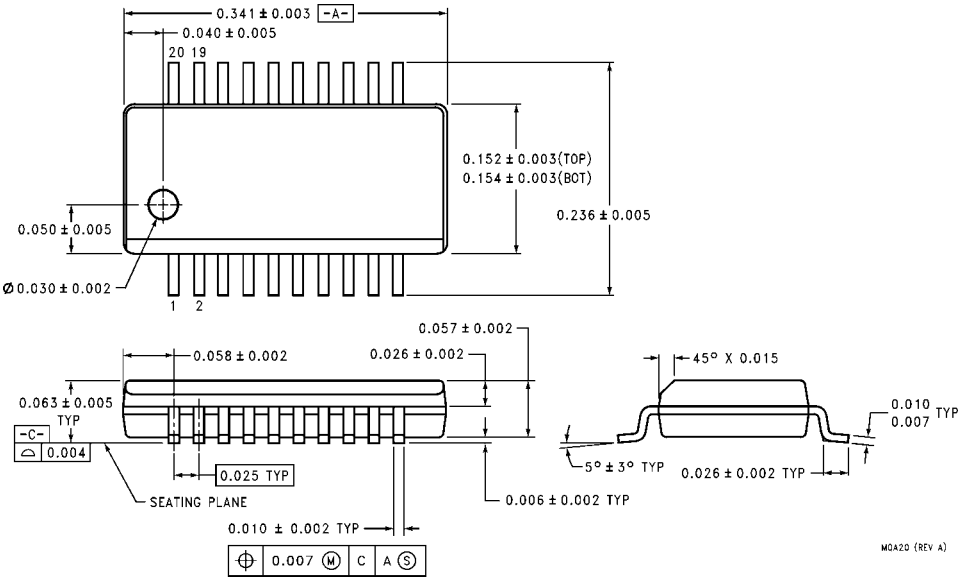


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

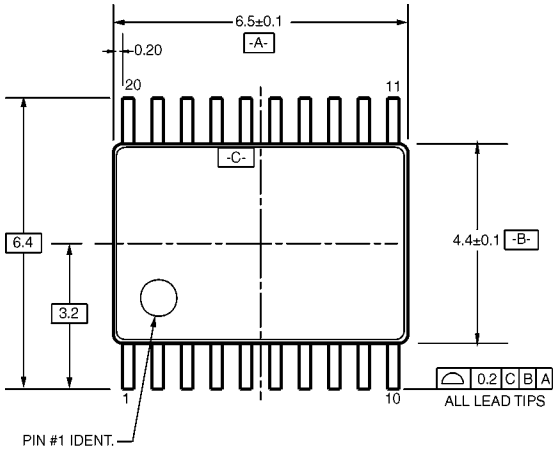


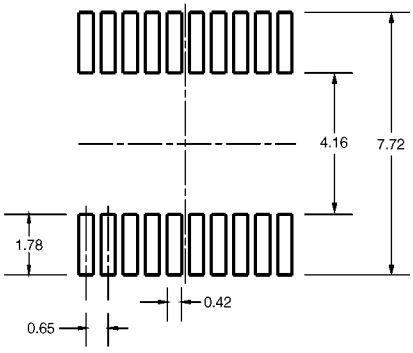
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B



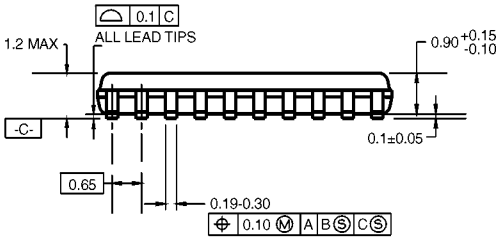
20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA20

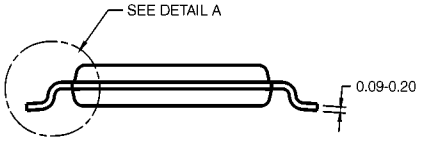
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS

NOTES:

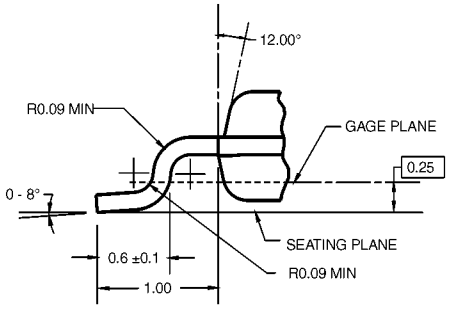
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1



DETAIL A

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

September 1997
Revised December 1999

FST3253
Dual 4:1 Multiplexer/Demultiplexer Bus Switch

General Description

The Fairchild Switch FST3253 is a dual 4:1 high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When $\overline{OE}$ is LOW, S_0 and S_1 connect the A Port to the selected B Port output. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

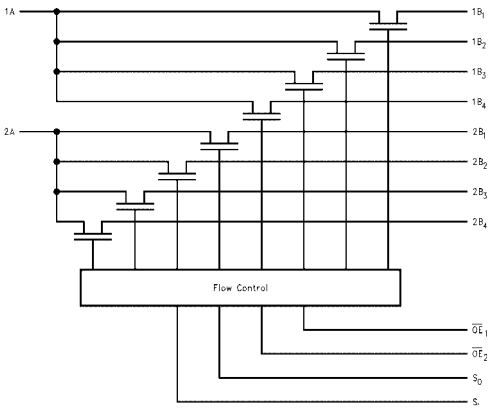
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

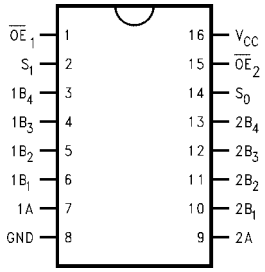
Order Number	Package Number	Package Description
FST3253M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
FST3253QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3253MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
S_0, S_1	Select Inputs
A	Bus A
B_1, B_2, B_3, B_4	Bus B

Truth Table

S_1	S_0	$\overline{OE}_1$	$\overline{OE}_2$	Function
X	X	H	X	Disconnect 1A
X	X	X	H	Disconnect 2A
L	L	L	L	$A = B_1$
L	H	L	L	$A = B_2$
H	L	L	L	$A = B_3$
H	H	L	L	$A = B_4$

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN})(Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating ($V_{CC)}$)	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0ns/V to 5ns/V
Switch I/O	0ns/V to DC
Free Air Operating Temperature (T_A)	–40 °C to –85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	High Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	Low Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
	Prop Delay, Select to Bus A	1.0	5.3		6.3			
t_{PZH}, t_{PZL}	Output Enable Time, Select to Bus B	1.0	5.3		6.0	ns	V_I = 7V for t_{PZL}	Figure 1 Figure 2
	Output Enable Time, I_{OE} to Bus A, B	1.0	5.3		6.2		V_I = OPEN for t_{PZH}	
t_{PHZ}, t_{PLZ}	Output Disable Time., Select to Bus B	1.0	5.8		6.2	ns	V_I = 7V for t_{PLZ}	Figure 1 Figure 2
	Output Disable Time, I_{OE} to Bus A, B	1.0	5.5		6.2		V_I = OPEN for t_{PHZ}	

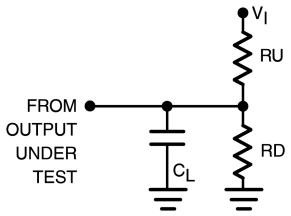
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol		Parameter	Typ	Max	Units	Conditions
C_{IN}		Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	A Port	Input/Output Capacitance	13		pF	V_{CC}, $\overline{OE}$ = 5.0V
	B Port		5		pF	

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

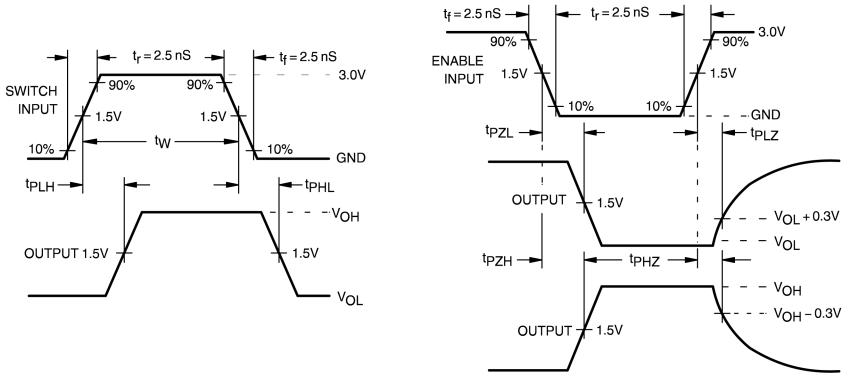
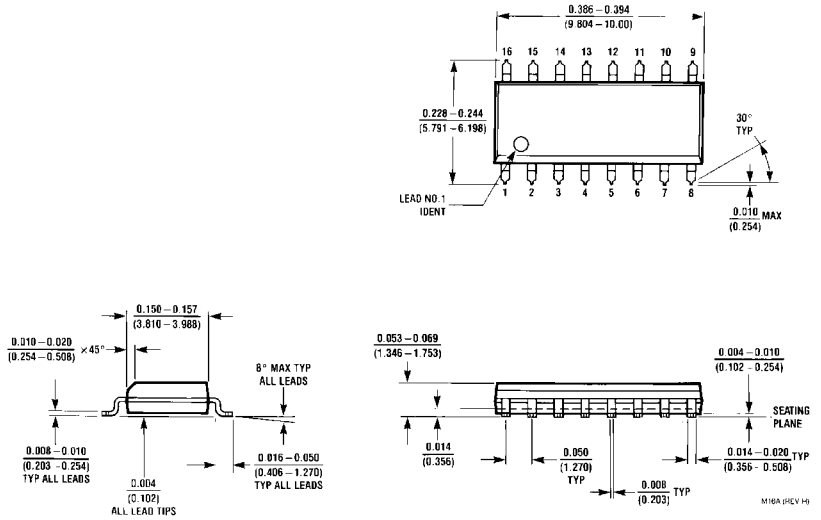
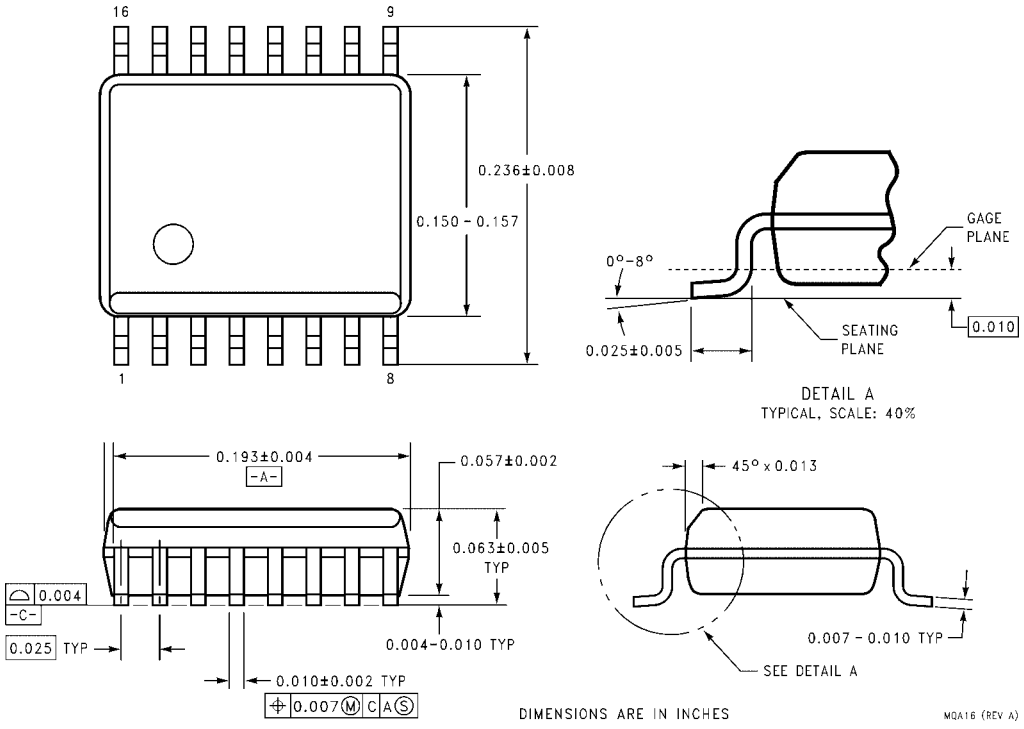


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

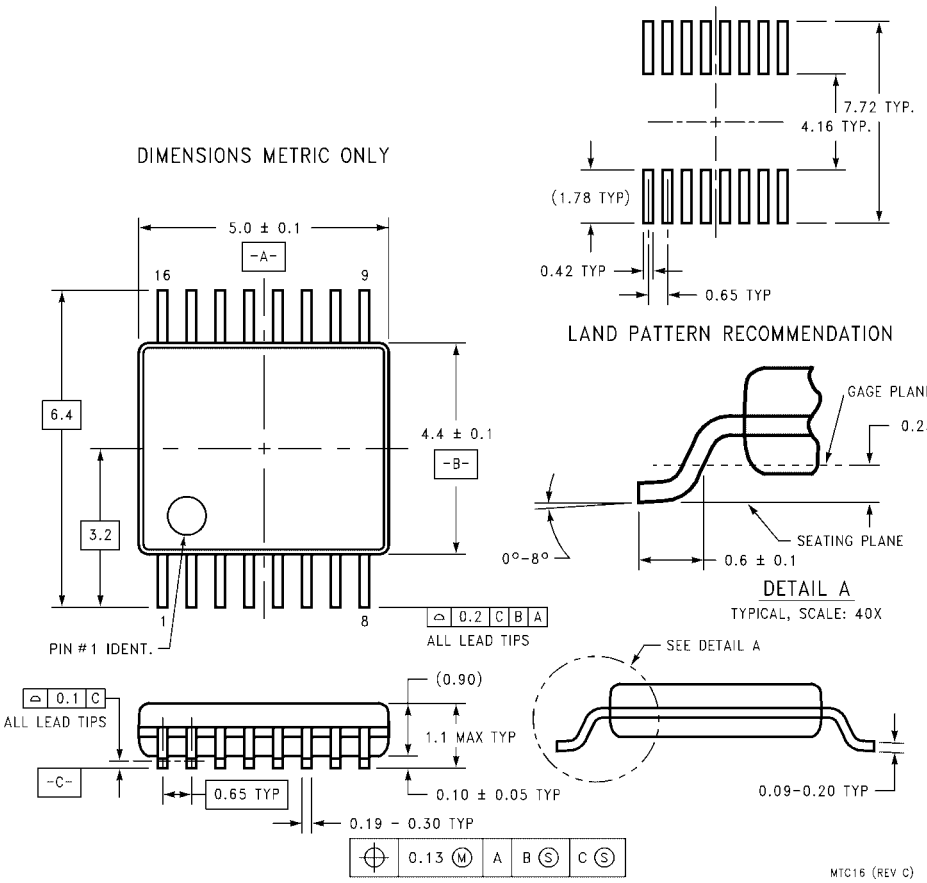


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

September 1997
Revised December 1999

FST3257
Quad 2:1 Multiplexer/Demultiplexer Bus Switch

General Description

The Fairchild Switch FST3257 is a quad 2:1 high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When $\overline{OE}$ is LOW, the select pin connects the A Port to the selected B Port output. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

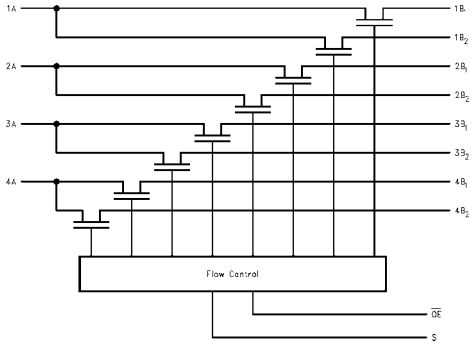
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

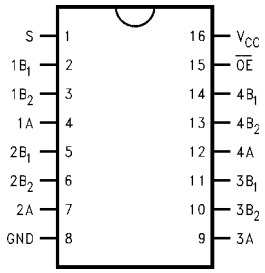
Order Number	Package Number	Package Description
FST3257M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
FST3257QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3257MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
S	Select Input
A	Bus A
B_1–B_2	Bus B

Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	$A = B_1$
H	L	$A = B_2$

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN})(Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, RU = RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
	Prop Delay, Select to Bus A	1.0	4.7		5.2			
t_{PZH}, t_{PZL}	Output Enable Time, Select to Bus B	1.0	5.2		5.7	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
	Output Enable Time, $\overline{OE}$ to Bus A, B	1.0	5.1		5.6			
t_{PHZ}, t_{PLZ}	Output Disable Time, Select to Bus B	1.0	5.2		5.5	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2
	Output Disable Time, Output Enable Time, $\overline{OE}$ to Bus A, B	1.5	5.5		5.5			

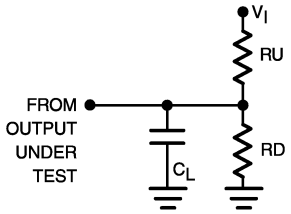
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol		Parameter	Typ	Max	Units	Conditions
C_{IN}		Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	A Port	Input/Output Capacitance	7		pF	V_{CC}, $\overline{OE}$ = 5.0V
	B Port		5		pF	

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

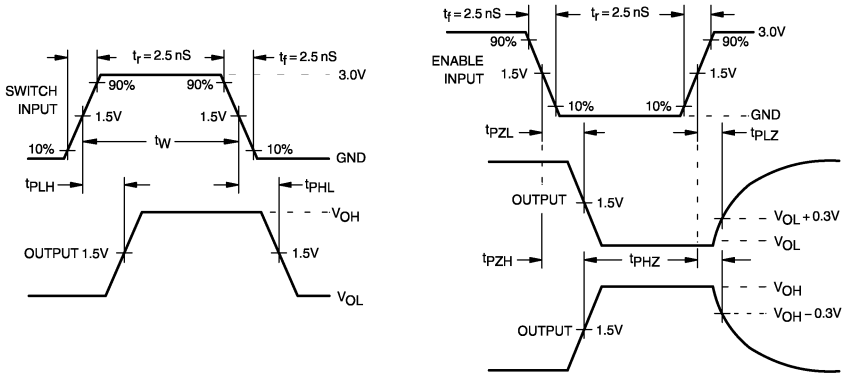
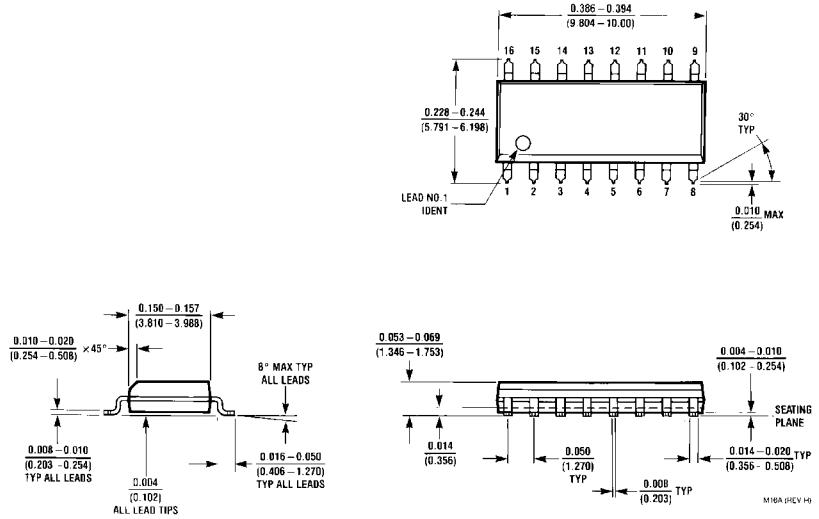
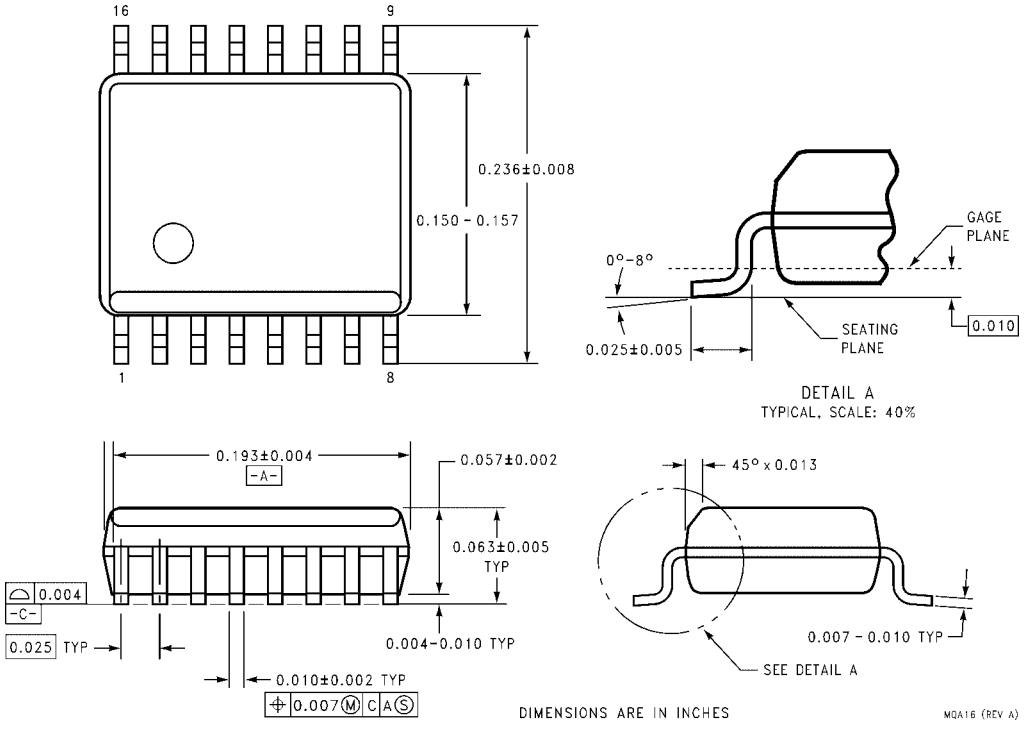


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

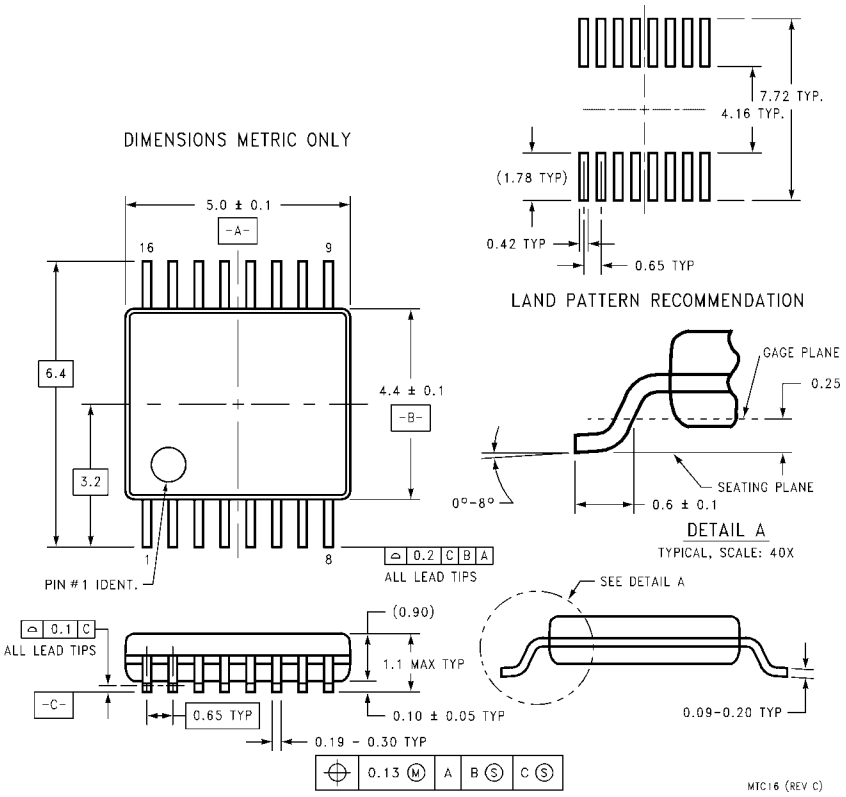


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

June 1997
Revised December 1999

FST3345
8-Bit Bus Switch

General Description

The Fairchild Switch FST3345 provides 8-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as an 8-bit switch bank with dual output enable inputs (OE and $\overline{OE}$). When $\overline{OE}$ is LOW or OE is HIGH, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH and OE is LOW, the switch is OPEN and a high-impedance state exists between the two ports.

Features

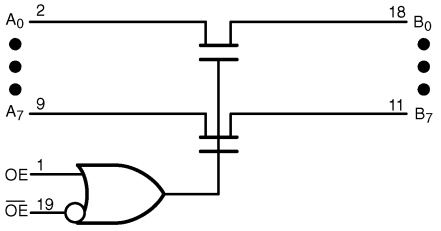
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

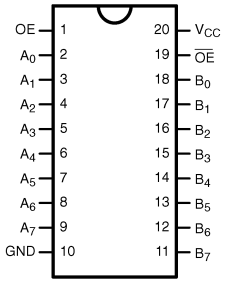
Order Number	Package Number	Package Description
FST3345WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
FST3345QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3345MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
OE, $\overline{OE}$	Bus Switch Enables
A	Bus A
B	Bus B

Truth Table

Inputs		Function
OE	$\overline{OE}$	
X	L	Connect
H	X	Connect
L	H	Disconnect

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = -18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,^\circ C$ to $+85\,^\circ C$, $C_L = 50$ pF, RU = RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	6.5		7.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.0	8.0		8.2	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

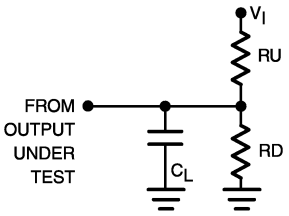
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	4		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	5		pF	V_{CC}, $\overline{OE}$ = 5.0V, OE = 0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz t_W = 500 nS

FIGURE 1. AC Test Circuit

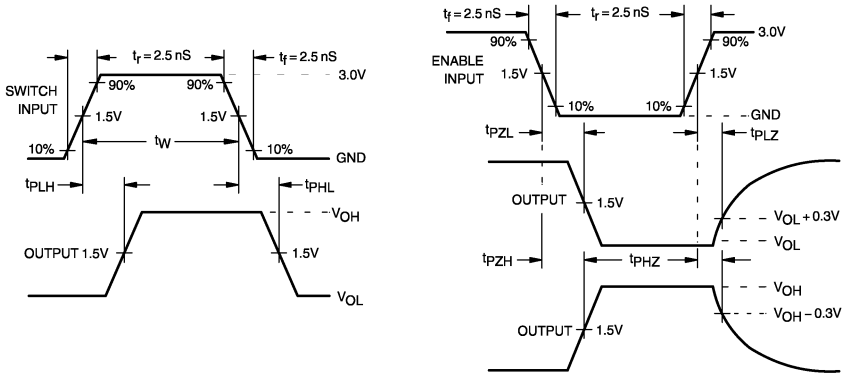
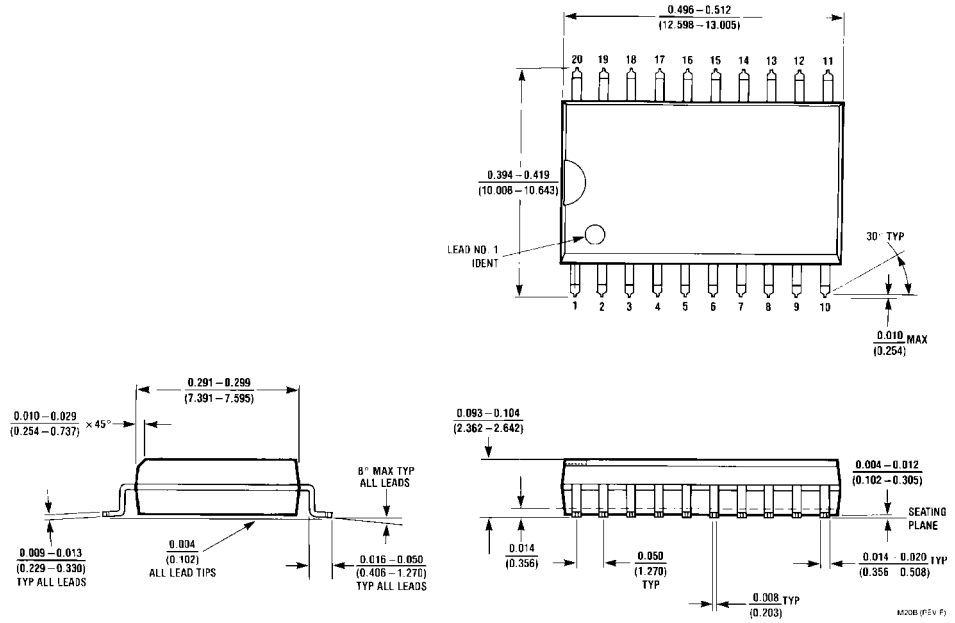
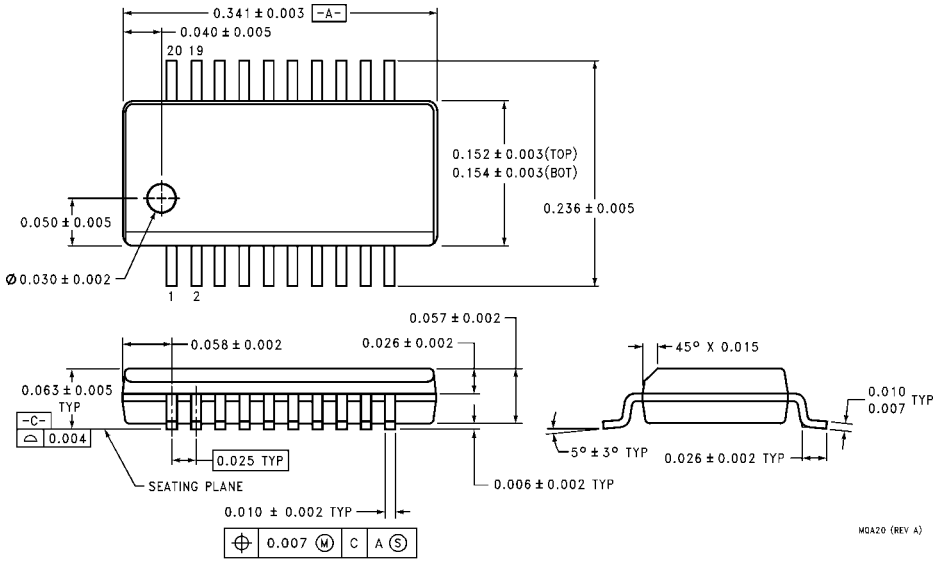


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

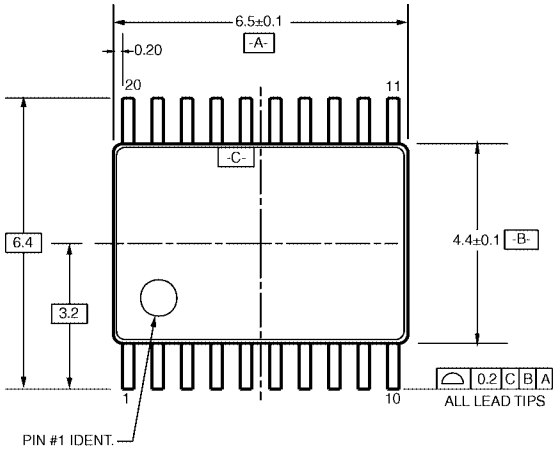


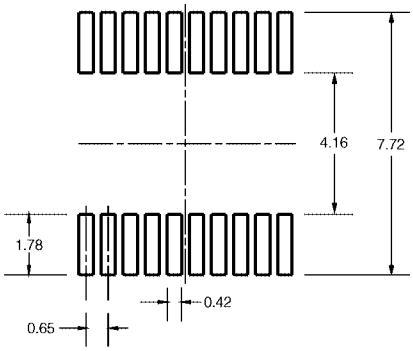
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B



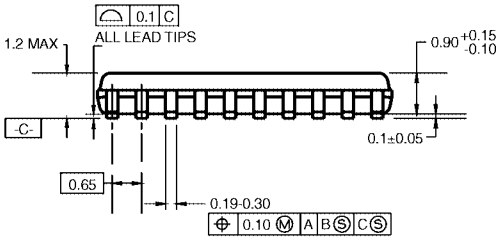
20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA20

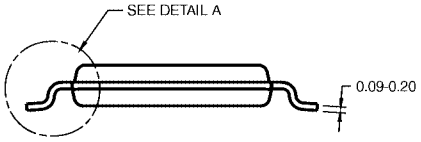
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS

NOTES:

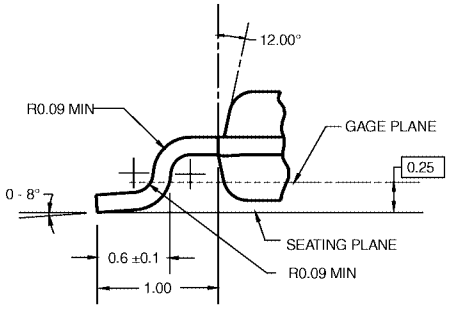
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1



DETAIL A

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

December 1993
Revised May 1999

FST3383
10-Bit Low Power Bus-Exchange Switch

General Description

The FST3383 provides two sets of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device operates as a 10-bit bus switch or a 5-bit bus exchanger. The bus exchange (BX) signal provides nibble swapping of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters. The bus enable ($\overline{BE}$) signal turns the switches ON.

Features

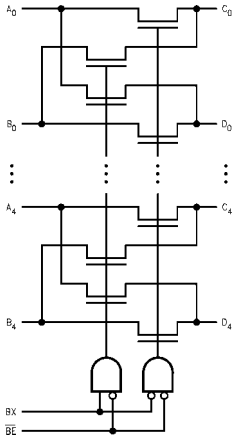
- 5Ω switch connection between two ports
- Zero propagation delay
- Ultra low power with 0.2 µA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level

Ordering Code:

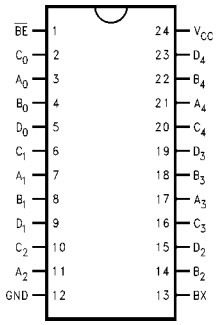
Order Number	Package Number	Package Description
FST3383WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
FST3383QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3383MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{BE}$	Bus Switch Enable
BX	Bus Exchange
A_0–A_4, B_0–B_4	Buses A, B
C_0–C_4, D_0–D_4	Buses C, D

Truth Table

$\overline{BE}$	BX	A_0–A_4	B_0–B_4	Function
H	X	High-Z State	High-Z State	Disconnect
L	L	C_0–C_4	D_0– D_4	Connect
L	H	D_0–D_4	C_0–C_4	Exchange

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_I) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IN}) with $V_I < 0$	−20 mA
DC Output (I_O) Sink Current	120 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation	0.5W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.0V to 5.5V
Free Air Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
			Min	Typ (Note 3)	Max		
V_{IK}	Maximum Clamp Diode Voltage	4.75			−1.2	V	$I_{IN} = -18$ mA
V_{IH}	Minimum High Level Input Voltage	4.75–5.25	2.0			V	
V_{IL}	Maximum Low Level Input Voltage	4.75–5.25			0.8	V	
I_{IN}	Maximum Input	0			10	µA	$0 \le V_{IN} \le 5.25V$
	Leakage Current	5.25			±1		
I_{OZ}	Maximum 3-STATE I/O Leakage	5.25			±10	µA	$0 \le A, B \le V_{CC}$
I_{OS}	Short Circuit Current	4.75	100			mA	$V_I(A)$, $V_I(B) = 0V$, $V_I(B)$, $V_I(A) = 4.75V$
R_{ON}	Switch On Resistance (Note 4)	4.75		5	7	Ω	$V_I = 0V$, $I_{ON} = 30$ mA
				10	15	Ω	$V_I = 2.4V$, $I_{ON} = 15$ mA
I_{CC}	Maximum Quiescent Supply Current	5.25		0.2	10	µA	$V_I = V_{CC}$, GND, $I_O = 0$
ΔI_{CC}	Increase in I_{CC} per Input (Note 5)	5.25			2.5	mA	$V_{IN} = 3.15V$, $I_O = 0$, Per Control Input

Note 3: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

Note 4: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: Per TTL driven input ($V_{IN} = 3.15V$, control inputs only). A and B pins do not contribute to I_{CC}.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units
			Min	Typ (Note 6)	Max	
t_{PLH}, t_{PHL}	Data Propagation Delay A_n to C_n, D_n or B_n to D_n, C_n (Note 7)	4.75			0.25	ns
t_{PLH}, t_{PHL}	Switch Exchange Time BX to A_n, B_n, C_n, D_n	4.75	1.5		6.5	ns
t_{PZL}, t_{PZH}	Switch Enable Time $\overline{BE}$ to A_n, B_n, C_n or D_n	4.75	1.5		6.5	ns
t_{PLZ}, t_{PHZ}	Switch Disable Time $\overline{BE}$ to A_n, B_n, C_n, or D_n	4.75	1.5		5.5	ns

Note 6: All typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

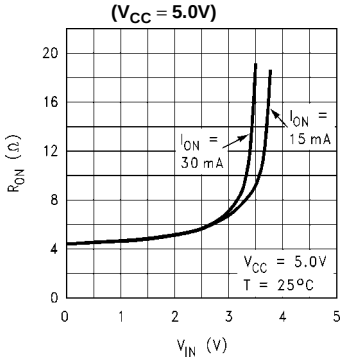
Note 7: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Capacitance (Note 8)

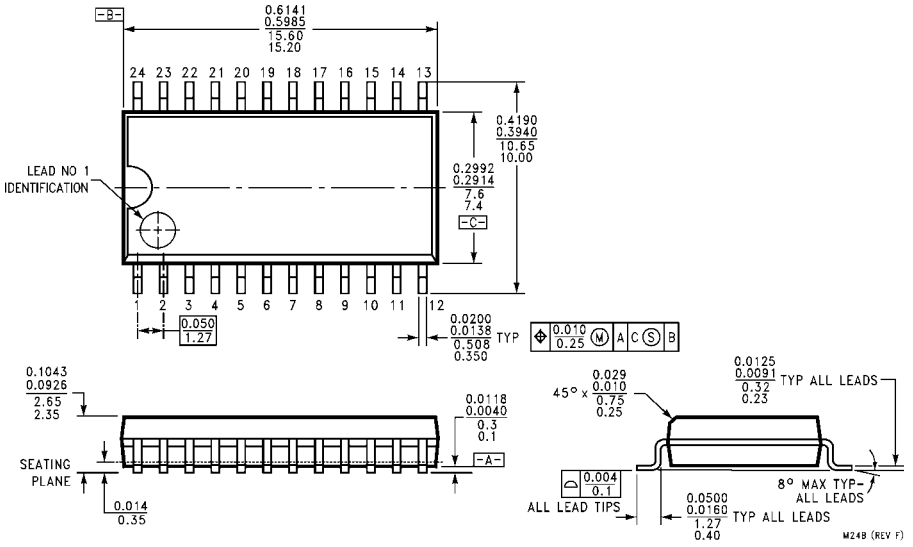
Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	4	6	pF	$V_{CC} = 5.0V$
$C_{I/O}$ (OFF)	Input/Output Capacitance	9	13	pF	$V_{CC} = 5.0V$

Note 8: Capacitance is characterized but not tested.

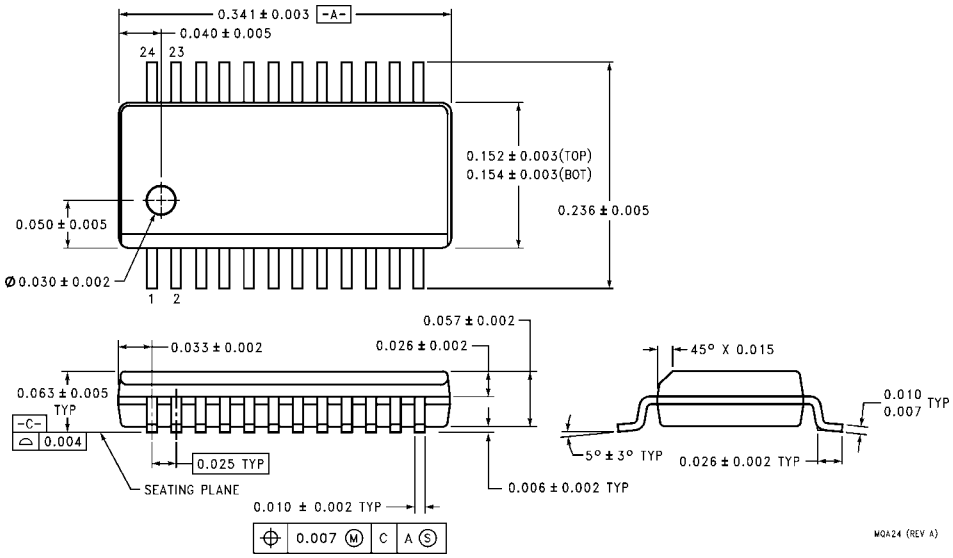
On-Resistance (R_{ON}) vs Input Voltage ($V_{CC} = 5.0V$)



Physical Dimensions inches (millimeters) unless otherwise noted

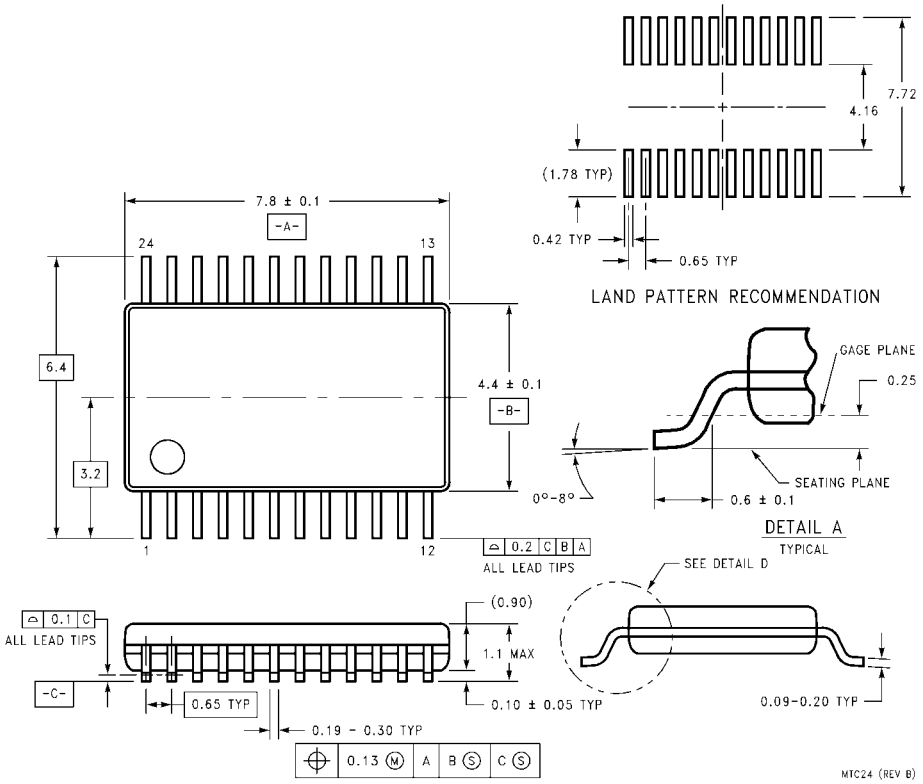


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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FAIRCHILD SEMICONDUCTOR™

September 1997
Revised December 1999

FST3384
10-Bit Low Power Bus Switch

General Description

The Fairchild Switch FST3384 provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ($\overline{OE}$) signals. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

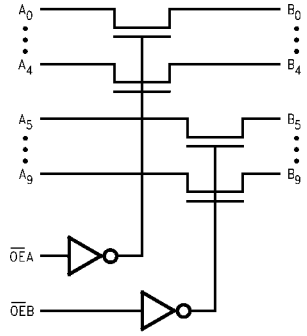
- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Ultra low power with < 0.1 µA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level

Ordering Code:

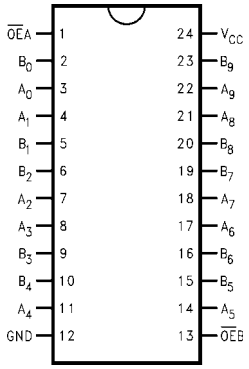
Order Number	Package Number	Package Description
FST3384WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
FST3384QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3384MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OEA}$, $\overline{OEB}$	Bus Switch Enable
A_0–A_9	Bus A
B_0–B_9	Bus B

Truth Table

$\overline{OEA}$	$\overline{OEB}$	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50 mA
DC Output (I_{OUT}) Sink Current	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C			Units	Condition
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN}= − 18mA
V_{IH}	HIGH Level Input Voltage	4.0-5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0-5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: All typical values are at V_{CC} = 5.0V, T_A = 25°C.

Note 5: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, RU = RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}_A$, $\overline{OE}_B$ to An, Bn	1.0	5.7		6.2	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}_A$, $\overline{OE}_B$ to An, Bn	1.5	5.2		5.5	ns	I_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

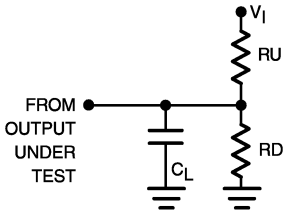
Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	3	6	pF	V_{CC} = 5.0V
$C_{I/O}$ (OFF)	Input/Output Capacitance	5	13	pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: Capacitance is characterized but not tested.

AC Loading and Waveforms



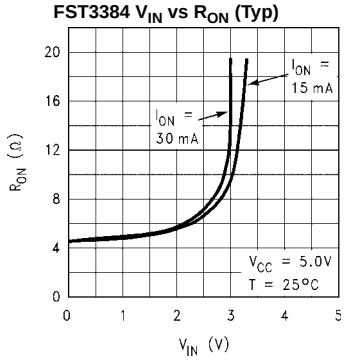
Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 nS

FIGURE 1. AC Test Circuit

FST3384 V_{IN} vs R_{ON} (Typ)



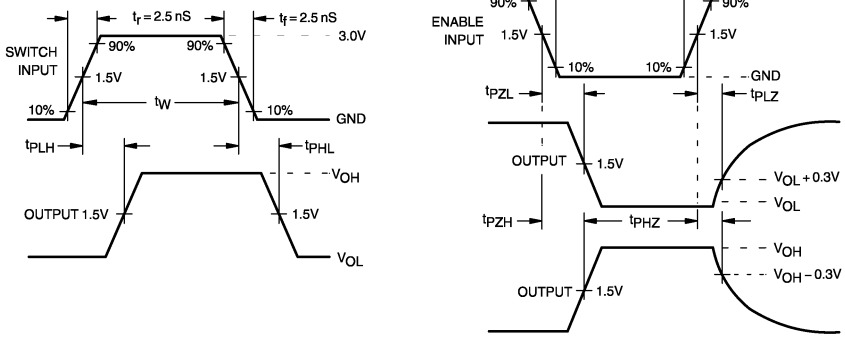
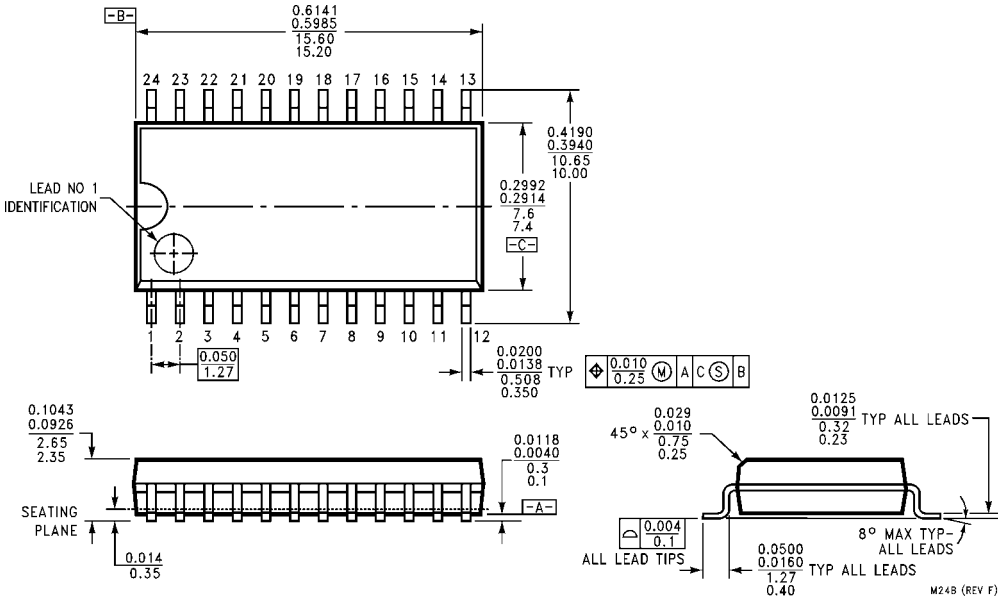
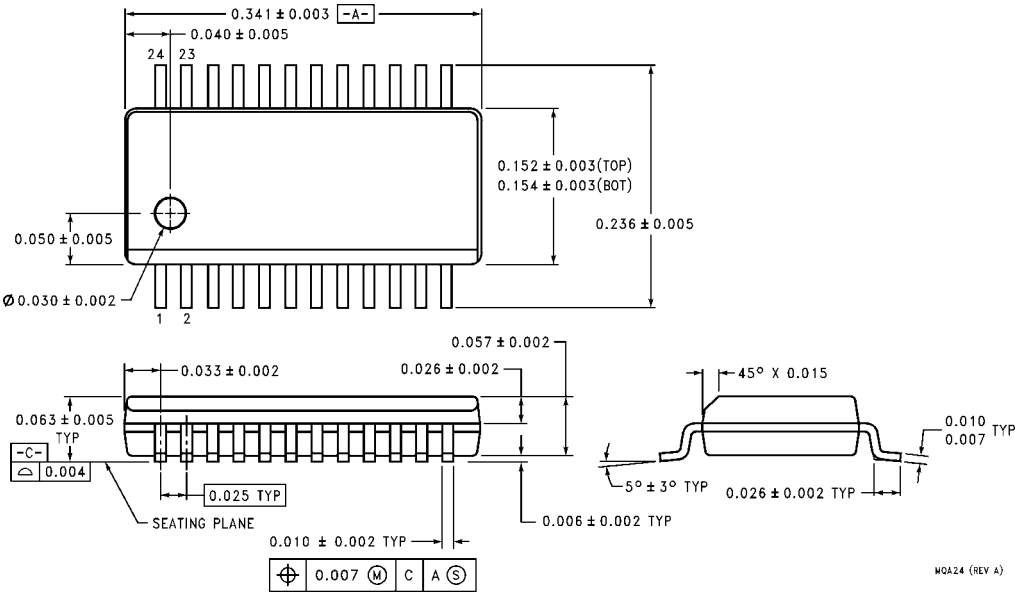


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

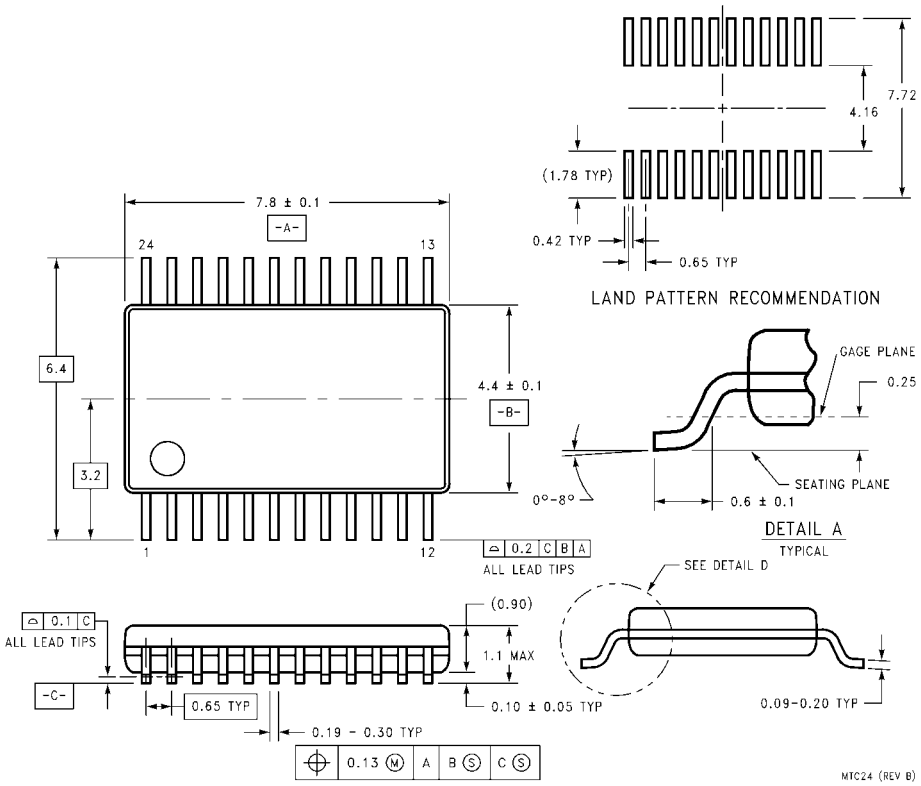


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

February 1998

FST3384A
10-Bit Low Power Extended Input Voltage Bus Switch

General Description

The FST3384A provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ($\overline{BE}$) signals. When $\overline{BE}$ is low, the switch is on and port A is connected to port B. When $\overline{BE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The FST3384A 10-bit bus switch is pin-for-pin and function compatible with the FST3384 device. It has the added feature of allowing extended negative input voltages on the I/O pins. The FST3384A bus switch, unlike most bus switches on the market, will not falsely turn on when $\overline{BE}$ is high and negative undershoot voltages are encountered on the I/O pins. Thus it is "undershoot hardened" (see related application note) tolerating undershoots up to −1.5V.

Typical applications include IDE bus connector interfaces, PCI card interfaces, backplane card interfaces, and other noisy environments where switches are needed.

Features

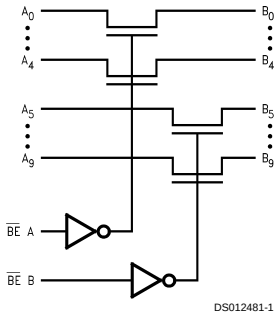
- Extended input voltage design tolerates input undershoots up to −1.5V
- 10Ω switch connection between two ports
- Ultra low power with 2 µA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC, QSOP and TSSOP

Ordering Code:

Order Number	Package Number	Package Description
FST3384AQSC	MQA24	24-Lead (0.150" Wide) Shrink Small Outline Package, QSOP
FST3384AMTC	MTC24	24-Lead Thin Small Outline Package, TSSOP

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

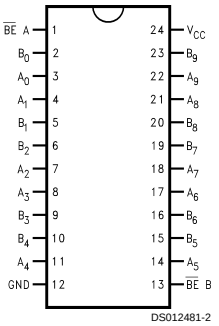
Logic Diagram



DS012481-1

Connection Diagram

Pin Assignment
SOIC, QSOP and TSSOP



DS012481-2

Pin Descriptions

Pin Names	Description
$\overline{BE}$ A, $\overline{BE}$ B	Bus Switch Enable
A_0–A_9	Bus A
B_0–B_9	Bus B

Truth Table

$\overline{BE}$ A	$\overline{BE}$ B	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5 to +7.0V
DC Input Input Voltage (V_I) (Note 2)	−0.5 to +7.0V
DC Input Diode Current with ($V_I < 0$)	−20 mA
DC Output (I_O) Sink Current	120 mA
Storage Temperature Range (T_{STG})	−65˚C to +150˚C
Power Dissipation	0.5W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.0V to 5.5V
Free Air Operating Temperature (T_A)	−40˚C to +85˚C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40˚C to +85˚C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Maximum Clamp Diode Voltage	4.75			−1.2	V	I_{IN} = −18 mA
V_{IH}	Minimum High Level Input Voltage	4.75–5.25	2.0			V	
V_{IL}	Maximum Low Level Input Voltage	4.75–5.25			0.8		
I_{IN}	Maximum Input Leakage Current	0			10	μA	0 ≤ V_{IN} ≤ 5.25V
		5.25			±1		
I_{OZ}	Maximum 3-STATE I/O Leakage	5.25			±10	μA	0 ≤ A, B ≤ V_{CC}
I_{OS}	Short Circuit Current	4.75	100			mA	V_I(A), V_I(B) = 0V, V_I(B), V_I(A) = 4.75V
R_{ON}	Switch On Resistance (Note 3)	4.75		6	12	Ω	V_I = 0V, I_{ON} = 30 mA
				15	25	Ω	V_I = 2.4V, I_{ON} = 15 mA
I_{CC}	Maximum Quiescent Supply Current	5.25		0.2	10	μA	V_I = V_{CC}, GND I_O = 0
ΔI_{CC}	Increase in I_{CC} per Input (Note 4)	5.25			2.5	mA	V_{IN} = 3.15V, I_O = 0 Per Control Input

Note 3: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 4: Per TTL driven Input (V_{IN} = 3.15V, control inputs only). A and B pins do not contribute to I_{CC}.

Note 5: All typical values are at V_{CC} = 5.0V, T_A = 25˚C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40^\circ C$ to $+85^\circ C$, $C_L = 50$ pF			Units
			Min	Typ (Note 6)	Max	
t_{PLH} t_{PHL}	Data Propagation Delay A_n to B_n or B_n to A_n (Note 7)	4.75			0.50	ns
t_{PZL} t_{PZH}	Switch Enable Time $\overline{BE}$ A, $\overline{BE}$ B to A_n, B_n	4.75	1.5		6.8	ns
t_{PLZ} t_{PHZ}	Switch Disable Time $\overline{BE}$ A, $\overline{BE}$ B to A_n, B_n	4.75	1.5		6.0	ns

Note 6: All typical values are at $V_{CC} = 5.0V$, $T_A = 25^\circ C$.

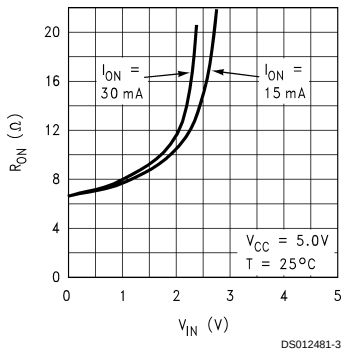
Note 7: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.5 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Capacitance (Note 8)

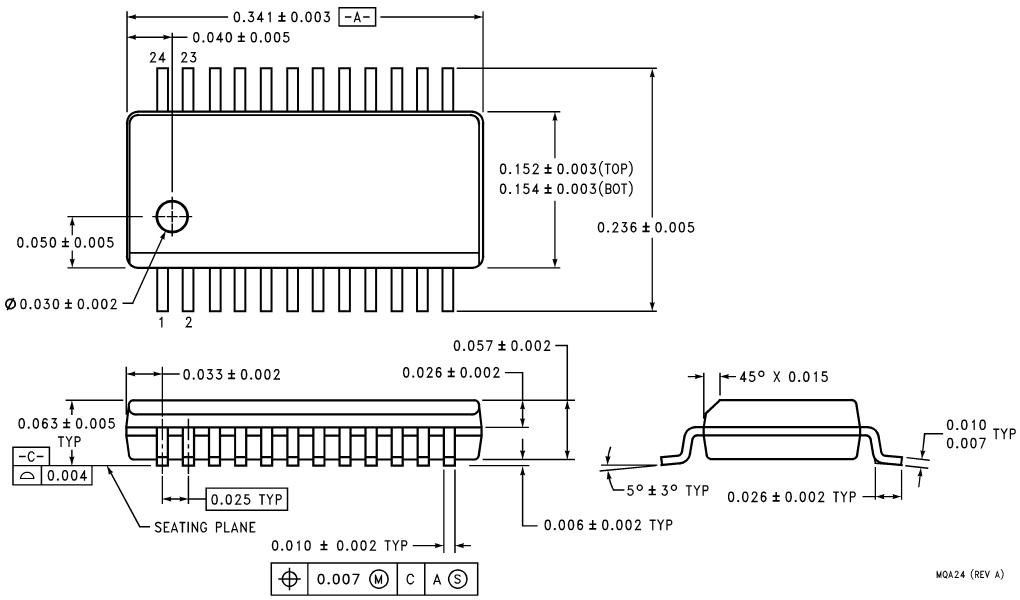
Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	4	6	pF	$V_{CC} = 5.0V$
$C_{I/O}$ (OFF)	Input/Output Capacitance	9	13	pF	$V_{CC} = 5.0V$

Note 8: Capacitance is characterized but not tested.

FST3384A V_{IN} vs R_{ON} (Typ)

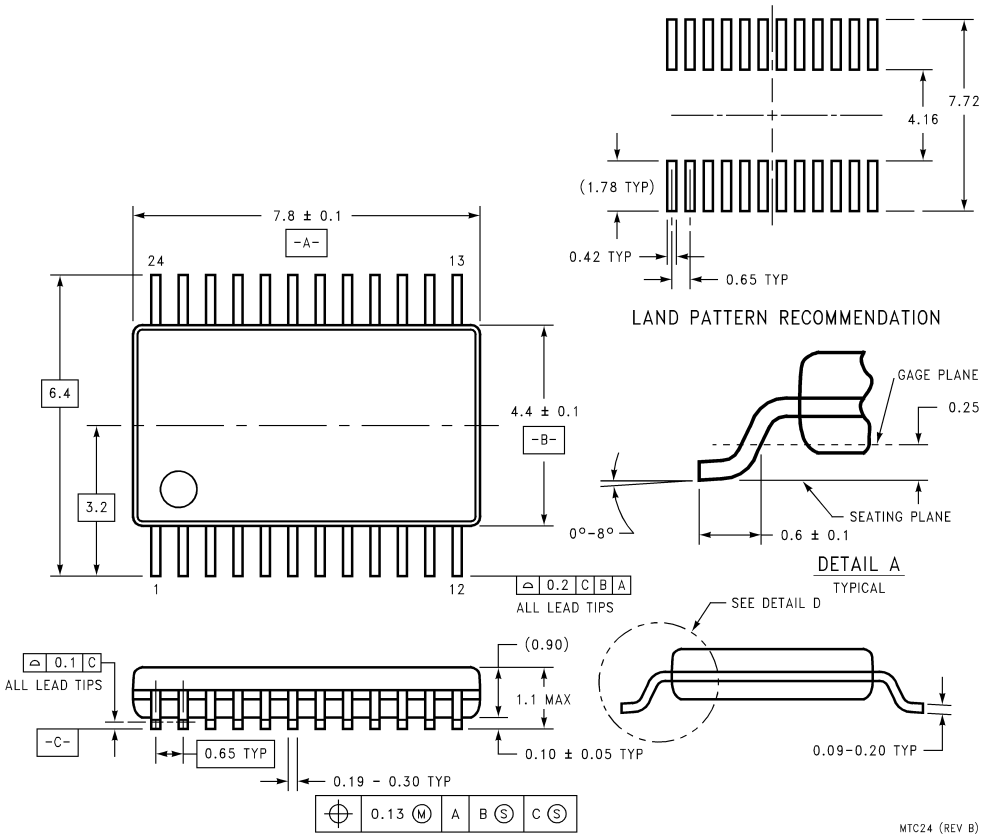


Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead (0.150" Wide) Shrink Small Outline Package, JEDEC (QSC)
(also known as QSOP)
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Small Outline Package, JEDEC (MTC)
Package Number MTC24

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FAIRCHILD SEMICONDUCTOR™

June 1997
Revised December 1999

FST6800
10-Bit Bus Switch with Pre-Charged Outputs

General Description

The Fairchild Switch FST6800 provides 10-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device precharges the B Port to a selectable bias voltage (BiasV) to minimize live insertion noise.

The device is organized as a 10-bit switch with a bus enable ($\overline{OE}$) signal. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and the B Port is precharged to BiasV through an equivalent 10-kΩ resistor.

Features

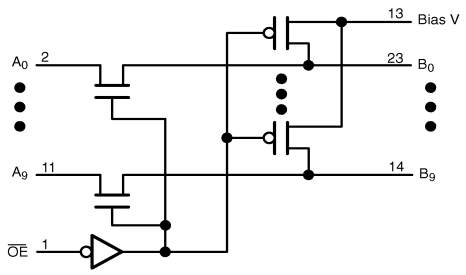
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Output precharge to minimize live insertion noise.
- Control inputs compatible with TTL level.

Ordering Code:

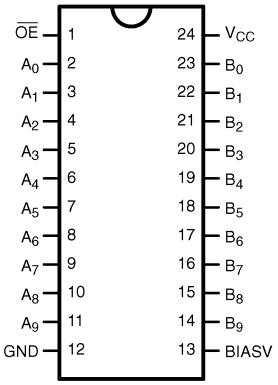
Order Number	Package Number	Package Description
FST6800WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
FST6800QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST6800MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
A	Bus A
B	Bus B

Truth Table

$\overline{OE}$	B_0–B_9	Function
L	A_0–A_9	Connect
H	BiasV	Precharge

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–0.5V to +7.0V
Bias V Voltage Range	–0.5V to +6.0V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Precharge Supply (BiasV)	1.5V to V_{CC}
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_O	Output Current	4.5	0.25			mA	BiasV = 2.4V, B = 0
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A ≤V_{CC}
R_{ON}	Switch On Resistance (Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A= +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 – 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figures 1, 2
t_{PZH}	Output Enable Time	1.5	6.2		6.5	ns	V_I = OPEN, BiasV = GND	Figure 1 Figure 2
t_{PZL}		1.5	6.2		6.5	ns	V_I = 7V, BiasV = 3V	
t_{PHZ}	Output Disable Time	1.5	6.1		6.5	ns	V_I = OPEN, BiasV = GND	Figure 1 Figure 2
t_{PLZ}		1.5	7.3		6.8	ns	V_I = 7V, BiasV = 3V	

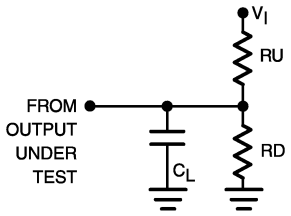
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	5		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

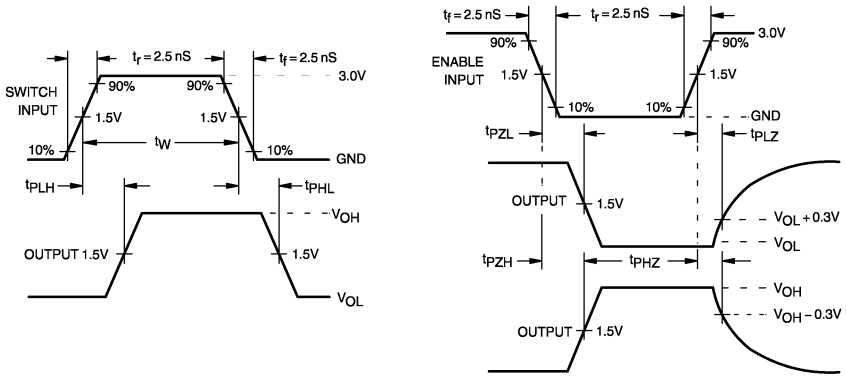
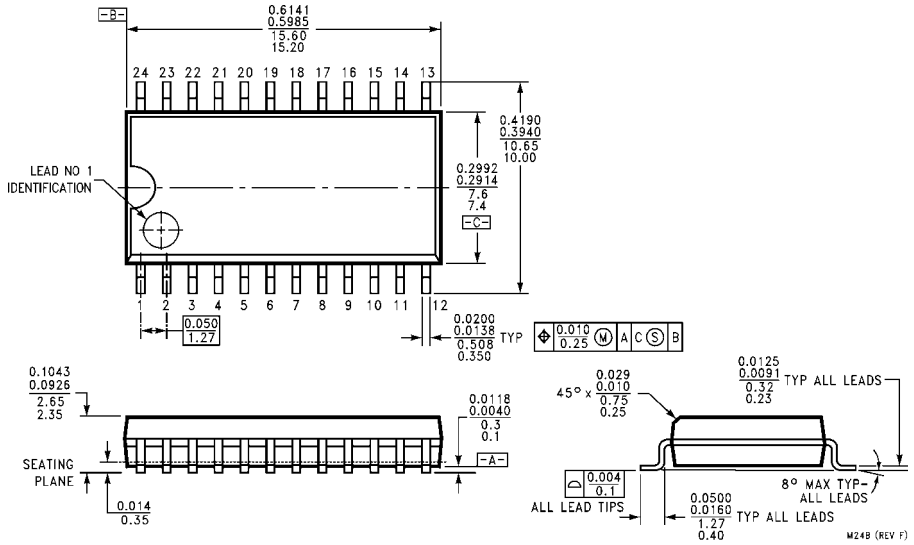
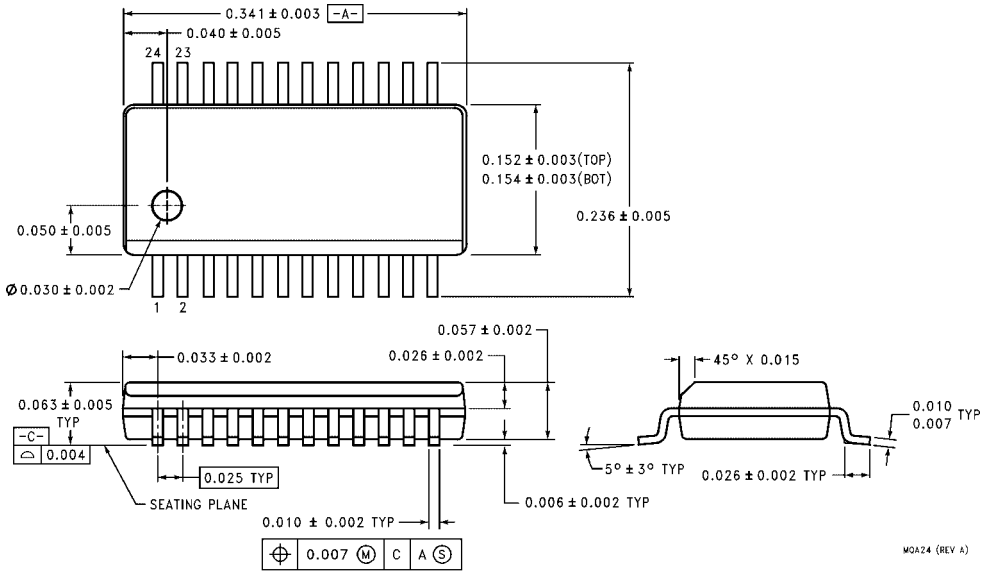


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

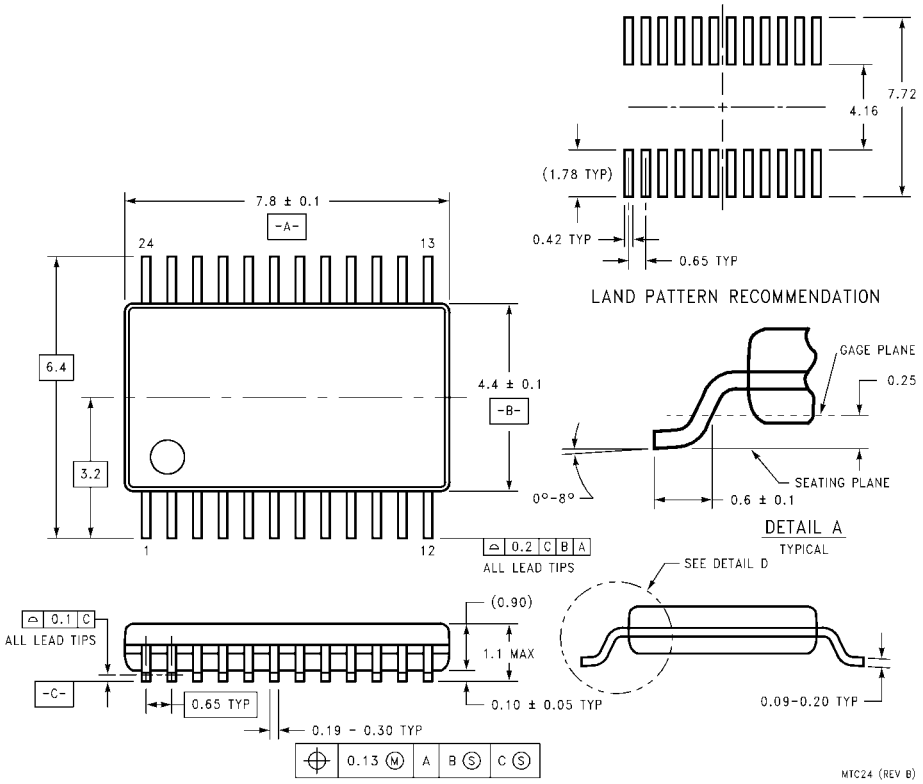


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

August 1999
Revised December 1999

FSTD16211
24-Bit Bus Switch with Level Shifting (Preliminary)

General Description

The Fairchild Switch FSTD16211 provides 24-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. A diode to V_{CC} has been integrated into the circuit to allow for level shifting between 5V inputs and 3.3V outputs.

The device is organized as a 12-bit or 24-bit bus switch. When $\overline{OE}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, Port 2A is connected to Port 2B. When $\overline{OE}_{1/2}$ is HIGH, a high impedance state exists between the A and B Ports.

Features

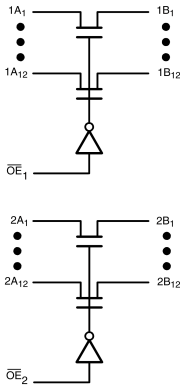
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

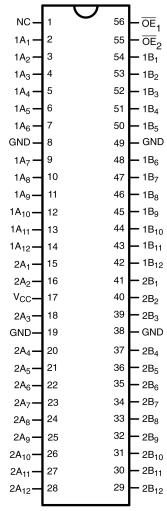
Order Number	Package Number	Package Description
FSTD16211MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	–0.5V to +7.0V
DC Input Control Pin Voltage (V_{IN})(Note 3)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	–50mA
DC Output (I_{OUT})	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
V_{OH}	HIGH Level	4.0–5.5	See Figure 3			V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 6)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		35	50	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		TBD	TBD	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			1.5	mA	OE_1 = OE_2 = GND V_{IN} = V_{CC} or GND, I_{OUT} = 0
					10	µA	OE_1 = OE_2 = V_{CC} V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 5: Typical values are at V_{CC} = 5.0V and T_A= +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,^\circ C$ to $+85\,^\circ C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 7)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	10.0		11.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	9.0		10.0	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1 Figure 2

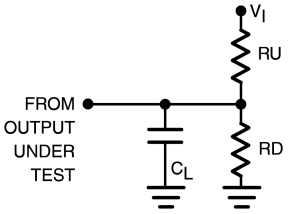
Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical ON resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	6		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 8: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: CL includes load and stray capacitance

Note: Input PRR = 1.0 MHz, T_W = 500 ns

FIGURE 1. AC Test Circuit

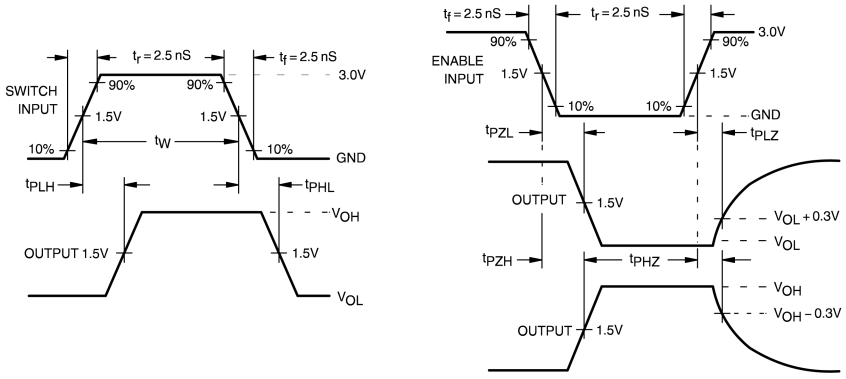
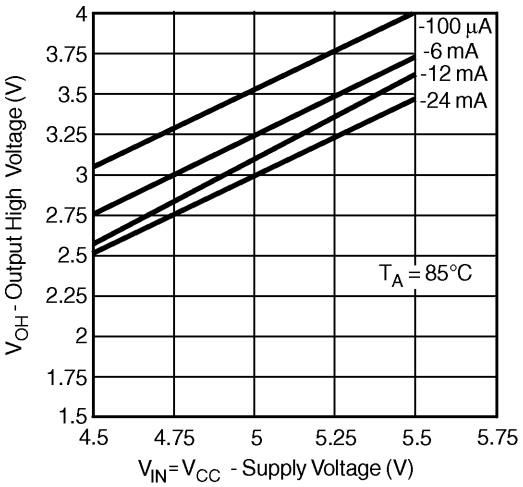
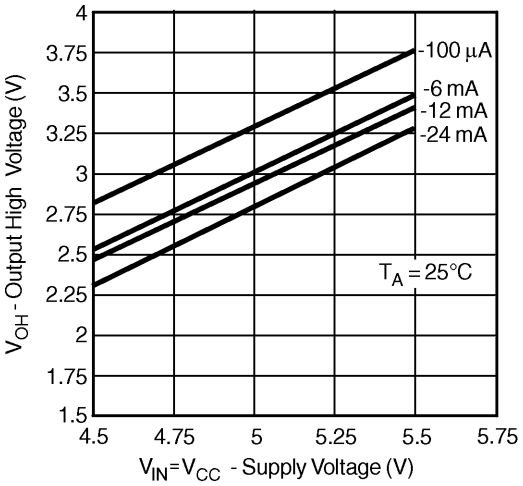


FIGURE 2. AC Waveforms

Output Voltage HIGH vs. Supply Voltage





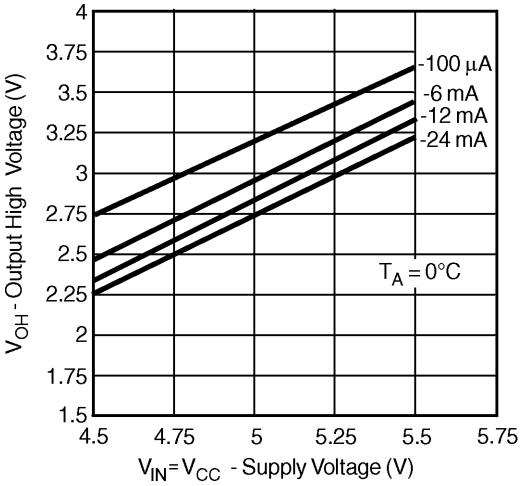
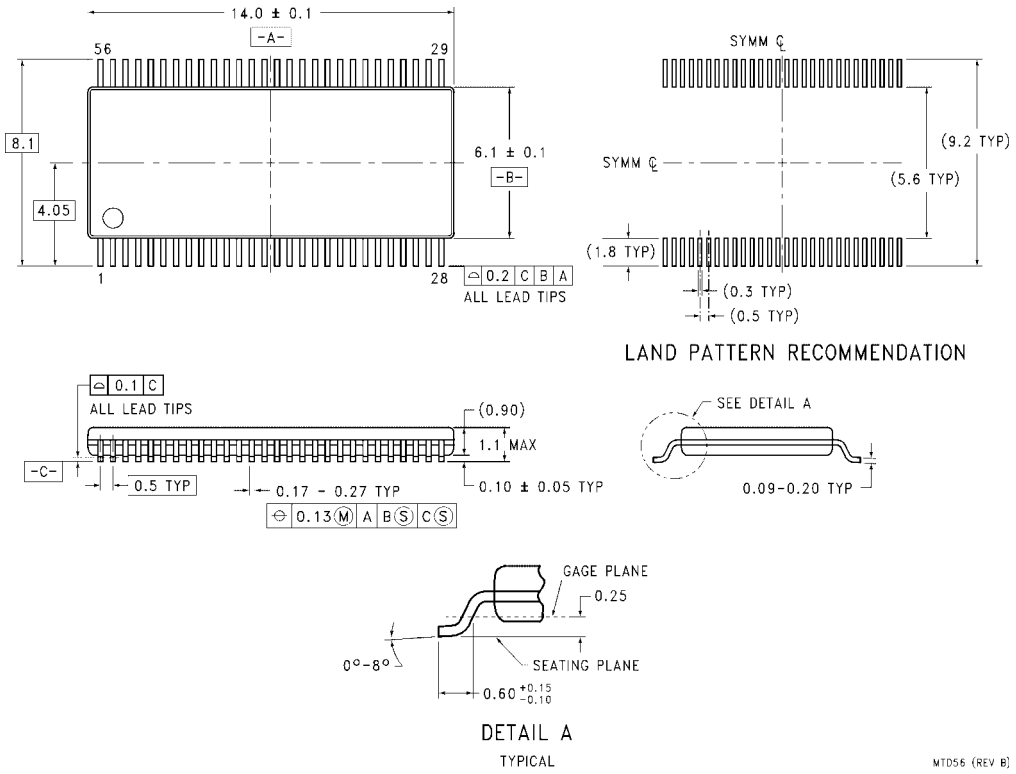


FIGURE 3.

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

May 1999
Revised November 1999

FSTU32160
16-Bit to 32-Bit Multiplexer/Demultiplexer Bus Switch with –2V Undershoot Hardened Circuit (UHC™) Protection

General Description

The Fairchild Switch FSTU32160 is a 16-bit to 32-bit high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device can be used in applications where two buses need to be addressed simultaneously. The FSTU32160 is designed so that the A Port demultiplexes into B_1 or B_2 or both. The A and B Ports are "undershoot hardened" with UHC™ protection to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit, UHC senses undershoot at the I/O's, and responds by preventing voltage differentials from developing and turning on the switch.

Two select (SEL_1, SEL_2) inputs provide switch enable control. When SEL_1, SEL_2 are HIGH, the device precharges the B Port to a selectable bias voltage (Bias V) to minimize live insertion noise.

Features

- Undershoot hardened to –2V (A and B Ports).
- Slower Output Enable times prevent signal disruption
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.
- See Applications Note AN-5008 for details

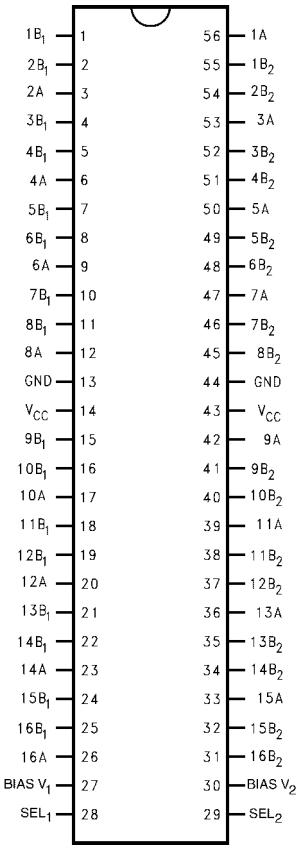
Ordering Code:

Order Number	Package Number	Package Description
FSTU32160MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

UHC™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagram



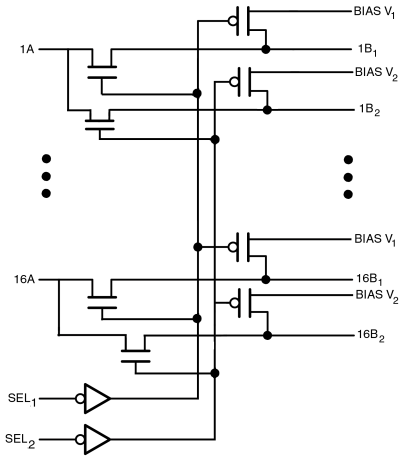
Pin Descriptions

Pin Name	Description
SEL_1, SEL_2	Select Inputs
A	Bus A
B_1, B_2	Bus B

Truth Table

Inputs		Function
SEL_1	SEL_2	
L	H	x A = x B_1
H	L	x A = x B_2
L	L	x A = x B_1 and x B_2
H	H	x B_1, x B_2 = BiasV

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−2.0V to +7.0V
BiasV Voltage Range	−0.5V to +7.0V
DC Input Control Pin Voltage (V_{IN}) (Note 3)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	−50 mA
DC Output Current (I_{OUT})	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100 mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Precharge Supply (BiasV)	1.5 to V_{CC}
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
		0			10	µA	V_{IN} = 5.5V
I_O	Output Current	4.5	0.25			mA	BiasV = 2.4V, SEL_X = 2.0V B_X = 0
I_{OZH}, I_{OZL}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, ≤ V_{CC}, V $BiasV_1$ = $BiasV_2$ = 5.5V
I_{OZH}, I_{OZL}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ B, ≤ V_{CC}, V $BiasV_1$ = $BiasV_2$ = FLOATING
R_{ON}	Switch On Resistance (Note 6)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64 mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30 mA
		4.5		8	14	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND
I_{BIAS}	Bias Pin Leakage Current	5.5			±1.0	µA	SEL_1, SEL_2 = 0V B_X = 0V, $BiasV_X$ = 5.5V
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA ≥ I_{IN} ≥ −50 mA SEL_1, SEL_2 = 5.5V

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, RU= RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	A or B, to B or A (Note 7)		0.25		0.25	ns	V_I = OPEN	Figure 2 Figure 3
t_{PZH}	Output Enable Time, SEL to A, B	7.0	30.0		35.0	ns	V_I = OPEN for t_{PZH} BiasV = GND	Figure 2 Figure 3
t_{PZL}	Output Enable Time, SEL to A, B	7.0	30.0		35.0	ns	V_I = 7V for t_{PZL} BiasV = 3V	Figure 2 Figure 3
t_{PHZ}	Output Disable Time, SEL to A, B	1.0	6.9		7.3	ns	V_I = OPEN for t_{PHZ} BiasV = GND	Figure 2 Figure 3
t_{PLZ}	Output Disable Time, SEL to A, B	1.0	7.7		7.7	ns	V_I = 7V for t_{PLZ}, BiasV = 3V	Figure 2 Figure 3

Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	4		pF	V_{CC} = 5.0V
$C_{I/O\ OFF}$	Input/Output Capacitance "OFF State"	8		pF	V_{CC} = 5.0V, Switch OFF

Note 8: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	$V_{OH} - 0.3$		V	Figure 1

Note 9: This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

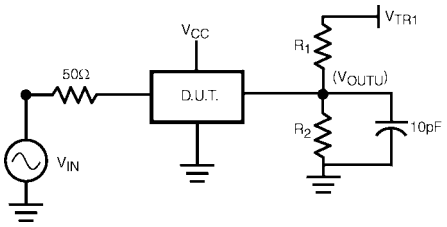
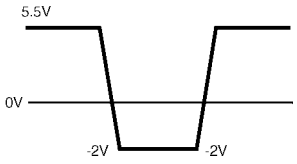


FIGURE 1.

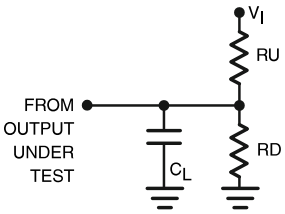
Device Test Conditions

Parameter	Value	Units
V_{IN}	see Waveform	V
$R_1 = R_2$	100K	Ω
V_{TRI}	11.0	V
V_{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance, C_L = 50 pF

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 2. AC Test Circuit

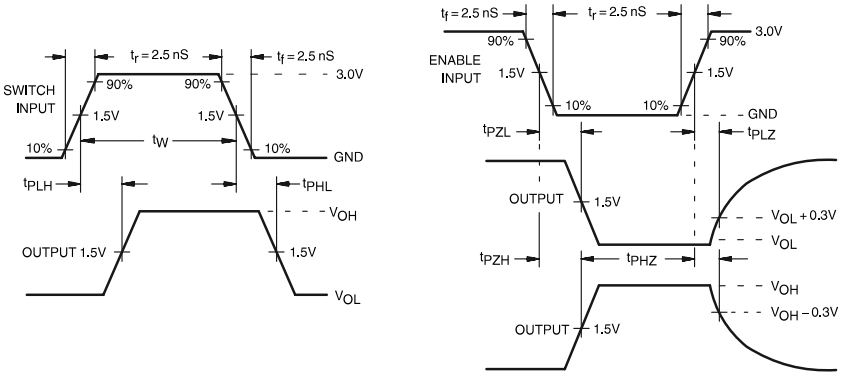
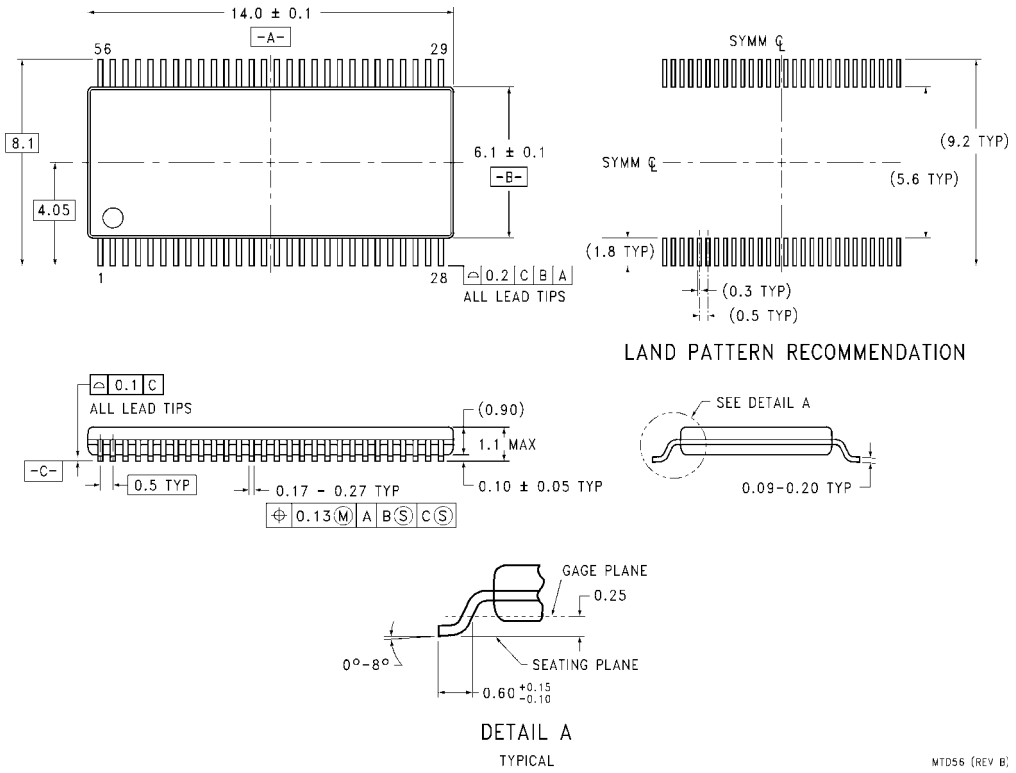


FIGURE 3. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

June 1999
Revised November 1999

FSTU32160A
16-Bit to 32-Bit Multiplexer/Demultiplexer Bus Switch with –2V Undershoot Hardened Circuit (UHC™) Protection

General Description

The Fairchild Switch FSTU32160A is a 16-bit to 32-bit high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device can be used in applications where two buses need to be addressed simultaneously. The FSTU32160A is designed so that the A Port demultiplexes into B_1 or B_2 or both. The A and B Ports are "undershoot hardened" with UHC™ protection to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit, UHC senses undershoot at the I/O's, and responds by preventing voltage differentials from developing and turning on the switch.

Two select (SEL_1, SEL_2) inputs provide switch enable control. When SEL_1, SEL_2 are HIGH, the device precharges the B Port to a selectable bias voltage (Bias V) to minimize live insertion noise.

Features

- Undershoot hardened to –2V (A and B Ports).
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.
- See Applications Note AN-5008 for details

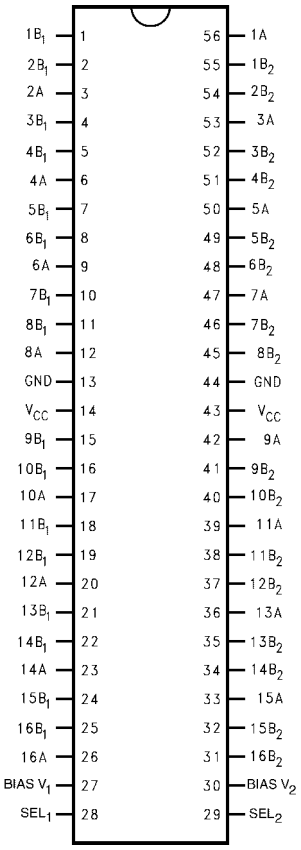
Ordering Code:

Order Number	Package Number	Package Description
FSTU32160AMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

UHC™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagram



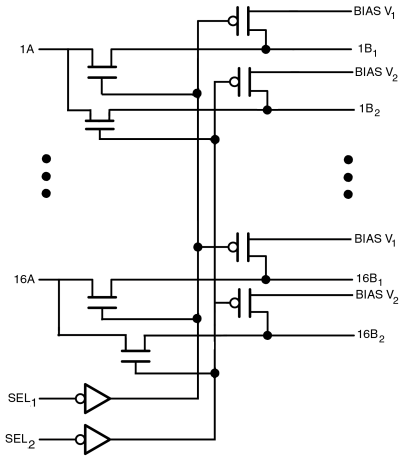
Pin Descriptions

Pin Name	Description
SEL_1, SEL_2	Select Inputs
A	Bus A
B_1, B_2	Bus B

Truth Table

Inputs		Function
SEL_1	SEL_2	
L	H	x A = x B_1
H	L	x A = x B_2
L	L	x A = x B_1 and x B_2
H	H	x B_1, x B_2 = BiasV

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−2.0V to +7.0V
BiasV Voltage Range	−0.5V to +7.0V
DC Input Control Pin Voltage (V_{IN}) (Note 3)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	−50 mA
DC Output Current (I_{OUT})	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100 mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Precharge Supply (BiasV)	1.5 to V_{CC}
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
		0			10	µA	V_{IN} = 5.5V
I_O	Output Current	4.5	0.25			mA	BiasV = 2.4V B_X = 0
I_{OZH}, I_{OZL}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A ≤ V_{CC}, V $BiasV_1$ = $BiasV_2$ = 5.5V
I_{OZH}, I_{OZL}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ B ≤ V_{CC}, V $BiasV_1$ = $BiasV_2$ = Floating
R_{ON}	Switch On Resistance (Note 6)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64 mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30 mA
		4.5		8	14	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND
I_{BIAS}	Bias Pin Leakage Current	5.5			±1.0	µA	SEL_1, SEL_2 = 0V B_X = 0V, $BiasV_X$ = 5.5V
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA ≥ I_{IN} ≥ −50 mA SEL_1, SEL_2 = 5.5V

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, RU= RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	A or B, to B or A (Note 7)		0.25		0.25	ns	V_I = OPEN	Figure 2 Figure 3
t_{PZH}	Output Enable Time, SEL to A, B	0.5	4.0		4.5	ns	V_I = OPEN for t_{PZH} BiasV = GND	Figure 2 Figure 3
t_{PZL}	Output Enable Time, SEL to A, B	1.0	4.8		5.5	ns	V_I = 7V for t_{PZL} BiasV = 3V	Figure 2 Figure 3
t_{PHZ}	Output Disable Time, SEL to A, B	1.0	5.9		6.9	ns	V_I = Open for t_{PHZ} BiasV = GND	Figure 2 Figure 3
t_{PLZ}	Output Disable Time, SEL to A, B	1.0	7.4		7.0	ns	V_I = 7V for t_{PLZ} BiasV = 3V	Figure 2 Figure 3

Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	4		pF	V_{CC} = 5.0V
$C_{I/O\ OFF}$	Input/Output Capacitance "OFF State"	8		pF	V_{CC} = 5.0V, Switch OFF

Note 8: T_A = +25°C, f = 1 Mhz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	$V_{OH} - 0.3$		V	Figure 1

Note 9: This is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

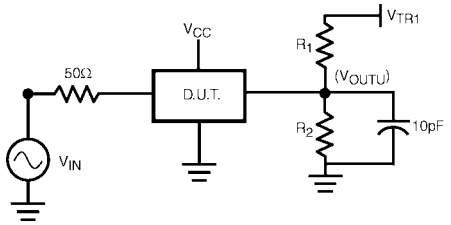
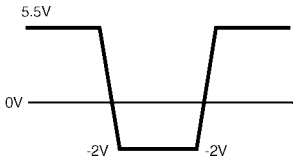


FIGURE 1.

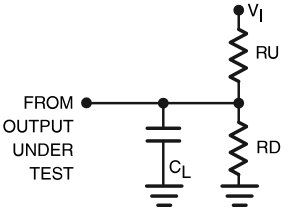
Device Test Conditions

Parameter	Value	Units
V_{IN}	See Waveform	V
R_1 - R_2	100K	Ω
V_{TRI}	11.0	V
V_{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance, C_L = 50 pF

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 2. AC Test Circuit

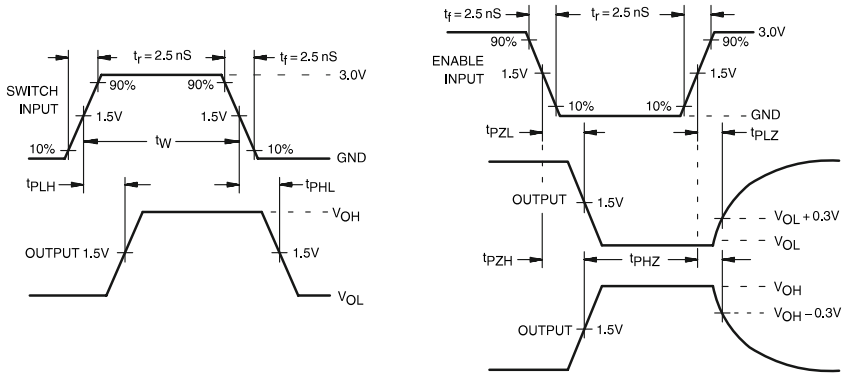
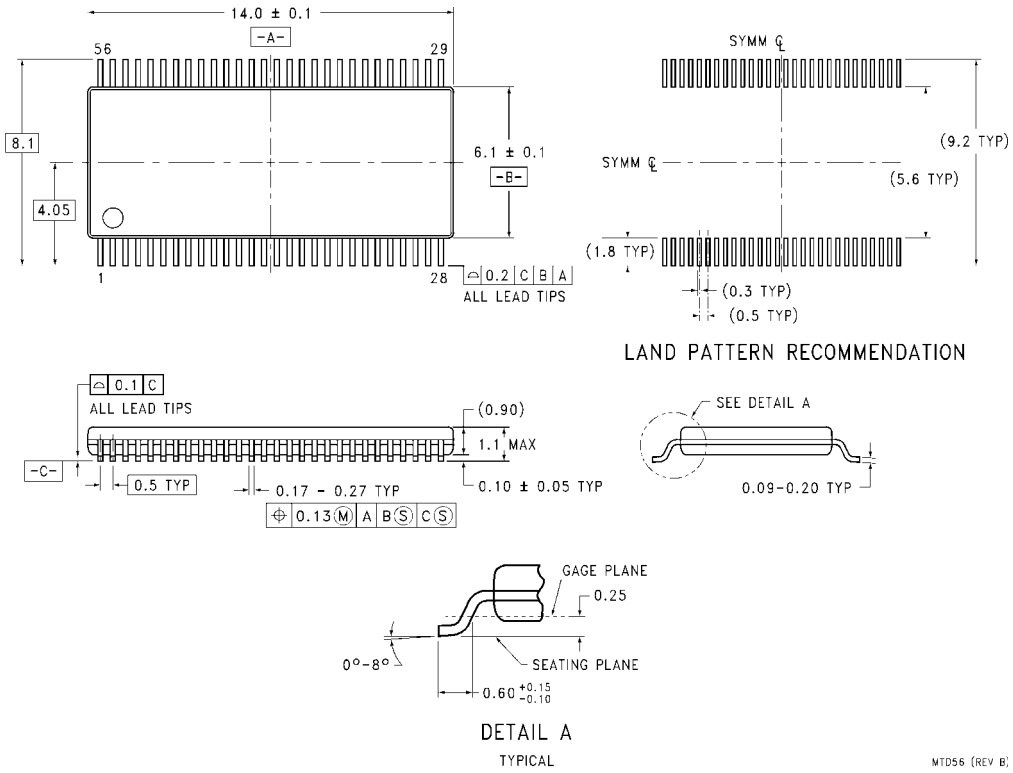


FIGURE 3. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

August 1999
Revised December 1999

FSTU3257
Quad 2:1 Multiplexer/Demultiplexer Bus Switch with –2V Undershoot Hardened Circuit (UHC™) Protection

General Description

The Fairchild Switch FSTU3257 is a quad 2:1 high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When $\overline{OE}$ is LOW, the select pin connects the A Port to the selected B Port output. The A and B Ports are "undershoot hardened" with UHC™ protection to support an extended range of 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit UHC senses undershoot at the I/O and responds by preventing voltage differentials from developing and turning on the switch. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

- Undershoot hardened to –2V (A and B Ports)
- Soft enable turn-on to minimize bus to bus charge sharing during enable
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.
- See Applications Note AN-5008 for details

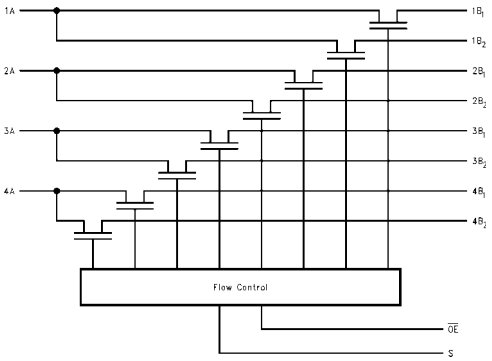
Ordering Code:

Order Number	Package Number	Package Description
FSTU3257QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FSTU3257MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

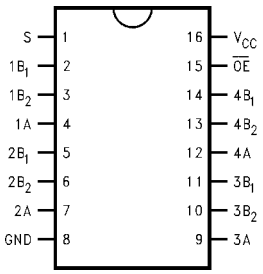
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

UHC™ is a trademark of Fairchild Semiconductor Corporation.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
S	Select Input
A	Bus A
B_1–B_2	Bus B

Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	$A = B_1$
H	L	$A = B_2$

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−2.0V to +7.0V
DC Input Control Pin Voltage (V_{IN})(Note 3)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT})	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance (Note 6)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	15	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA ≥ I_{IN} ≥ −50 mA $\overline{OE}$ = 5.5V

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 7)		0.25		0.25	ns	V_I = OPEN	Figure 2 Figure 3
	Prop Delay, Select to Bus A	7.0	30.0		35.0			
t_{PZH}, t_{PZL}	Output Enable Time, Select to Bus B	7.0	30.0		35.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 2 Figure 3
	Output Enable Time, $\overline{OE}$ to Bus A, B	7.0	30.0		35.0			
t_{PHZ}, t_{PLZ}	Output Disable Time, Select to Bus B	1.5	8.4		9.8	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 2 Figure 3
	Output Disable Time, Output Enable Time, $\overline{OE}$ to Bus A, B	1.5	8.8		9.8			

Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 8)

Symbol		Parameter	Typ	Max	Units	Conditions
C_{IN}		Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	A Port	Input/Output Capacitance	7.5		pF	V_{CC}, $\overline{OE}$ = 5.0V
	B Port		5.5		pF	
$C_{I/O}$ ON State		Input/Output Capacitance ON State (A or B Port)	14		pF	V_{CC} = 5.0V Switch ON

Note 8: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	$V_{OH} - 0.3$		V	Figure 1

Note 9: This is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

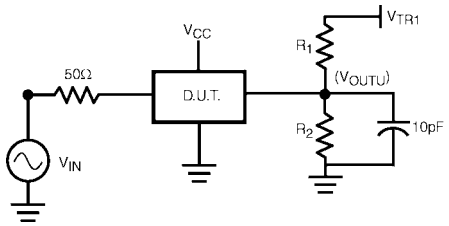
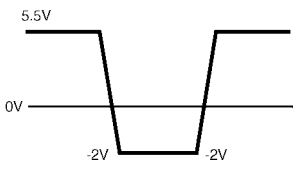


FIGURE 1.

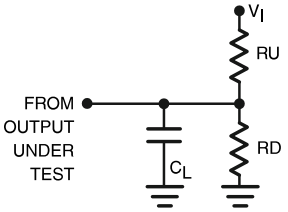
Device Test Conditions

Parameter	Value	Units
V_{IN}	See Waveform	V
R_1 - R_2	100K	Ω
V_{TRI}	11.0	V
V_{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 nS

FIGURE 2. AC Test Circuit

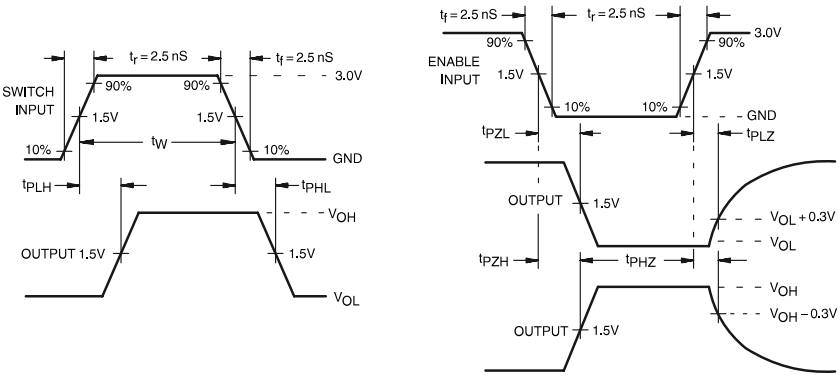
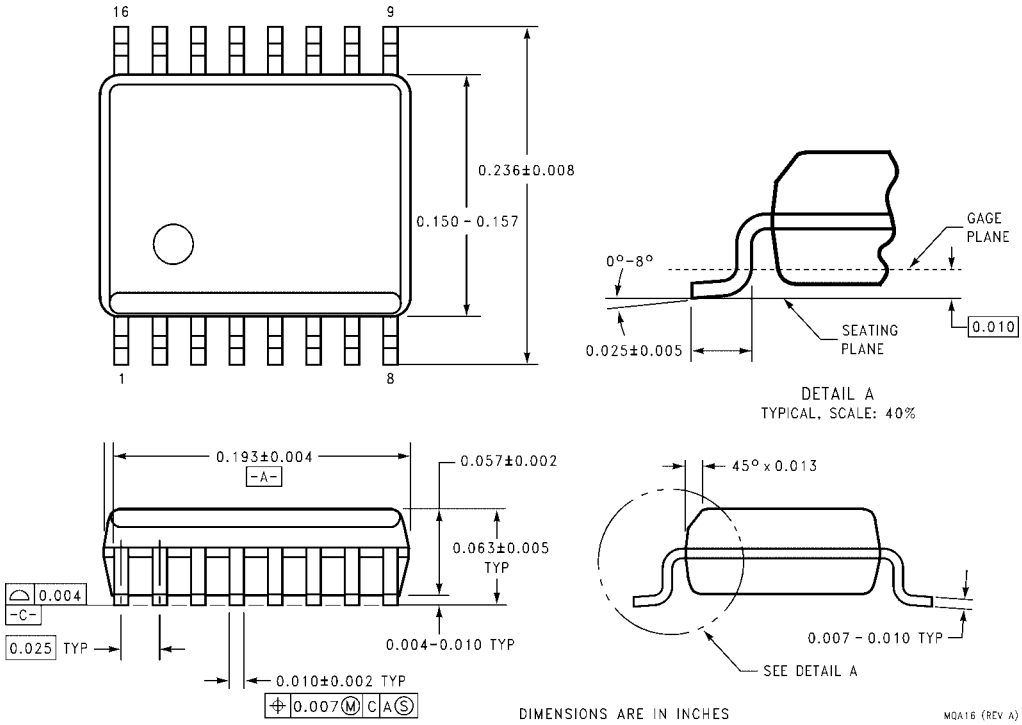


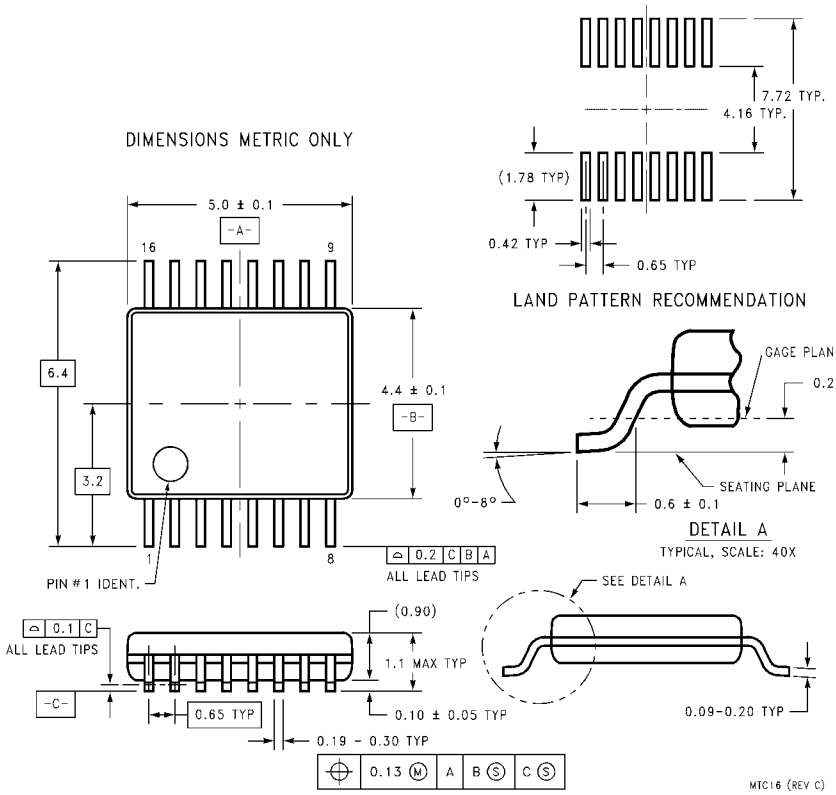
FIGURE 3. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
Package Number MQA16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

May 1999
Revised December 1999

FSTU3384
10-Bit Bus Switch with –2V Undershoot Hardened Circuit (UHC™) Protection

General Description

The Fairchild Switch FSTU3384 provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay generating additional ground bounce noise. Both the A Ports and the B Ports are "undershoot hardened" with UHC™ protection to support an extended input range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit, UHC senses undershoot at the I/Os, and responds by preventing voltage differentials from developing and turning on the switch. The device is organized as two 5-bit switches with separate bus enable ($\overline{OE}$) signals. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

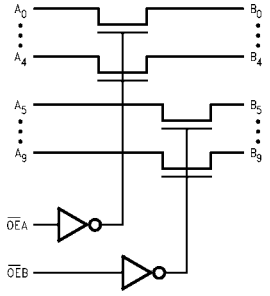
- 4Ω switch connection between two ports
- Undershoot Hardened to -2.0V.
- Minimal propagation delay through the switch
- Low I_{CC}.
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- See Applications Note AN-5008 for details.

Ordering Code:

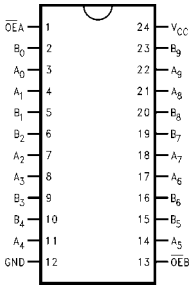
Order Number	Package Number	Package Description
FSTU3384WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MO-153 4.4mm Wide
FSTU3384QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
FSTU3384MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}A$, $\overline{OE}B$	Bus Switch Enable
A_0–A_9	Bus A
B_0–B_9	Bus B

Truth Table

$\overline{OE}A$	$\overline{OE}B$	B_0–B_4	B_5–B_9	Function
L	L	A_0–A_4	A_5–A_9	Connect
L	H	A_0–A_4	HIGH-Z State	Connect
H	L	HIGH-Z State	A_5–A_9	Connect
H	H	HIGH-Z State	HIGH-Z State	Disconnect

UHC™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−2.0V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50 mA
DC Output (I_{OUT}) Sink Current	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C			Units	Condition
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = − 18 mA
V_{IH}	HIGH Level Input Voltage	4.0-5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0-5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, B ≤ V_{CC}, V_{IN} = V_{IH}
R_{ON}	Switch On Resistance (Note 4)	4.5		4	7	Ω	V_S = 0V, I_{IN} = 64 mA
		4.5		4	7	Ω	V_S = 0V, I_{IN} = 30 mA
		4.5		8	15	Ω	V_S = 2.4V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_S = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_S = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	$\overline{OE}$ input at 3.4V Other inputs at V_{CC} or GND
I_{BIAS}	Bias Pin Leakage Current	5.5			±1.0	µA	$\overline{OE}$ = 0V, B = 0V, BiasV = 5.5V
I_{OZU}	Switch Undershoot Current	5.5			100	µA	I_{IN}= − 20 mA, $\overline{OE}$ = 5.5V, V_{OUT} ≥ V_{IH}
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA ≥ I_{IN} ≥ − 50 mA, $\overline{OE}$ = 5.5V

Note 4: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: All typical values are at V_{CC} = 5.0V, T_A = 25°C.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, RU = RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1, Figure 2
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}_A$, $\overline{OE}_B$ to A_n, B_n	1.0	5.7		6.2	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figure 1, Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}_A$, $\overline{OE}_B$ to A_n, B_n	1.5	5.2		5.5	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figure 1, Figure 2

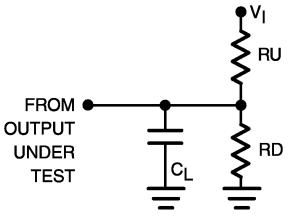
Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$ (OFF)	Input/Output Capacitance	5		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω, RU = RD = 500 Ω

Note: C_L includes load and stray capacitance, C_L = 50 pF

Note: Input PRR = 1.0 MHz, t_W = 500 nS

FIGURE 1. AC Test Circuit

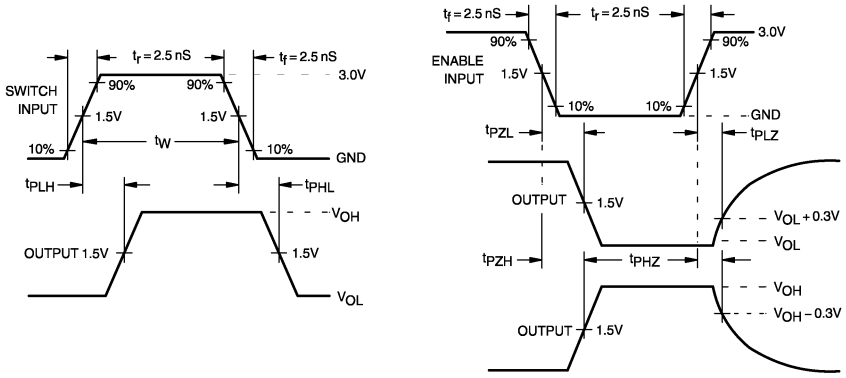
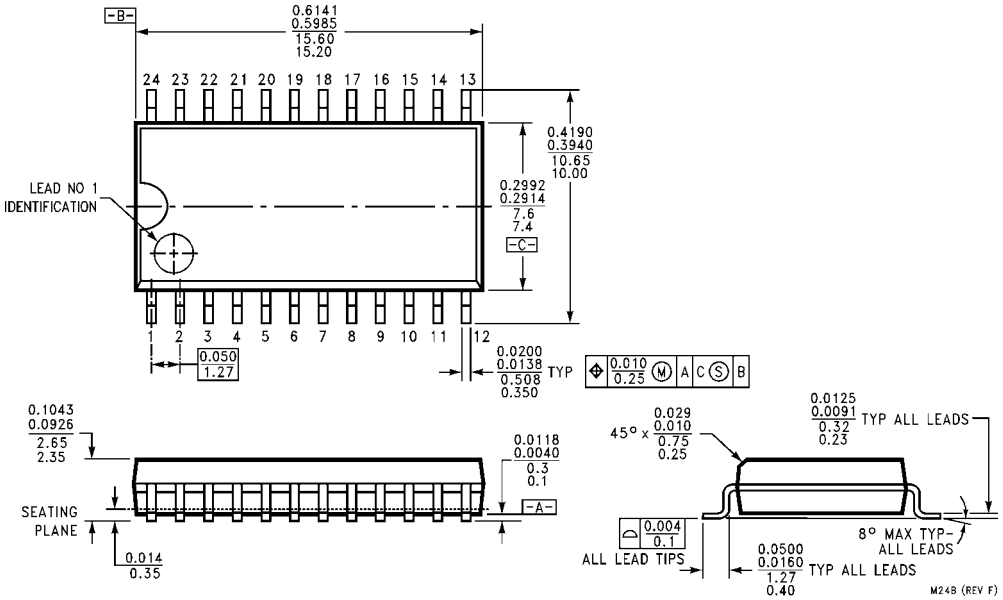
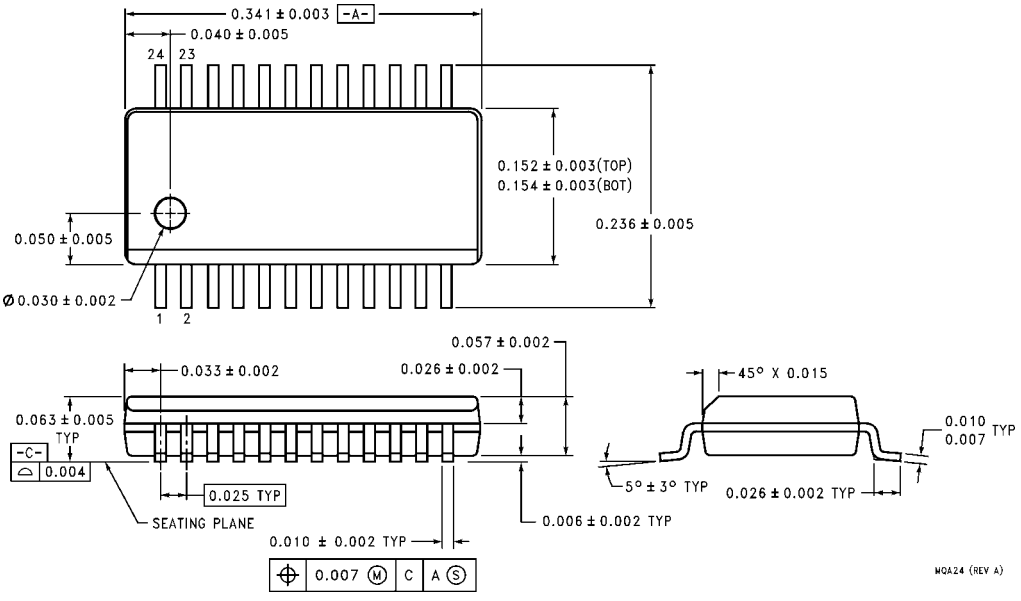


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

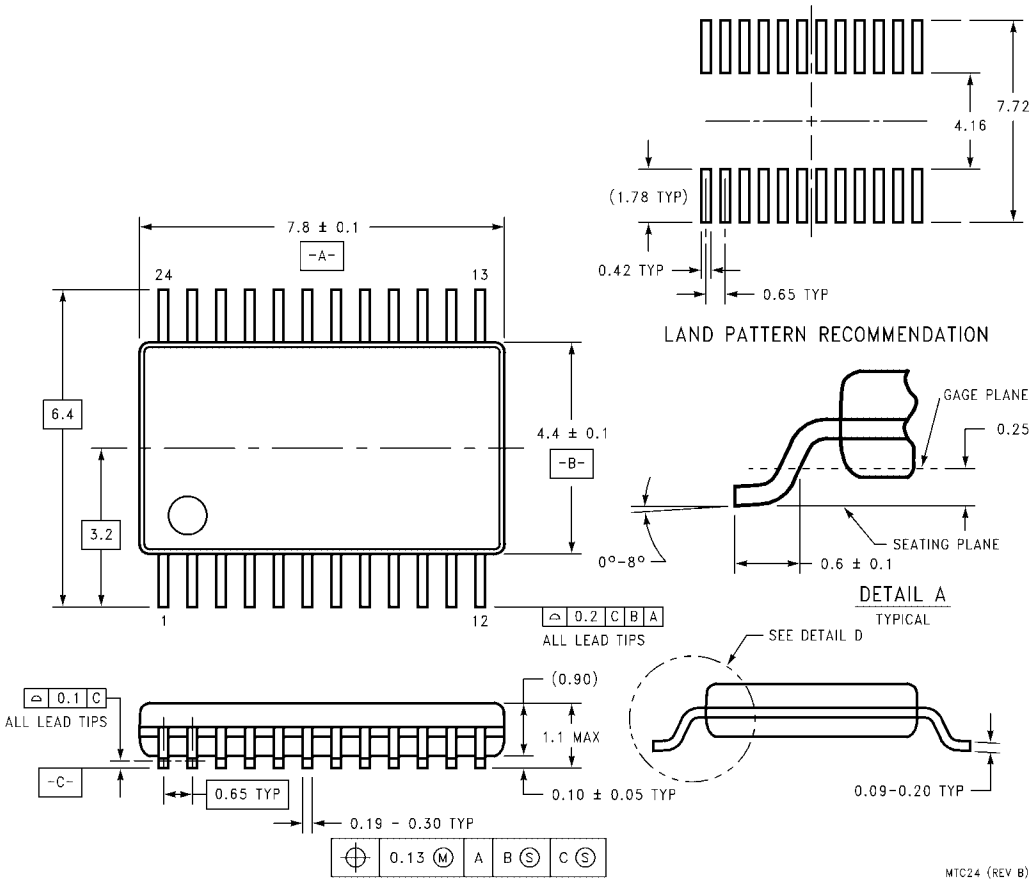


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MO-153 4.4mm Wide
Package Number M24B



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

December 1998
Revised December 1999

FSTU6800

10-Bit Bus Switch with Pre-Charged Outputs and −2V Undershoot Hardened Circuit (UHC™) Protection

General Description

The Fairchild Switch FSTU6800 provides 10-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. Both the A Ports and the B Ports are "undershoot hardened" with UHC™ protection to support an extended input range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit, UHC senses undershoot at the I/Os, and responds by preventing voltage differentials from developing and turning on the switch. The device also precharges the B Port to a selectable bias voltage (BiasV) to minimize live insertion noise.

The device is organized as a 10-bit switch with a bus enable ($\overline{OE}$) signal. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and the B Port is precharged to BiasV through an equivalent 10-kΩ resistor.

Features

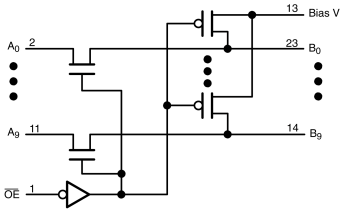
- 4Ω switch connection between two ports.
- Undershoot Hardened to -2.0V.
- Soft enable turn-on to minimize bus-to-bus charge sharing during enable.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Output precharge to minimize live insertion noise.
- Control inputs compatible with TTL level.
- See Applications Note AN-5008 for details.

Ordering Code:

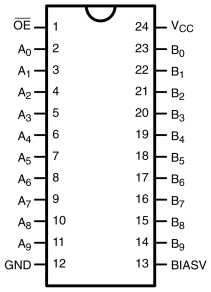
Order Number	Package Number	Package Description
FSTU6800WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MO-153 4.4mm Wide
FSTU6800QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
FSTU6800MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
A	Bus A
B	Bus B
BiasV	Bus B Voltage Bias

Truth Table

$\overline{OE}$	B_0–B_9	Function
L	A_0–A_9	Connect
H	BiasV	Precharge

UHC™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Switch Voltage (V_S)	–2.0V to +7.0V
Bias V Voltage Range	–0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	–0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}< 0V	–50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/– 100mA
Storage Temperature Range (T_{STG})	–65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Precharge Supply (BiasV)	1.5V to V_{CC}
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0 nS/V to 5 nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	–40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = –40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			–1.2	V	I_{IN} = –18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
I_O	Output Current	4.5	0.25			mA	BiasV = 2.4V, B = 0
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A ≤ V_{CC}, V_{IN} = V_{IH}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_S = 0V, I_{IN} = 64 mA
	(Note 4)	4.5		4	7	Ω	V_S = 0V, I_{IN} = 30 mA
		4.5		8	15	Ω	V_S = 2.4V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_S = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_S = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	$\overline{OE}$ input at 3.4V Other inputs at V_{CC} or GND
I_{BIAS}	Bias Pin Leakage Current	5.5			±1.0	µA	$\overline{OE}$ = 0V, B = 0V, BiasV = 5.5V
I_{OZU}	Switch Undershoot Current	5.5			100	µA	I_{IN} = –20 mA, $\overline{OE}$ = 5.5V, V_{OUT} ≥ V_{IH}
V_{IKU}	Voltage Undershoot	5.5			–2.0	V	0.0 mA ≥ I_{IN} ≥ –50 mA, $\overline{OE}$ = 5.5V

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: Typical values are at V_{CC} = 5.0V and T_A= +25°C

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,^{\circ}C$ to $+85\,^{\circ}C$, $C_L = 50$ pF, RU = RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL},t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}	Output Enable Time	7.0	30.0		35.0	ns	V_I = OPEN BiasV = GND	Figure 1 Figure 2
t_{PZL}		7.0	30.0		35.0	ns	V_I = 7V BiasV = 3V	
t_{PHZ}	Output Disable Time	1.0	6.1		6.5	ns	V_I = OPEN BiasV = GND	Figure 1 Figure 2
t_{PLZ}		1.0	7.3		6.8	ns	V_I = 7V BiasV = 3V	

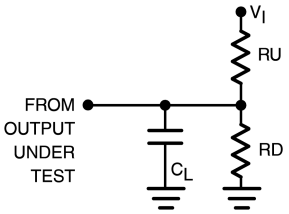
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	5		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω, RU = RD = 500 Ω

Note: C_L includes load and stray capacitance, C_L = 50 pF

Note: Input PRR = 1.0 MHz, t_W = 500 nS

FIGURE 1. AC Test Circuit

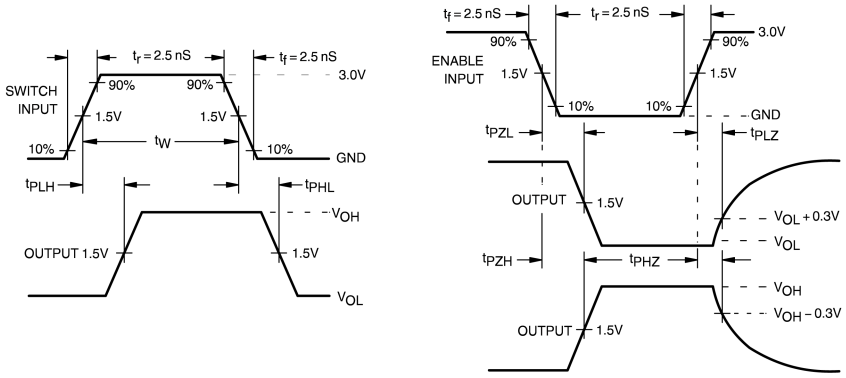
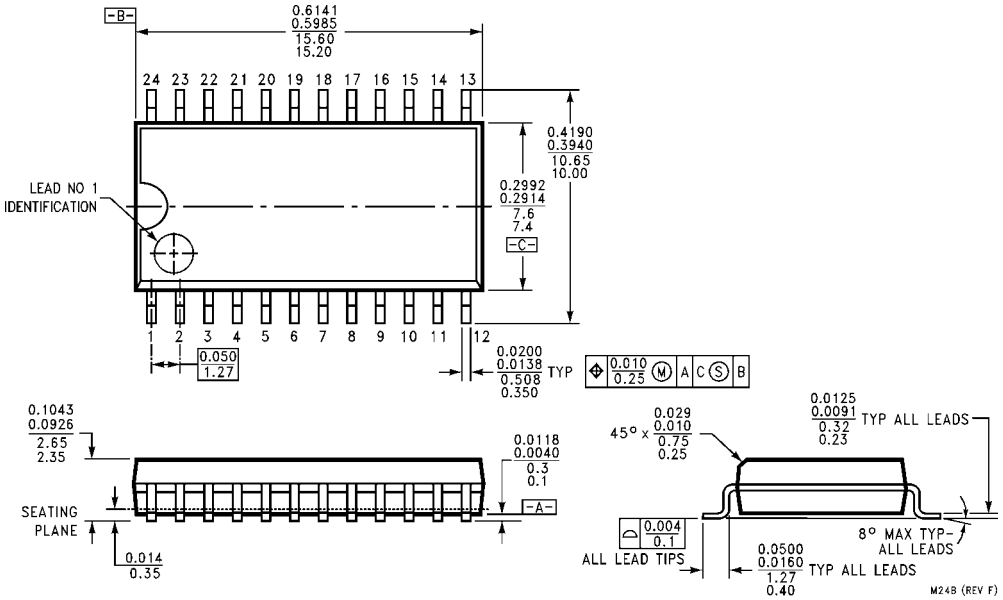
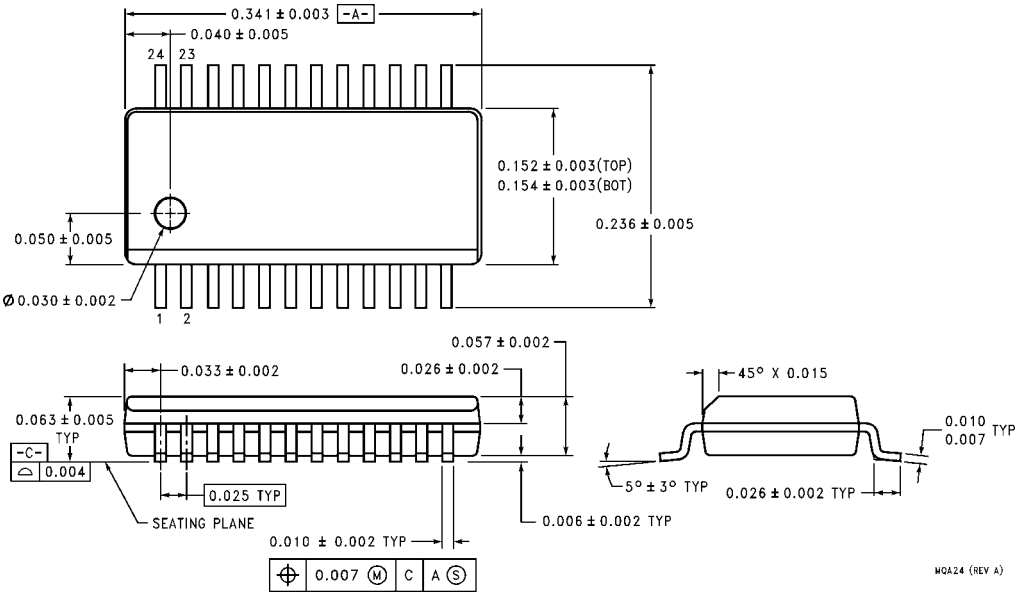


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

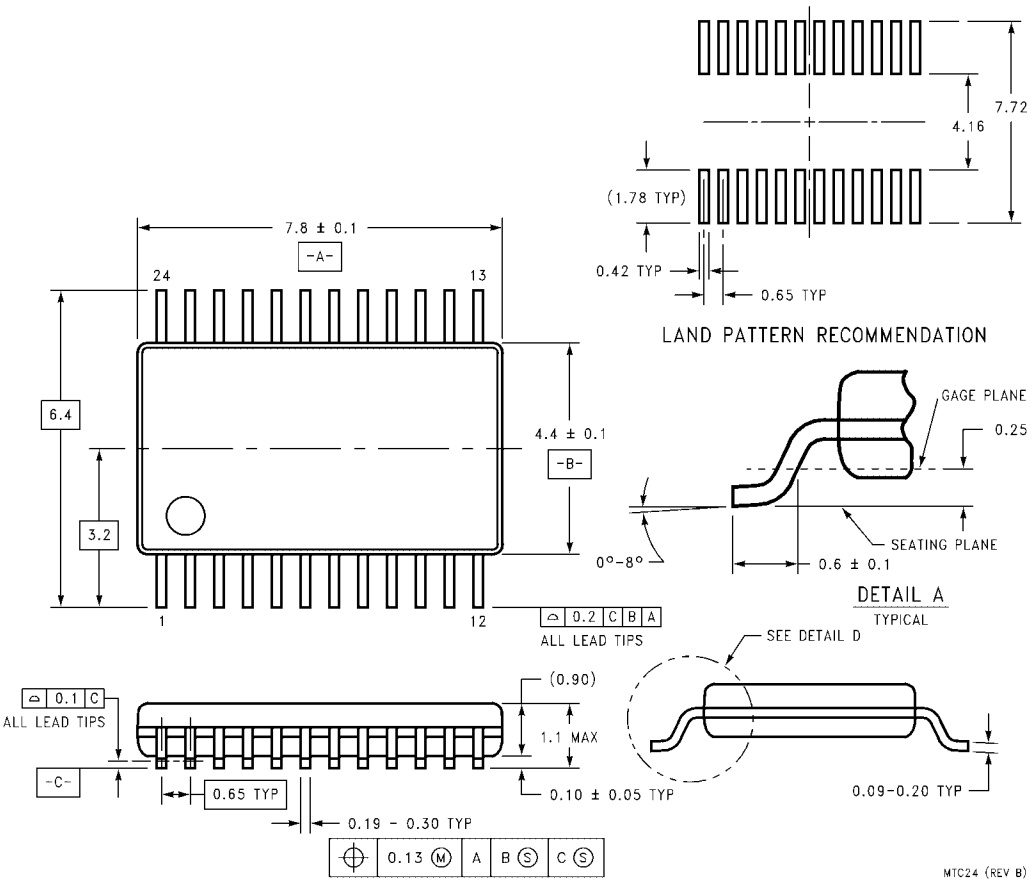


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MO-153 4.4mm Wide
Package Number M24B



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

FAIRCHILD SEMICONDUCTOR™

December 1998
Revised December 1999

FSTU6800A
10-Bit Bus Switch with Pre-Charged Outputs and −2V Undershoot Hardened Circuit (UHC™) Protection (Preliminary)

General Description

The Fairchild Switch FSTU6800A provides 10-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. Both the A Ports and the B Ports are "undershoot hardened" with UHC™ protection to support an extended input range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit, UHC senses undershoot at the I/Os, and responds by preventing voltage differentials from developing and turning on the switch. The device also precharges the B Port to a selectable bias voltage (BiasV) to minimize live insertion noise.

The device is organized as a 10-bit switch with a bus enable ($\overline{OE}$) signal. When $\overline{OE}$ is LOW, the switch is ON and Port A is connected to Port B. When $\overline{OE}$ is HIGH, the switch is OPEN and the B Port is precharged to BiasV through an equivalent 10-kΩ resistor.

Features

- 4Ω switch connection between two ports.
- Undershoot Hardened to -2.0V.
- Soft enable turn-on to minimize bus-to-bus charge sharing during enable.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Output precharge to minimize live insertion noise.
- Control inputs compatible with TTL level.
- See Applications Note AN-5008 for details.

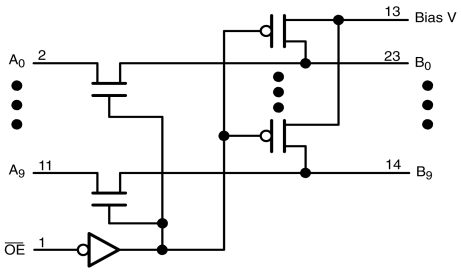
Ordering Code:

Order Number	Package Number	Package Description
FSTU6800AWM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MO-153 4.4mm Wide
FSTU6800AQSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
FSTU6800AMTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

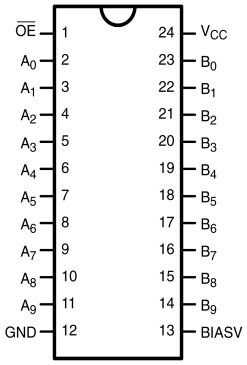
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

UHC™ is a trademark of Fairchild Semiconductor Corporation.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
A	Bus A
B	Bus B
BiasV	Bus B Voltage Bias

Truth Table

$\overline{OE}$	B_0–B_9	Function
L	A_0–A_9	Connect
H	BiasV	Precharge

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−2.0V to +7.0V
Bias V Voltage Range	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}< 0V	−50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Precharge Supply (BiasV)	1.5V to V_{CC}
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0 nS/V to 5 nS/V
Switch I/O	0 nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18 mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
I_O	Output Current	4.5	0.25			mA	BiasV = 2.4V, B = 0
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A ≤ V_{CC}, V_{IN} = V_{IH}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_S = 0V, I_{IN} = 64 mA
	(Note 4)	4.5		4	7	Ω	V_S = 0V, I_{IN} = 30 mA
		4.5		8	15	Ω	V_S = 2.4V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_S = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_S = V_{CC} or GND, I_{OUT} = 0
Δ I_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	$\overline{OE}$ input at 3.4V Other inputs at V_{CC} or GND
I_{BIAS}	Bias Pin Leakage Current	5.5			±1.0	µA	$\overline{OE}$ = 0V, B = 0V, BiasV = 5.5V
I_{OZU}	Switch Undershoot Current	5.5			100	µA	I_{IN} = −20 mA, $\overline{OE}$ = 5.5V, V_{OUT} ≥ V_{IH}
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA ≥ I_{IN} ≥ −50 mA, $\overline{OE}$ = 5.5V

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: Typical values are at V_{CC} = 5.0V and T_A= +25°C

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		Min	Max	Min	Max			
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Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 7)

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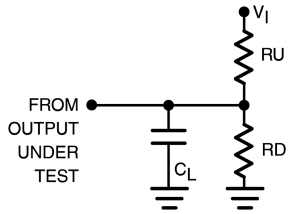
Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω, RU = RD = 500 Ω

Note: C_L includes load and stray capacitance, C_L= 50 pF

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

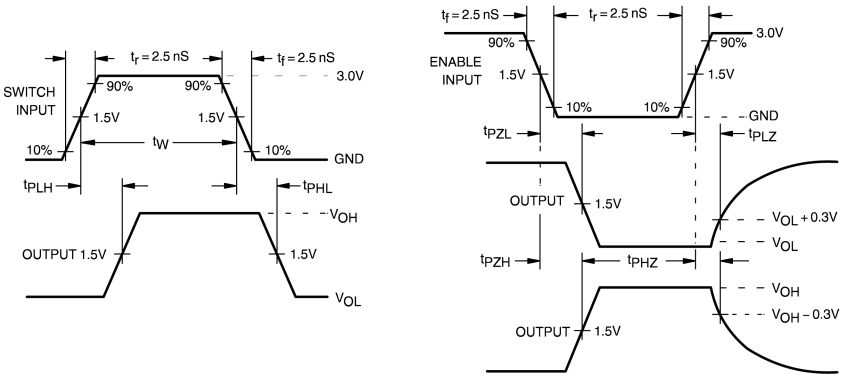
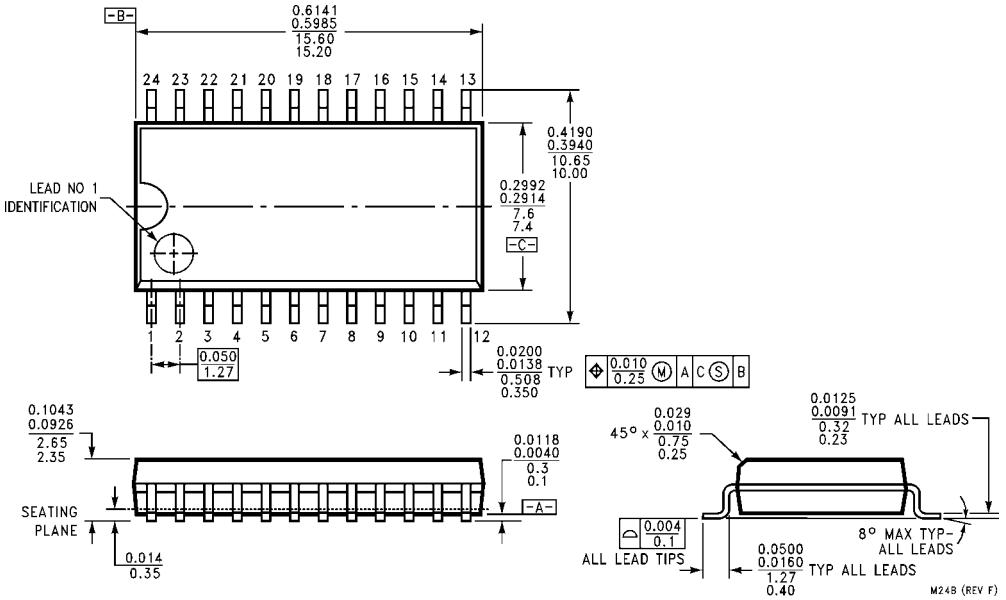
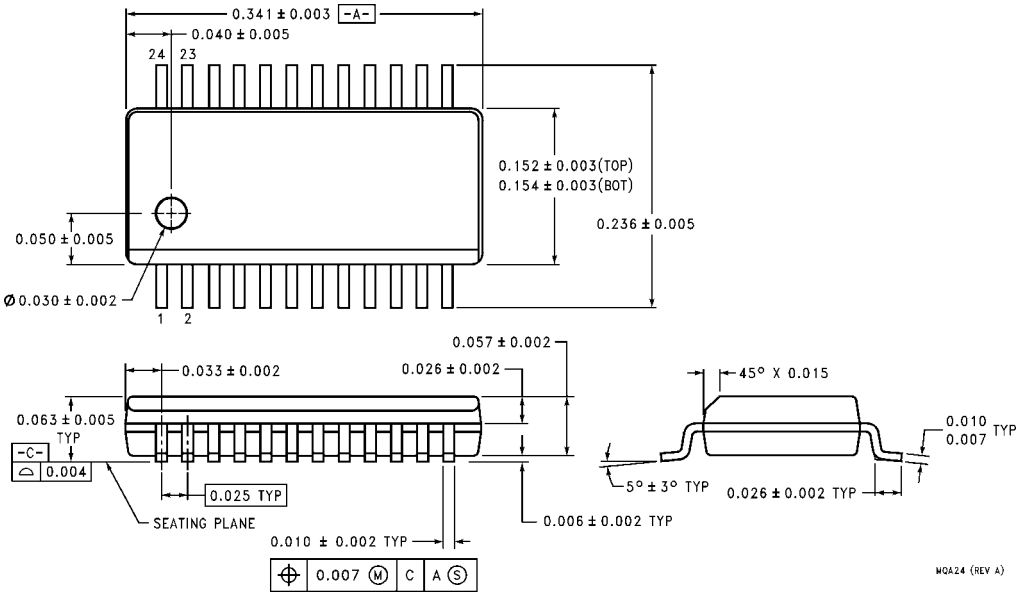


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

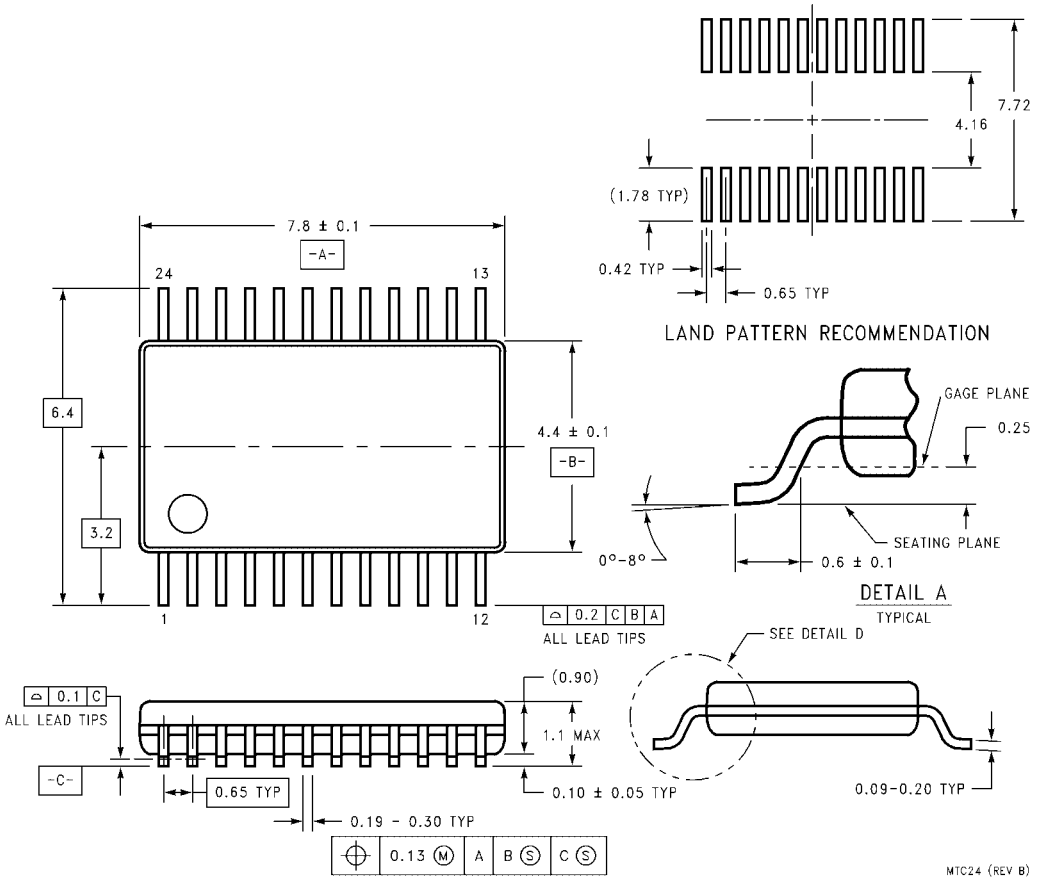


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MO-153 4.4mm Wide
Package Number M24B



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

Technology Description

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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