MX-COM, INC.

MX806A

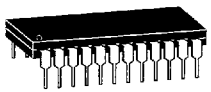
C-BUS COMPATIBLE

AUDIO PROCESSOR

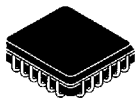
Description

The MX806A LMR audio processor is intended primarily to operate as the "Audio Terminal" of radio systems using the DBS 800 Digitally-integrated Baseband Subsystem.

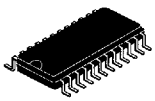
The MX806A half-duplex device has signal paths and level setting elements that are configured and adjusted by digital information sent from the radio microcontroller using C-BUS protocol. (C-BUS is the serial interface for all DBS 800 ICs.)



MX806AJ
24-pin CDIP



MX806ALH
24-lead PLCC



MX806ADW
24-pin SOIC

The signal path of the MX806A can be divided into three sections:

- **Input Process**
  This stage has selectable TX/RX paths. Transmit voice signals pass through microphone pre-amplifier, voltage controlled gain (VOGAD) and highpass filter stages. Received audio is de-emphasized. This initial audio, after in-line gain adjustment, may be switched to external audio processes (such as scrambling) or to the internal Main Process stages.
- **Main Process**
  Conditioning for the input or external process signals is completed in this stage. It is comprised of pre-emphasis, high and lowpass switched-capacitor filters and a deviation limiter.
- **Mixing and Output Drives**
  Main audio for transmission is mixed with signaling and data from external sources (other DBS 800 ICs) to provide the composite signal for the digitally adjustable transmitter modulation drives. Received audio level is adjusted for output to loudspeaker circuitry.

If selected, signal level stability and output accuracy of the MX806A is maintained by a voltage-controlled gain system using selectable signal-level detectors. Signal levels can be dynamically controlled to provide "dynamic compensation" for factors such as temperature drift, VCO non-linearity, etc.

MX806A audio output stages can be completely disabled - or the whole IC can be placed into powersave mode, leaving only clock and C-BUS circuitry active.

The MX806A is a low-power 5V CMOS integrated circuit. It is available in 24-pin CDIP and SMT packages.

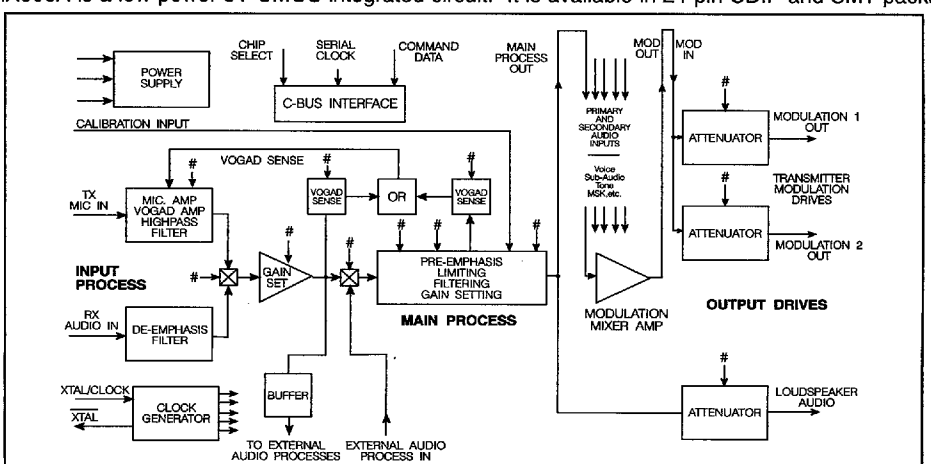


Figure 1 - MX806A Audio Processor

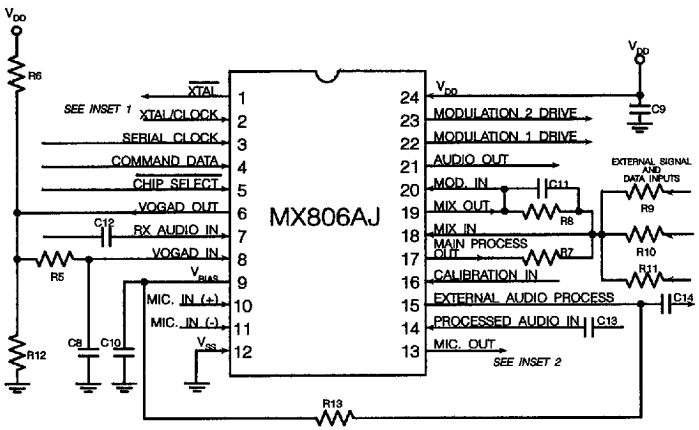
PIN FUNCTION CHART

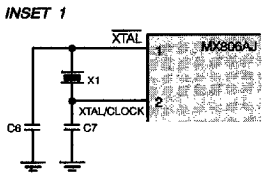
Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the 4.032 MHz on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	**Xtal/Clock:** The input to the on-chip 4.032 MHz clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock should be connected here. See Figure 2. This clock provides timing for on-chip elements, filters, etc.
3	**Serial Clock:** The "C-BUS" serial data loading clock input. This clock, produced by the microcontroller, is used for transfer timing of Command Data to the Audio Processor. See Timing diagrams.
4	**Command Data:** The "C-BUS" serial data input from the microcontroller. Command Data is loaded to this device in 8-bit bytes, MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. The Command/Data instruction is acted upon at the end of loading the whole instruction. Command information is detailed in Tables 1 - 5. See Timing diagrams.
5	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the microcontroller. Command Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams.
6	**VOGAD Out:** The error-voltage output of the selected VOGAD sensor. This output, with external attack and decay setting components, should be connected as in Figures 2 and 3, to the VOGAD In pin.
7	**RX Audio In:** The audio input to the MX806A from the radio receiver's demodulator circuits. This input, which requires a.c. coupling with capacitor C_{12}, is selected via a Control Command bit.
8	**VOGAD In:** The gain control signal from the selected VOGAD sensor (VOGAD Out) to the Input Process voltage-controlled amplifier. The required sensor is selected via a Mode Command. The choice of two sensors enables gain control from either the Input Process or an External Process. External attack and decay setting components should be applied as recommended in Figures 2 and 3.
9	**V_{BIAS}:** The output of the on-chip analog circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_{10}. See Figure 2.
10	**Mic In (+):** The non-inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2.
11	**Mic In (-):** The inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2.
12	**V_{SS}:** Negative supply (GND).

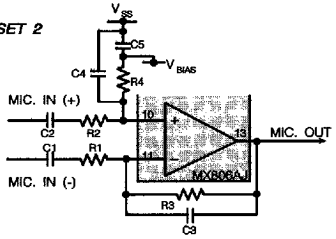
PIN FUNCTION CHART

Pin	Function
13	**Mic Out:** The output of the Microphone Op-Amp, used with the Mic In (-) input to provide the required gain/attenuation using external components as shown in Figure 2. The external components shown are to assist in the use of this amplifier with either inverting or non-inverting inputs. During Powersave (Volume Command) this output is placed at V_{SS}.
14	**Processed Audio In:** The input to the device from such external audio processes as Voice Store and Retrieve or Frequency Domain Scrambling. This input, which requires a.c. coupling with capacitor C_{13}, is selected by a Mode Command bit.
15	**External Audio Process:** The buffered output of the Input Processing Stage. Its purpose is to further external audio processing stages prior to re-introduction at the Processed Audio In pin.
16	**Calibration Input:** A unique audio input to be used for dynamic balancing of the modulator drives and for measuring Deviation Limiter levels. A CUE (beep) input from the MX803 Audio Tone Processor can be entered on this line. This audio input must be externally biased. It is selected via a Mode Command bit.
17	**Main Process Out:** The output of the Main Process stage. This output should be mixed with any additional system audio inputs (Audio, Sub-Audio Signaling, MSK) in the on-chip Modulation Summing Amplifier. External components shown in Figure 2 should be used as required.
18	**Sum In:** The input and output terminals of the on-chip Modulation Summing Amplifier. External components are required for input signals and gain/attenuation setting
19	**Sum Out:** as shown in Figure 2. For single-signal, no-gain requirements, Main Process Out may be linked directly to Modulation In.
20	**Modulation In:** The final, composite modulating signal to VCO (Mod 1) and Reference (Mod 2) Output Drives.
21	**Audio Output**: The processed audio signal output intended as a received audio (volume) output. Though normally used in the RX mode, operation in TX is permitted. The output level of this attenuator is controlled via a Volume Set command. During Powersave this output is placed at V_{SS}.
22	**Modulation 1 Drive:** The drive to the radio modulator Voltage Controlled Oscillator (VCO) from the composite audio summing stage.
23	**Modulation 2 Drive:** The drive to the radio modulator Reference Oscillator from the composite audio summing stage. NOTE: These VCO output attenuators are individually adjustable using the Modulator Level command. During Powersave these outputs are placed at V_{SS}.
24	V_{DD}: Positive supply. A single, stable +5 volt supply is required. Levels and voltages within this Audio Processor are dependent upon this supply.

Analog Application Information







Component	Value	Component	Value	Component	Value
R_1	10kΩ	R_{10}	100kΩ	C_6	33pF
R_2	10kΩ	R_{11}	100kΩ	C_7	5-65pF
R_3	20kΩ	R_{12}	2.2MΩ	C_8	1.0µF
R_4	20kΩ	R_{13}	470kΩ	C_9	1.0µF
R_5	10kΩ	C_1	.47µF	C_{10}	1.0µF
R_6	2.2MΩ	C_2	.47µF	C_{11}	22pF
R_7	100kΩ	C_3	270pF	C_{12}	0.1µF
R_8	100kΩ	C_4	270pF	C_{13}	0.01µF
R_9	100kΩ	C_5	0.1µF	C_{14}	0.01µF
				X_1	4.0MHz

Figure 2 - Recommended External Components

Tolerance: R=±10%. C=±20%.

Notes:

Input Op-Amp gain/attenuation components (voltage gain = 6.0dB) are shown in Inset 1 in a differential configuration to demonstrate the versatility of this input. Components for a single (+ or -) input may be used.

Resistor values R_7 to R_{11} (summation components) are dependent upon application and configuration requirements.

Xtal circuit capacitors C_6 (C_D) and C_7 (C_G) shown in Inset 2 are recommended in accordance with MX-COM's Crystal Oscillator Application Note, March 1990. Circuit drive and drain resistors are incorporated on-chip. Operation of any MX-COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, you should install a current limiting device (resistor or fast-reaction fuse) on the power input (V_{DD}).

Analog Application Information

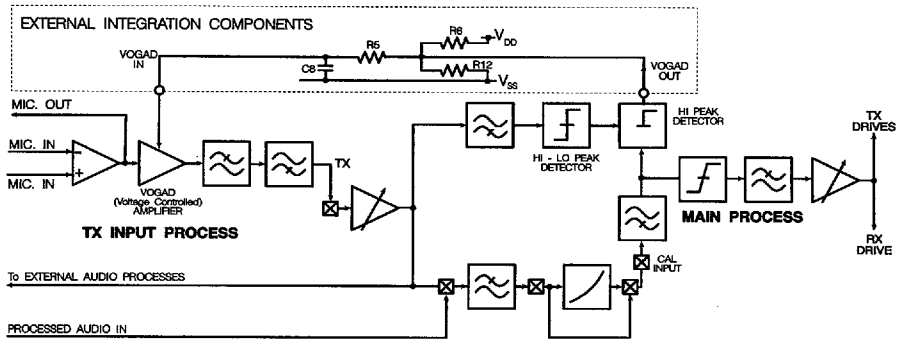


Figure 3 - VOGAD Sensors and Timing Components (from Fig. 5)

The overall Gain Control system of the MX806A consists of 2 selectable signal peak detectors whose output is fed via external integrating components to adjust the gain of the Voltage Controlled Amplifier positioned in the TX Input Process Path. The transmit input signal is presented to Peak Detector 1 or 2. The Peak Detectors are enabled individually by a Mode command. When the input signal exceeds the peak-to-peak threshold of the detector, a 5 volt level is produced at the VOGAD Out pin. This level remains for as long as the signal exceeds the threshold.

The integrated level to the VOGAD In pin causes the Voltage Controlled Amplifier gain to be reduced. As can be seen from Figures 3 and 5, Peak Detector 1 allows control of the audio level to the external audio process and Peak Dector 2 allows control of transmit deviation levels.

VOGAD attack and decay times are set using the external components shown in Figures 2 and 3. They are calculated as described below.

4

VOGAD Components Calculations - Figures 2 and 5

Provided $R_5 >> 1.0k\Omega$ and $R_6 = R_{12} >> R_5$

Then

$$\text{Attack Time } (T_A) = R_5 \times C_8$$

$$\text{Decay Time } (T_D) = \frac{R_6 \times C_8}{2}$$

Suggested Calibration Methods

To effectively null all internal IC tolerances, the following initial calibration routine is suggested:

TX Calibration: From Mic. In to Modulator Drives Out
Disable Peak Detectors (Mode Command).
Set Transmitter Drives to 0dB (Mod. Levels Set).
Pre-emphasis may be employed as required (Control Command).
Set Input Level Amp to 0dB (Control Command).

1) Mic. In = 250 mVrms at 1kHz. Set Process Gain Amp for output of 1440 mV p-p (100% deviation).
2) With Process Gain Amp set as 1 and with Mic. In = 25 mVrms at 1 kHz, set the Input Level Amp for an output level of 308 mVrms (60% deviation).

RX Calibration: From RX Audio In to Audio Out
Set Audio Output Drive to 0dB (Volume Set)
Leave Process Gain Amp set as 1 (see above).
3) With an RX Audio In level of between 154 mVrms and 308 mVrms (see Specifications) at 1 kHz, set the Input Level Amp for an output level of 308 mVrms.

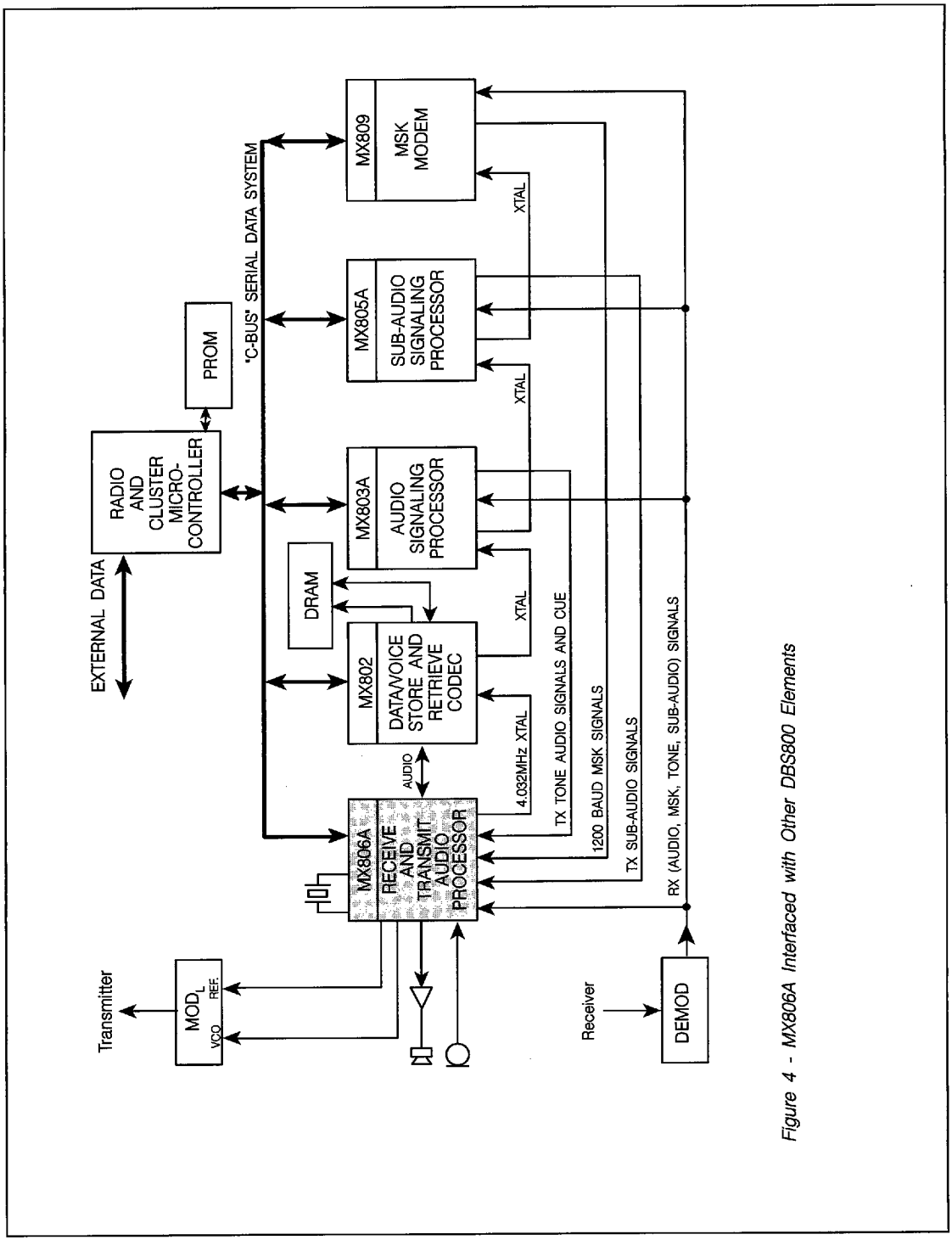


Figure 4 - MX806A Interfaced with Other DBS800 Elements

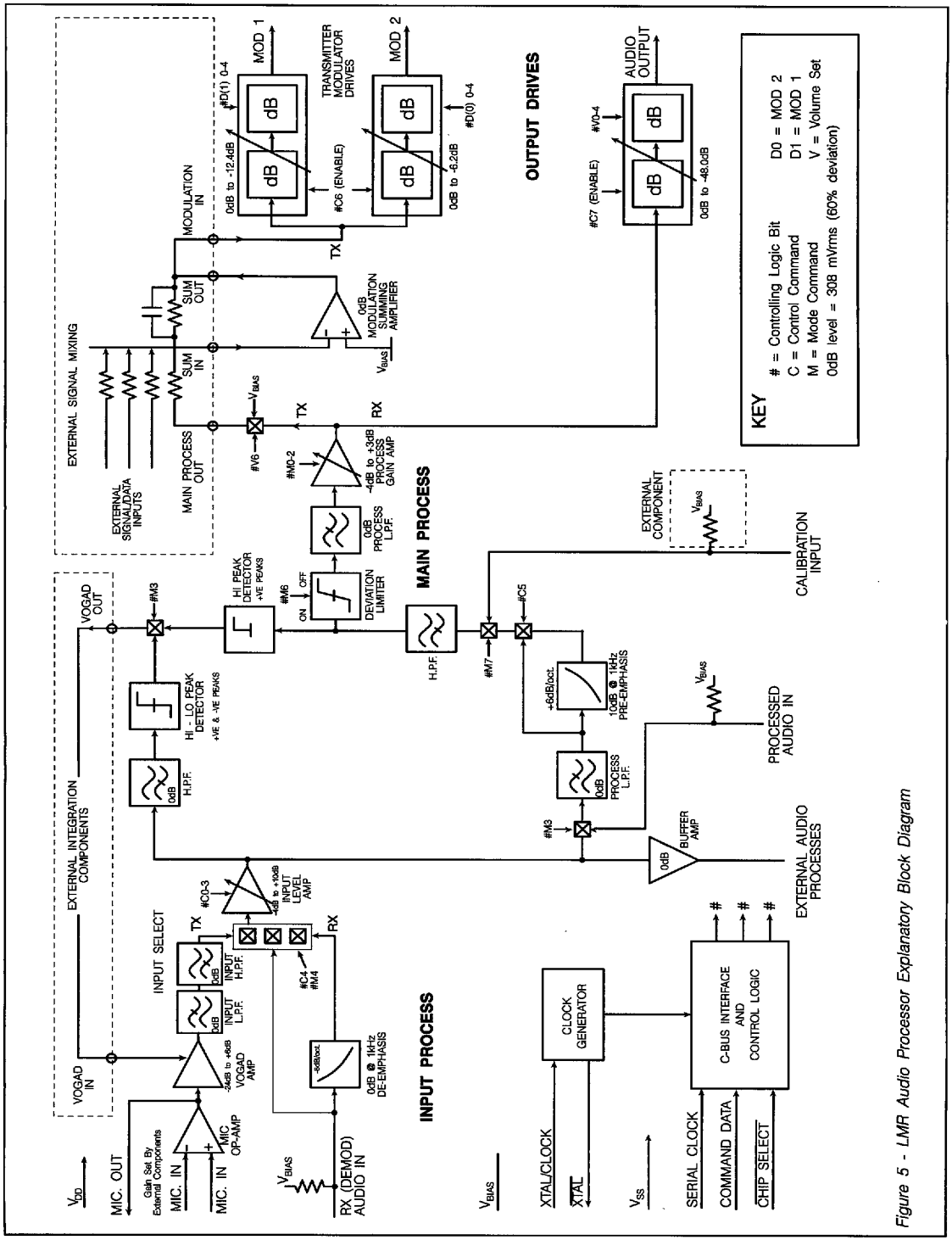


Figure 5 - LMR Audio Processor Explanatory Block Diagram

Controlling Protocol

Control of the functions and levels within the MX806A LMR Audio Processor is by a group of Address/Commands and appended data instructions from the system microcontroller. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Hex.	Address/Command Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Control Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
Mode Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
Mod. Levels Set	12	0 0 0 1 0 0 1 0	+	2 bytes	4
Volume Set	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 - C-BUS Address/Commands

In "C-BUS" protocol the MX806A is allocated Address/Command values 10_H to 13_H. C-BUS Command, Mode, Modulation and Volume assignments and data requirements are given in Table 1 and illustrated in Figure 5.

Commands and Data are only to be loaded in the group configurations detailed since the "C-BUS" interface recognizes the first byte after Chip Select (logic"0") as an Address/Command.

Function or Level control data, which is detailed in Tables 2, 3, 4, and 5, is acted upon at the end of the loaded instruction.

Upon power-up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command (01_H) is required. This command is provided to "reset" all devices on the Command Data line and has the following effect on the MX806A:

Control Address Command	Loaded as 00_H
Mode Address Command	Loaded as 00_H
Volume Set	Loaded as 00_H

Control Command *(Preceded by A/C 10_H)*

Setting	Control Bits
(MSB) Bit 7	**Audio Output (RX)**
0	Disabled
1	Enabled
6	**Modulation Drives**
0	Disabled
1	Enabled
5	**Pre-Emphasis**
0	Bypass
1	Enabled
4	**Input Select**
0	RX In
1	Mic. In
3 2 1 0	**Input Level Set**
0 0 0 0	Input Amp Disabled
0 0 0 1	-4.0dB
0 0 1 0	-3.0dB
0 0 1 1	-2.0dB
0 1 0 0	-1.0dB
0 1 0 1	0dB
0 1 1 0	1.0dB
0 1 1 1	2.0dB
1 0 0 0	3.0dB
1 0 0 1	4.0dB
1 0 1 0	5.0dB
1 0 1 1	6.0dB
1 1 0 0	7.0dB
1 1 0 1	8.0dB
1 1 1 0	9.0dB
1 1 1 1	10.0dB

Table 2 - Control Commands

Mode Command *(Preceded by A/C 11_H)*

Setting	Mode Bits
(MSB) Bit 7	**Drive Source**
0	Signals
1	Calibration
6	**Deviation Limiter**
0	Disabled
1	Enabled
5	**VOGAD**
0	Disabled
1	Enabled
4	**De-Emphasis**
0	Enabled
1	Bypassed
3	**Signal Select**
0	Internal
1	External
2 1 0	**Process Gain Set**
0 0 0	-4.0dB
0 0 1	-3.0dB
0 1 0	-2.0dB
0 1 1	-1.0dB
1 0 0	0dB
1 0 1	1.0dB
1 1 0	2.0dB
1 1 1	3.0dB

Table 3 - Mode Commands

Modulator Levels *(Preceded by A/C 12_H)*

Setting	Modulator Drives
Byte 1 (MSB)	***First byte for transmission***
7 6 5	
0 0 0	Must be "0"
4 3 2 1 0	**VCO Drive Attenuation**
0 0 0 0 0	12.4dB
0 0 0 0 1	12.0dB
0 0 0 1 0	11.6dB
0 0 0 1 1	11.2dB
0 0 1 0 0	10.8dB
0 0 1 0 1	10.4dB
0 0 1 1 0	10.0dB
0 0 1 1 1	9.6dB
0 1 0 0 0	9.2dB
0 1 0 0 1	8.8dB
0 1 0 1 0	8.4dB
0 1 0 1 1	8.0dB
0 1 1 0 0	7.6dB
0 1 1 0 1	7.2dB
0 1 1 1 0	6.8dB
0 1 1 1 1	6.4dB
1 0 0 0 0	6.0dB
1 0 0 0 1	5.6dB
1 0 0 1 0	5.2dB
1 0 0 1 1	4.8dB
1 0 1 0 0	4.4dB
1 0 1 0 1	4.0dB
1 0 1 1 0	3.6dB
1 0 1 1 1	3.2dB
1 1 0 0 0	2.8dB
1 1 0 0 1	2.4dB
1 1 0 1 0	2.0dB
1 1 0 1 1	1.6dB
1 1 1 0 0	1.2dB
1 1 1 0 1	0.8dB
1 1 1 1 0	0.4dB
1 1 1 1 1	0dB
Byte 0 (MSB)	***Last byte for transmission***
7 6 5	
0 0 0	Must be "0"
4 3 2 1 0	**VCO (Ref.) Drive Attenuation**
0 0 0 0 0	6.2dB
0 0 0 0 1	6.0dB
0 0 0 1 0	5.8dB
0 0 0 1 1	5.6dB
0 0 1 0 0	5.4dB
0 0 1 0 1	5.2dB
0 0 1 1 0	5.0dB
0 0 1 1 1	4.8dB
0 1 0 0 0	4.6dB
0 1 0 0 1	4.4dB
0 1 0 1 0	4.2dB
0 1 0 1 1	4.0dB
0 1 1 0 0	3.8dB
0 1 1 0 1	3.6dB
0 1 1 1 0	3.4dB
0 1 1 1 1	3.2dB
1 0 0 0 0	3.0dB
1 0 0 0 1	2.8dB
1 0 0 1 0	2.6dB
1 0 0 1 1	2.4dB
1 0 1 0 0	2.2dB
1 0 1 0 1	2.0dB
1 0 1 1 0	1.8dB
1 0 1 1 1	1.6dB
1 1 0 0 0	1.4dB
1 1 0 0 1	1.2dB
1 1 0 1 0	1.0dB
1 1 0 1 1	0.8dB
1 1 1 0 0	0.6dB
1 1 1 0 1	0.4dB
1 1 1 1 0	0.2dB
1 1 1 1 1	0dB

Table 4 - Modulator Drive Levels

Volume Set *(Preceded by A/C 13_H)*

Setting	Volume Set
(MSB)	
7 6	**Main Process Out**
0 0	Enabled
0 1	Biased
5	**Powersave**
0	Chip Enabled
1	Powersaved
4 3 2 1 0	**Volume Set Attenuation**
0 0 0 0 0	Off
0 0 0 0 1	48.0dB
0 0 0 1 0	46.4dB
0 0 0 1 1	44.8dB
0 0 1 0 0	43.2dB
0 0 1 0 1	41.6dB
0 0 1 1 0	40.0dB
0 0 1 1 1	38.4dB
0 1 0 0 0	36.8dB
0 1 0 0 1	35.2dB
0 1 0 1 0	33.6dB
0 1 0 1 1	32.0dB
0 1 1 0 0	30.4dB
0 1 1 0 1	28.8dB
0 1 1 1 0	27.2dB
0 1 1 1 1	25.6dB
1 0 0 0 0	24.0dB
1 0 0 0 1	22.4dB
1 0 0 1 0	20.8dB
1 0 0 1 1	19.2dB
1 0 1 0 0	17.6dB
1 0 1 0 1	16.0dB
1 0 1 1 0	14.4dB
1 0 1 1 1	12.8dB
1 1 0 0 0	11.2dB
1 1 0 0 1	9.6dB
1 1 0 1 0	8.0dB
1 1 0 1 1	6.4dB
1 1 1 0 0	4.8dB
1 1 1 0 1	3.2dB
1 1 1 1 0	1.6dB
1 1 1 1 1	0dB

Table 5 - Volume Set

Notes

Command Loading: Address/Commands and data bytes must be loaded in accordance with the information given in Figure 6.

The **Powersave** function is enabled by bit 5 of the Volume Set Command (Table 5).

During Powersave all internal elements except the Clock Generator and "C-BUS" interface are off. The Mic Op-Amp and Output Drive stage outputs are connected to V_{SS}.

Modulator Drives are controlled separately, but the whole two-byte Modulator Drive command must be loaded for each requirement adjustment.

$\overline{\text{Chip Select}}$ must be held at a logic "1" for the period "t_{CSOFF}" between transactions.

Timing Information

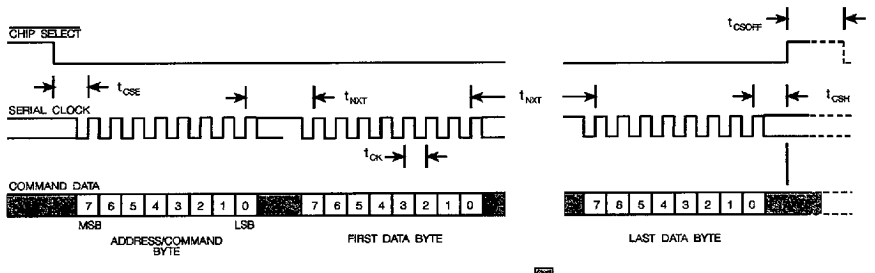


Figure 6 - C-BUS Timing Information

Parameter	Abbreviation	Min.	Typ.	Max.	Unit
"$\overline{CS}$ Enable" to "clock high"	t_{CSE}	2.0	-	-	µs
Last "clock high" to "CS high"	t_{CSH}	4.0	-	-	µs
"$\overline{CS}$ high" time between transactions	t_{CSOFF}	2.0	-	-	µs
Inter byte time	t_{NXT}	4.0	-	-	µs
Serial Clock Period	t_{CK}	2.0	-	-	µs

Notes
Command data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last.
Data is clocked into the peripheral on the rising clock edge.
Loaded data instructions are acted upon at the end of each individual, loaded byte.
To allow for different microcontroller serial interface formats, the MX806A is able to work with either polarity Serial Clock pulses.

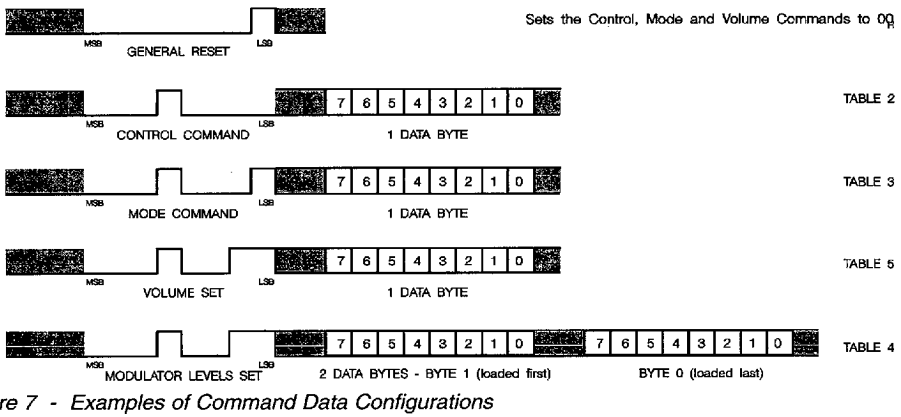


Figure 7 - Examples of Command Data Configurations

Application Information
To assist in rapid setting, this quick-reference list should be used with Figure 5.

Control	A/C = 10_H
7	Audio Out (RX) Enable
6	Modulator Drive Enable
5	Pre-Emphasis Select
4	Input Select (RX/TX)
3-0	Input Level Set (-4dB to 10dB)

Mode	A/C = 11_H
7	Drive Source
6	Deviation Limiter Enable
5	VOGAD Enable
4	De-Emphasis Enable
3	Signal Select
2-0	Process Gain Set (-4dB to 3dB)

Modulator Levels	A/C = 12_H
Byte1	
7-5	"0"
4-0	Mod 1 Attenuation (0 to 12.4dB)
Byte 2	
7-5	"0"
4-0	Mod 2 Attenuation (0 to 6.2dB)

Volume Set	A/C = 13_H
7-6	"0"
5	Powersave
4-0	Volume Set Attenuation (0 to 48dB)

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD}+0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.0MHz

Audio Level 0dB ref = 308mVrms @ 1kHz *(60% deviation, FM)*

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (All elements enabled)		-	8.0	15.0	mA
(Maximum Powersave)		-	.7	1.5	mA
"C-BUS" Interface					
Input Logic "1"	3.5	-	-	V	
Input Logic "0"	-	-	1.5	V	
Input Current		-1.0	-	1.0	µA
Input Capacitance		-	-	7.5	pF
Overall Performance					
Microphone Input Level	1,2		25		mVrms
Discriminator Input Level	2,3	154	-	308	mVrms
Output Drive Level					
(60% deviation)	2,4	291	308	326	mVrms
(100% deviation)	2,4,5	-	1440	-	mV pk-pk
Passband	6	297	-	3000	Hz
Passband Ripple	7	-2	-	0.5	dB
Stopband Attenuation	6,8				
@150Hz		10	12	-	dB
@3400Hz		-	2	-	dB
@6000Hz		30	36	-	dB
@8000 to 20,000 Hz		-	60	-	dB
Signal Path Noise TX		-	-50	-	dBp
	9	-	-45	-	dB
RX		-	-60	-	dB
	9	-	-55	-	dB
Total Harmonic Distortion (RX or TX, 60% deviation)		-	1.0	-	%
Circuit Elements - Figure 5					
Mic. Amp or Mod. Summation Amp					
Open Loop Gain		-	50.0	-	dB
Bandwidth		20.0	-	-	kHz
Input Impedance		10.0	-	-	MΩ
Output Impedance (Open Loop)		-	6.0	-	kΩ
(Closed Loop)		-	600	-	Ω
De-emphasis					
Slope		-	-6.0	-	dB/oct.
Gain (at 1.0kHz)		-	0	-	dB
Input Impedance		-	1	-	MΩ
Voltage Controlled Gain Amp (VOGAD)					
Gain (Non-Compressing)	2	-	6.0	-	dB
(Full Compression)		-	-24	-	dB

Characteristics	See Note	Min.	Typ.	Max.	Unit
Input Impedance		10.0	-	-	MΩ
VOGAD Peak Detectors					
Output Impedance Logic "1" (Compress)		-	1	-	kΩ
Logic "0"		-	10	-	MΩ
Hi/Lo Peak Detector Threshold	10	-	1,300	-	mV p-p
Hi Peak Detector Threshold	10	-	650	-	mV+ve pk
Input (Low + Highpass) Filter					
Gain (at 1.0 kHz)		-1.0	0	1.0	dB
Input Level Amp					
Gain Range		-	0	-	dB
Overall Tolerance		-1.0	-	1.0	dB
Step Size		0.75	1.0	1.25	dB
External Audio Buffer					
Gain		-0.1	0	0.1	dB
Pre-emphasis (Main Process and VOGAD)					
Slope		-	6.0	-	dB/oct.
Gain (at 1.0kHz)		-	10.0	-	dB
Process Highpass Filter					
Gain (at 1.0 kHz)		-0.1	0	0.1	dB
Deviation Limiter					
Threshold		708	1300	1413	mVrms
Gain		-0.5	-	0.5	dB
Process Lowpass Filter					
Gain (at 1.0 kHz)		-0.1	0	0.1	dB
Process Gain Amp					
Gain Range		-4.0	-	3.0	dB
Overall Tolerance		-0.5	-	0.5	dB
Step Size		0.75	1.0	1.25	dB
Output Impedance		-	600	-	Ω
Transmitter Modulator Drives					
Input Impedance		-	15.0	-	kΩ
Mod. 1 Attenuator					
Attenuation Range		0	-	12.4	dB
Overall Tolerance		-1	-	1	dB
Step Size		0.2	0.4	0.6	dB
Output Impedance		-	600	-	Ω
Mod. 2 Attenuator					
Attenuation Range		0	-	6.2	dB
Overall Tolerance		-0.5	-	0.5	dB
Step Size		0.1	0.2	0.3	dB
Output Impedance		-	600	-	Ω
Audio Output Attenuator					
Attenuation Range		0	-	48.0	dB
Overall Tolerance		-1.0	-	1.0	dB
Step Size		1.1	1.6	2.1	dB
Output Impedance		-	600	-	Ω
Miscellaneous Impedances					
Processed Audio Input		-	500	-	kΩ
Calibration Input		-	500	-	kΩ
External Process Out		-	100	-	Ω
RX with De-emphasis Bypass		-	25.0	-	kΩ

Notes

1. Producing an output of 0dB with the Mic. Op-Amp set to 6dB (as shown in Figure 2) and the Modulator Drives set to 0dB.
2. With Output Drives set to 0dB and the system calibrated as described in the Application Notes.
3. Input level range for 0dB output, by adjustment of the Input Level Amp.
4. It is recommended that these output levels will produce 60% or 100% deviation in the transmitter.
5. With the microphone input level 20dB above the level required to produce 0dB at the Output Drives.
6. Between Microphone or RX inputs to Modulator or Audio Outputs.
7. Deviation from the ideal overall response including the pre- or de-emphasis slope.
8. Excluding the effect of pre- or de-emphasis slope.
9. In a 30kHz bandwidth.
10. Using pre-emphasis in the TX path.