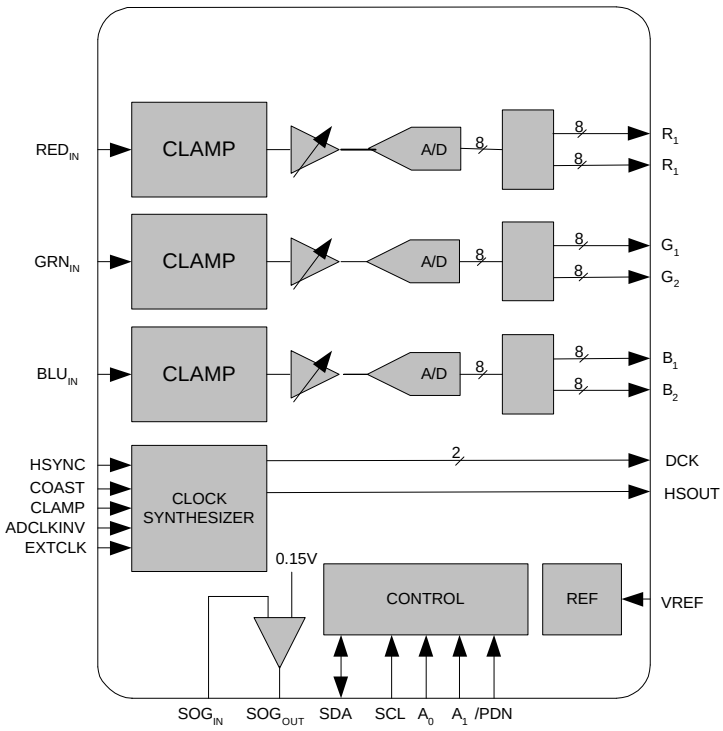
MX88L295EC
MX88L296EC
Data Sheet
Rev.1.0A

FEATURES OVERVIEW

- MX88L295EC support triple ADC with 20 - 110 MHz Sampling Rate
- MX88L296EC support triple ADC with 20 - 140 MHz Sampling Rate
- MX88L295EC and MX88L296EC are Fully Pin Compatible
- Integrated line locked PLL generates pixel clock from HSYNC
- Integrated 5-bit pixel clock phase adjustment for precise sample timing control
- Integrated clamp with timing generator
- Integrated Brightness & Contrast controls
- Integrated precision voltage reference
- Compatible with VGA thru SXGA RGB graphics signals
- Pin Compatible with AD9884A

BLOCK DIAGRAM



- Serial port programming interface

DESCRIPTION

Most flat-panel monitors and projectors require a digital graphics input in order to accurately scale and display graphics. The huge installed base of computers with analog video graphics interfaces necessitates the use of a graphics digitizer to re-digitize the analog RGB signal before further processing.

- The MX88L295EC/MX88L296EC are fully integrated analog interfaces for digitizing high-resolution RGB graphics signals from PC's and workstations. With a sampling rate capability of up to 110/140 MHz, it can accurately support display resolutions up to 1280x1024 (SXGA) at 60/75Hz. The clamped input circuits provide sufficient bandwidth to accurately digitize each pixel.
- The MX88L295EC/MX88L296EC provide a high performance highly integrated solution to support the digitization process, including the ADC's, a voltage reference, a PLL to generate the pixel sampling clock from HSYNC, clamping circuits, and programmable offset and gain circuits to provide brightness and contrast controls.
- When the COAST signal is asserted, the PLL will maintain its output frequency when HSYNC pulses are absent, such as during the VSYNC period in some systems.
- A 32-step programmable phase adjustment control (0-360 deg) is provided for the pixel sampling clock to adjust for the difference between the HSYNC edge and RGB pixel edge timing.
- The MX88L295ECMX88L296EC can send output data through one 24-bit port at the pixel clock rate, or through two 24-bit ports at ½ the pixel clock rate. The ½ pixel clock rate data can be sent fully parallel or using a staggered clock to improve ground bounce or system EMI.