CML Semiconductor Products

PRODUCT INFORMATION

FX009 Digitally Controlled Amplifier Array

T-74-05-01

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Provisional Issue

CONSUMER MICROCIRCUITS

Features/Applications

- 8 Digitally Controlled Amplifiers
- 15 Gain/Attenuation Steps
- 7 Trimmers, with a ± 3dB Range in 0.43dB Steps
- 1 'Volume' Trimmer, with a ± 14dB Range in 2.0dB Steps
- 8-Bit Serial Data Control
- Output Mute/Powersave Function
- Audio and Data Gain Control Applications
- Cellular, PMR, PABX Applications

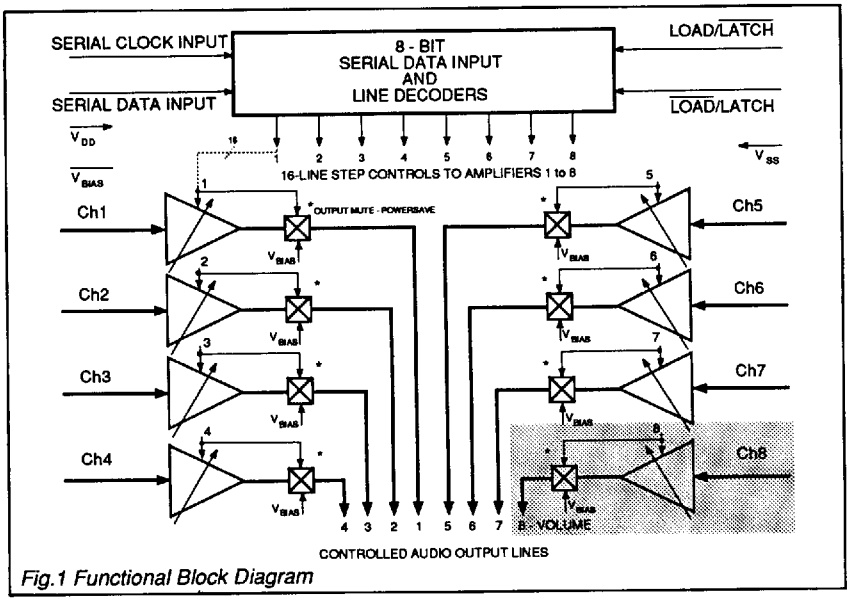

Fig.1 Functional Block Diagram

FX009

Brief Description

The FX009 Digitally Adjustable Amplifier Array is intended to replace trimmer potentiometers and volume controls in Cellular, PMR, Telephony and Communications applications where d.c., voice or data signals need adjustment.

The FX009 is a single-chip LSI consisting eight digitally controlled amplifier stages, each with 15 distinct gain/attenuation steps. Control of each individual amplifier is by an 8-bit serial data stream. Seven of the amplifier stages offer a +/-3dB range in steps of 0.43dB, whilst the remaining amplifier offers a +/-14dB range in steps of 2dB, and is intended for volume control applications. Each amplifier includes a 16th 'Mute' state which sets the output to bias ($V_{DD}/2$) and powersaves the entire section. Minimum current drain may be achieved by muting all eight sections.

This product replaces the need for manual trimming of audible signals by using the host microprocessor to digitally control the set-up of all audio levels.

Applications Include:

(i) Control, adjustment and set-up of communications equipment by an Intelligent ATE without manual intervention – eg. Deviation, Microphone and L/S Level, Rx Audio Level etc.

(ii) Automatic Dynamic Compensation of drift caused by variations in temperature, linearity, etc.

(iii) Fully automated servicing and re-alignment.

The FX009 is a low-power, single 5-volt CMOS device available in both 24-pin DIL and SMD package versions.

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Pin Number DIL FX009J	Pin Number Quad FX009LG/LS	Function
1	1	**Serial Clock :** This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Data Load Timing. This input has an internal 1MΩ pullup resistor.
2	2	**Load/$\overline{\text{Latch}}$:** Governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '0' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '0' ⇒ '1' ⇒ '0' to latch the new data in. Data is executed on the falling edge of the strobe. If the Load/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pullup resistor.
3	3	**$\overline{\text{Load}}$/$\overline{\text{Latch}}$:** The inverted Load/$\overline{\text{Latch}}$ input. This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '1' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '1' ⇒ '0' ⇒ '1' to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/$\overline{\text{Latch}}$ input is used this pin should be left open circuit. This input has an internal 1MΩ pulldown resistor.
4	4	**Ch1 Input :** **Analogue Inputs :**
5	5	**Ch2 Input :** These individual amplifier inputs are self-biasing, a.c. input analogue signals must be capacitively coupled to these pins, as shown in Figure 2.
6	6	**Ch3 Input :** In the powersave modes the inputs are biased at $V_{DD}/2$.
7	7	**Ch4 Input :** Note that amplifiers Ch1 to Ch8 are 'inverting amplifiers.'
8	8	**V_{BIAS} :** The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} as shown in Figure 2.
9	9	**Ch5 Input :** **Analogue Inputs :**
10	10	**Ch6 Input :**
11	11	**Ch7 Input :**
12	12	**Ch8 Input :**
13	13	**V_{SS} :** Negative supply rail (GND).
14	14	**Ch8 Output :** **Analogue Outputs :**
15	15	**Ch7 Output :** The individual "Gain Controlled" amplifier outputs.
16	16	**Ch6 Output :** Ch1 to Ch7 range from -3dB to +3dB in 0.43dB steps, Ch8 could be utilized as a volume control, ranging from -14dB to +14dB in 2.0dB steps.
17	17	**Ch5 Output :** In the powersave mode the selected output is biased at $V_{DD}/2$.
18	18	No internal connection. Do not use.
19	19	**Ch4 Output :** **Analogue Outputs**
20	20	**Ch3 Output :** Note that amplifiers Ch1 to Ch8 are 'inverting amplifiers.'
21	21	**Ch2 Output :**
22	22	**Ch1 Output :**
23	23	**V_{DD} :** Positive supply rail. A single +5-volt power supply is required.
24	24	**Control Data Input :** Operation of the 8 amplifier channels (Ch1 – Ch8) is controlled by the 8 bits of data entered serially at this pin . The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1MΩ pullup resistor.

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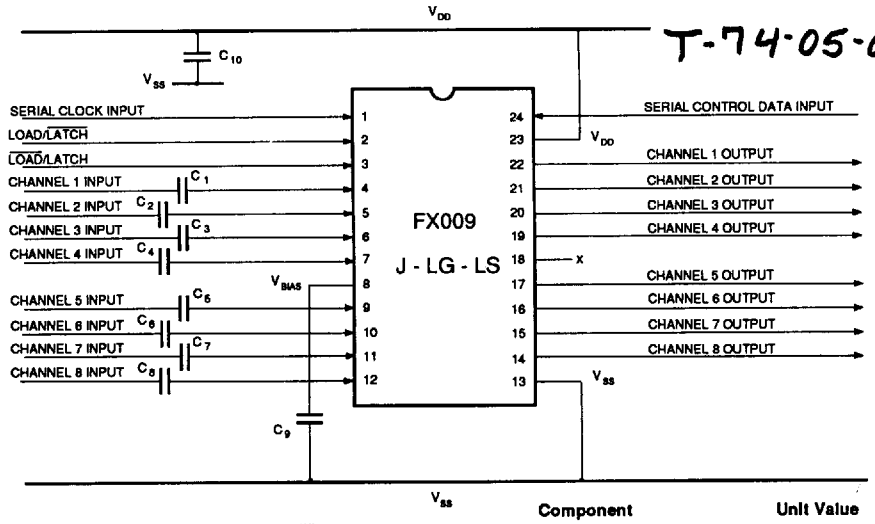


Notes

(1) Channel Amplifiers 1 to 8 are inverting amplifiers.

(2) Analogue input capacitors C_1 to C_8 are only required for a.c. input signals, d.c. input signals do not require these components.

Component	Unit Value
C_1 to C_8	0.1µ
C_9	1.0µ
C_{10}	1.0µ

Tolerances: C = ± 20%

Fig.2 External Component Connections

Application Recommendations

To avoid excess noise and instability in the final installation it is recommended that the following points be noted.

(a) A noisy or badly regulated power supply can cause instability and/or variance of selected gains.

(b) Care should be taken on the design and layout of the printed circuit board.

(c) All external components (Figure 2) should be kept close to the FX009 package.

(d) Inputs and outputs should be screened wherever possible.

(e) Tracks should be kept short.

(f) Analogue tracks should not run parallel to digital tracks.

(g) A "Ground Plane" connected to V_{SS} will assist in eliminating external pick-up on the channel input and output pins.

(h) Do not run high-level output tracks close to low-level input tracks.

(i) Input signal amplitudes should be applied with due regard to Figure 3.

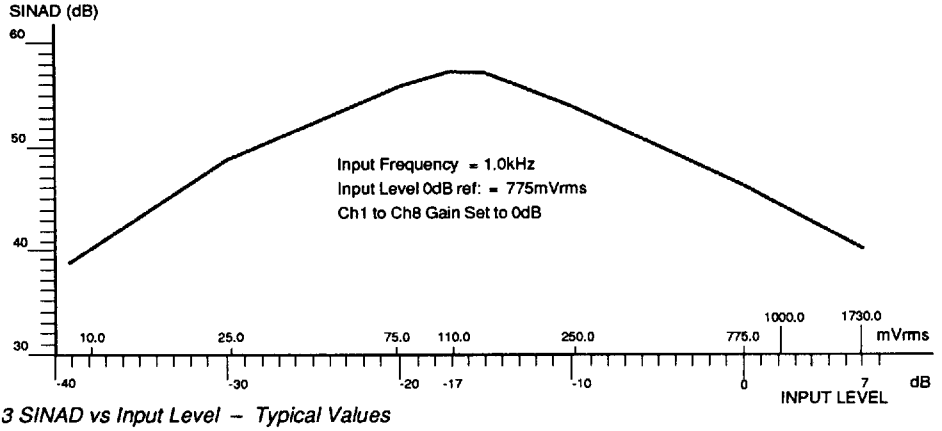


Fig.3 SINAD vs Input Level – Typical Values

Control Data and Timing

The gain of each amplifier block (Channel 1 to Channel 8) in the FX009 is set by a separate 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0), is loaded to the Control Data Input in serial format using the external data clock.

Data is loaded to the FX009 on the rising edge of the Serial Clock. Loaded data is executed on the falling (rising) edge of the Load/Latch (Load/Latch) pulse. Table 1 shows the format of each 4-bit Address word, Table 2 shows the format of each Gain Control word with Figure 4 describing the data loading operation and timing.

Table 1 Address Word Format

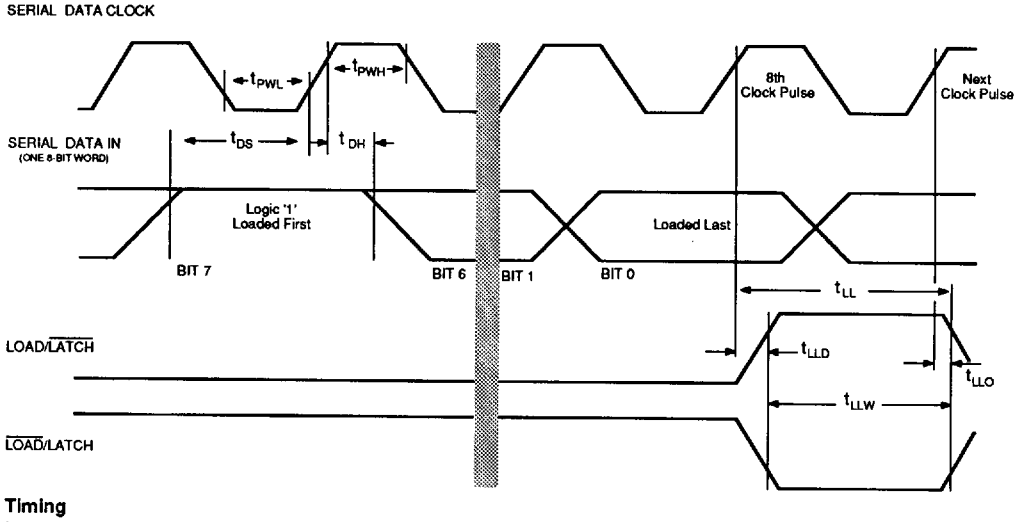
Bit 7 MSB	Bit 6	Bit 5	Bit 4 LSB	Channel Selected
1	0	0	0	1
1	0	0	1	2
1	0	1	0	3
1	0	1	1	4
1	1	0	0	5
1	1	0	1	6
1	1	1	0	7
1	1	1	1	8

Table 2 Gain Control Word Format

Bit 3 MSB	Bit2	Bit 1	Bit 0 LSB	Stage 1 to 7 (0.43dB)	Stage 8 (2.0dB)
0	0	0	0	Powersave	Powersave
0	0	0	1	-3.0	-14.0 dB
0	0	1	0	-2.571	-12.0 dB
0	0	1	1	-2.143	-10.0 dB
0	1	0	0	-1.714	-8.0 dB
0	1	0	1	-1.286	-6.0 dB
0	1	1	0	-0.857	-4.0 dB
0	1	1	1	-0.428	-2.0 dB
1	0	0	0	0	0 dB
1	0	0	1	0.428	2.0 dB
1	0	1	0	0.857	4.0 dB
1	0	1	1	1.286	6.0 dB
1	1	0	0	1.714	8.0 dB
1	1	0	1	2.143	10.0 dB
1	1	1	0	2.571	12.0 dB
1	1	1	1	3.0	14.0 dB

Data Loading

The 8-bit data word is loaded *bit 7 first and bit 0* last.
Bit 7 must be a logic "1" to address the chip.
If bit 7 in the word is a logic "0" that 8-bit word will not be executed. Figure 4 (below) shows the timing information required to load and operate this device.



Timing

t_{PWH} Serial Clock "High" Pulse Width
t_{PWL} Serial Clock "Low" Pulse Width
t_{DS} Data Set-up Time
t_{DH} Data Hold Time
t_{LLD} Load/Latch Delay
t_{LL} Load/Latch Set-up Time
t_{LLW} Load/Latch Pulse Width
t_{LLO} Load/Latch Over Time

Fig.4 Serial Control Data Loading Diagram

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX009J**	-30°C to +85°C (cerdip)
	FX009LG/LS	-30°C to +70°C (plastic)
Storage temperature range:	**FX009J**	-55°C to +125°C (cerdip)
	FX009LG/LS	-40°C to +85°C (plastic)

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Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. Audio Level 0dB ref: = 775mVrms. Amplifier Gain Set = 0dB.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current –					
– All Stages Quiescent		–	0.13	–	mA
– All Stages Operating		–	2.6	–	mA
Dynamic Values					
Control Functions					
Input Logic '1'		3.5	–	–	V
Input Logic '0'		–	–	1.5	V
Digital Input Impedances		0.5	1.0	–	MΩ
Amplifier Stages (General)					
Bandwidth (-3dB)		20.0	–	–	kHz
Output Impedance		–	0.8	3.0	kΩ
Total Harmonic Distortion	1	–	0.35	0.5	%
Output Noise Level (per stage)	2	–	180.0	400.0	µVrms
Onset of Clipping	3	–	1.73	–	Vrms
Gain Variation	4	–	–	0.1	dB
Interstage Isolation		–	60.0	–	dB
"Trimmer" Stages (Ch1 – Ch7)					
Gain		-3.0		+3.0	dB
Gain per Step (15 in No.)		–	0.43	–	dB
Step Error		–	–	0.2	dB
Input Impedance		100.0	–	–	kΩ
"Volume" Stage (Ch8)					
Gain		-14.0		+14.0	dB
Gain per Step (15 in No.)		–	2.0	–	dB
Step Error		–	–	0.4	dB
Input Impedance		50.0	–	–	kΩ
Timing (Figure 4)					
Serial Clock "High" Pulse Width (t_{PWH})		250	–	–	ns
Serial Clock "Low" Pulse Width (t_{PWL})		250	–	–	ns
Data Set-up Time (t_{DS})		150	–	–	ns
Data Hold Time (t_{DH})		50.0	–	–	ns
Load/Latch Set-up Time (t_{LL})		250	–	–	ns
Load/Latch Pulse Width (t_{LLW})		150	–	–	ns
Load/Latch Delay (t_{LLD})		200	–	–	ns
Load/Latch Over (t_{LLO})		–	–	50.0	ns
Serial Data Clock Frequency		–	–	2.0	MHz

Notes

1. Gain Set 0dB, Input Level 1kHz -3.0dB (549mVrms).
2. a.c short-circuit input, measured in a 30kHz bandwidth.
3. See Figure 3.
4. Over temperature and supply voltage range

Package Outlines

The FX009J, the cerdip package is shown in Figure 5. The 'LG' version is shown in Figure 6, and the 'LS' version in Figure 7. To allow complete identification, the FX009 LG and LS packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4.

Handling Precautions

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The FX009 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

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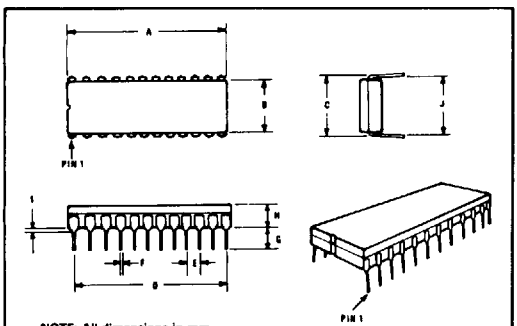
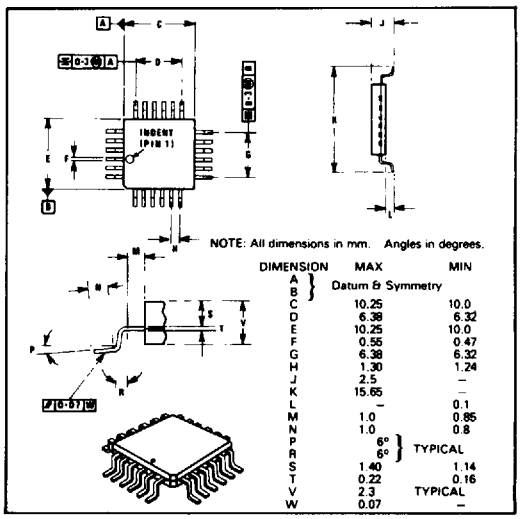
Fig. 5 **FX009J** *24-pin DIL Package*



NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.
A	32.03	31.50
B	14.81	13.06
C	15.61	15.14
D	28.04	27.84
E	2.54 }	TYPICAL
F	0.46 }	
G	4.30	4.10
H	4.35	3.99
I	1.40	TYPICAL
J	18.20	16.54

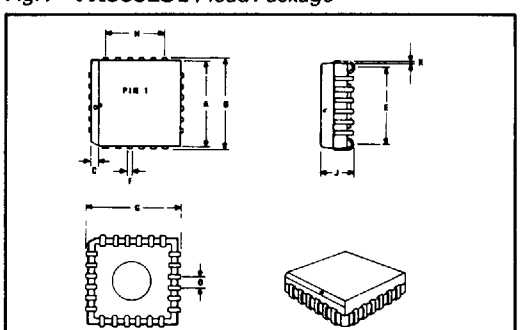
Fig. 6 **FX009LG** *24-pin Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX	MIN
A }	Datum & Symmetry	
B }		
C	10.25	10.0
D	6.38	6.32
E	10.25	10.0
F	0.55	0.47
G	6.38	6.32
H	1.30	1.24
J	2.5	–
K	15.65	–
L	–	0.1
M	1.0	0.85
N	1.0	0.8
P	6° }	TYPICAL
R	6° }	
S	1.40	1.14
T	0.22	0.16
V	2.3	TYPICAL
W	0.07	–

Fig. 7 **FX009LS** *24-lead Package*



All dimensions in mm. Angles in degrees

DIMENSION	MAX.	TYP.	MIN.	DIMENSION	MAX.	TYP.	MIN.
A	10.40		9.70	F	0.55		0.45
B	11.05		10.60	G	11.05		10.60
C		1.15 x 45°		H		6.35	
D		1.27		J	3.70		3.25
E		9.30		K	0.27		0.17

Ordering Information

FX009J	**24-pin cerdip DIL**
FX009LG	**24-pin quad plastic encapsulated bent and cropped**
FX009LS	**24-lead plastic leaded chip carrier**

Integrated Circuits Data Book

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Section 11

CONSUMER MICROCIRCUITS

Packaging and Applications

CML Packaging	11.2
Handling Precautions	11.6
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CML Packaging

For ease and convenience CML products are packaged for despatch in industry standard bulk or individual packaging as described below.

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- Trays (17cm x 10.5cm) and cardboard boxes with conductive foam.
- 50-pocket conductive trays for surface-mount microcircuits.
- Anti-static coated tubes, of various sizes, with thumbplugs.
- 13-inch reel Tape-and-Reel packaging which fully conforms to the latest EIC specification. The conductive embossed tape provides a secure cavity sealed with a peel-back cover tape. 500 units/reel – no partial reel counts are available.

CML Tape and Reel Specification

1. Scope

The specification relates to the tape packaging of integrated circuits suitable for use in "surface mount" assembly. It includes only those dimensions which are essential for the purchaser to use the product.

2. Dimensions (Refer to Figures 1a, 1b and 1c)

2.1	**Tape width**		W = 24 + 0.3mm
2.2	**Carrier Tape Thickness**		t = 0.3mm Max.
2.3	**Pitch of Sprocket Holes**		Po = 4.0 + 0.1mm
2.4	**Diameter of Sprocket Holes**		D = 1.5 + 0.1mm 1.5 - 0.00mm
2.5	**Distance**		E = 1.75 + 0.1mm
2.6	**Distance, centre to centre**		F = 11.5 + 0.1mm
2.7	**Dimension, centre to centre**		
2.7.1	LG		P2 = 10 + 0.1mm
2.7.2	LH		P2 = 6 + 0.1mm
2.7.3	LS		P2 = 6 + 0.1mm
2.8	**Embossed Pocket Dimension Ao and Bo**		
2.8.1	LG		Ao = 15.8 + 0.1mm
2.8.2	LG		Bo = 15.8 + 0.1mm
2.8.3	LH		Ao = 13.1 + 0.1mm
2.8.4	LH		Bo = 13.1 + 0.1mm
2.8.5	LS		Ao = 11.7 + 0.1mm
2.8.6	LS		Bo = 11.7 + 0.1mm
2.9	**Embossed Tape Dimension Ko**		
2.9.1		LG	Ko = 2.8 + 0.1mm
2.9.2		LH	Ko = 4.9 + 0.1mm
2.9.3		LS	Ko = 4.3 + 0.1mm
2.10	**Pitch of Component Compartments**		
2.10.1		LG	P = 20 + 0.1mm
2.10.2		LH	P = 16 + 0.1mm
2.10.3		LS	P = 16 + 0.1mm
2.11	**Outside Dimension of Pocket**		
2.11.1		LG	B1 = 16.4 + 0.1mm
2.11.2		LH	B1 = 13.8 + 0.1mm
2.11.3		LS	B1 = 12.3 + 0.1mm
2.12	**Pocket Centre Holes**		
2.12.1		LG	D1 = 2.0mm Min.
2.12.2		LH	D1 = 2.0mm Min.
2.12.3		LS	D1 = 2.0mm Min.

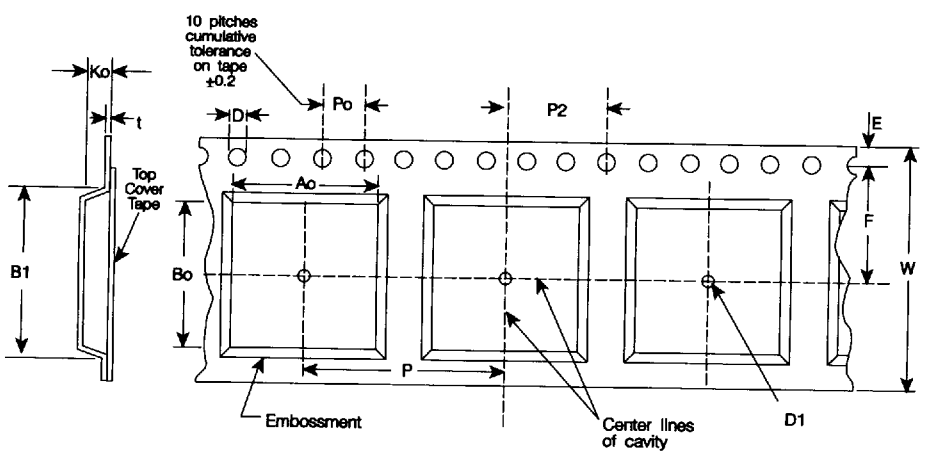

Fig.1a

CML Packaging .....

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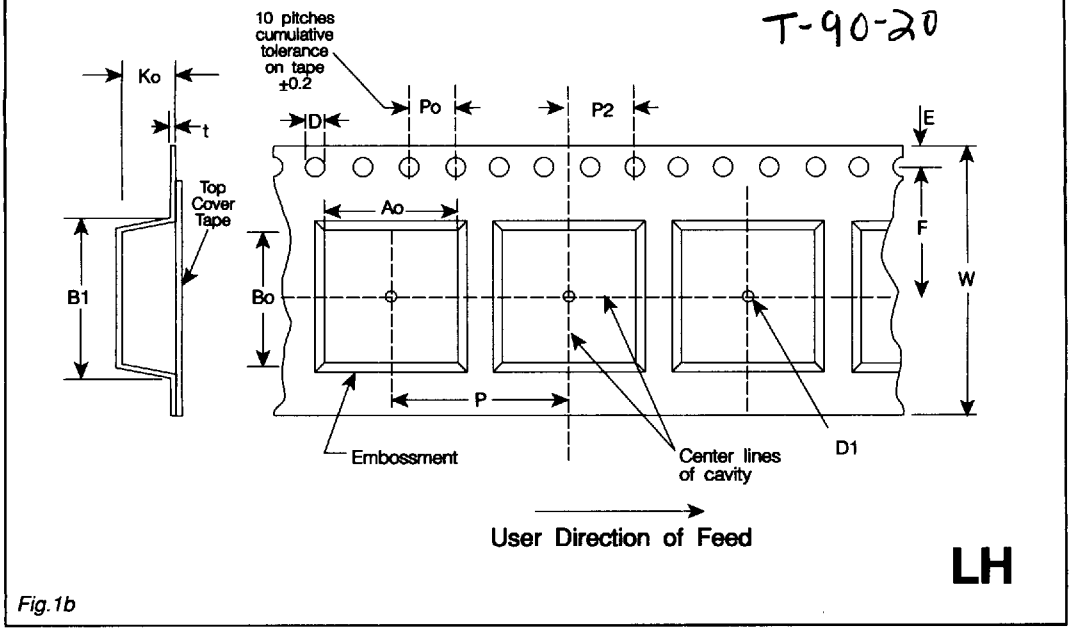

Fig.1b

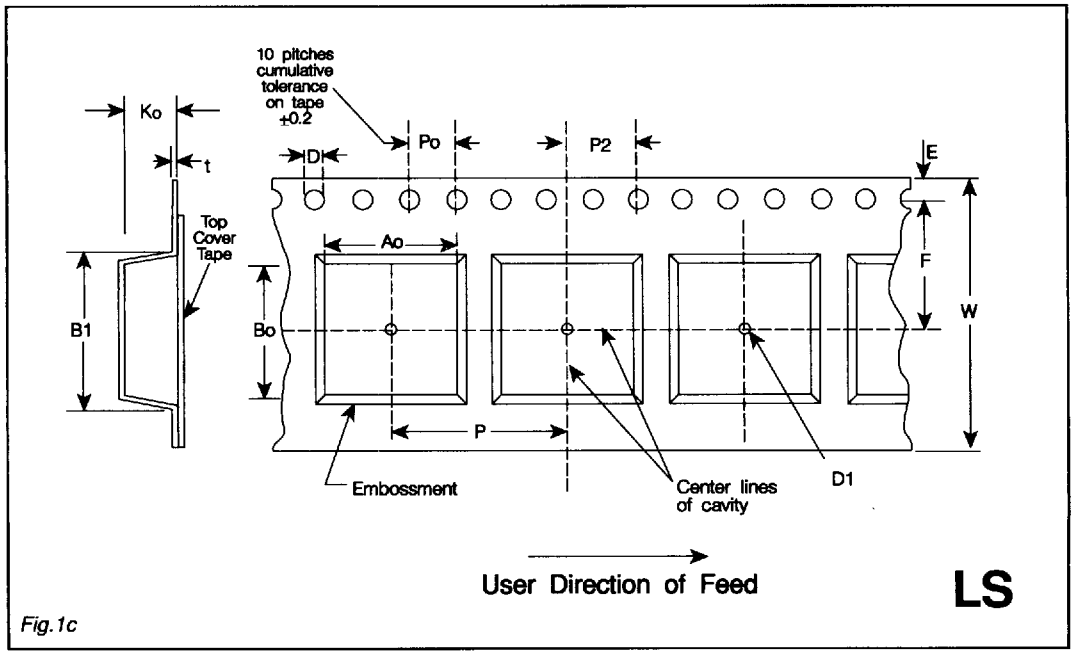

Fig.1c

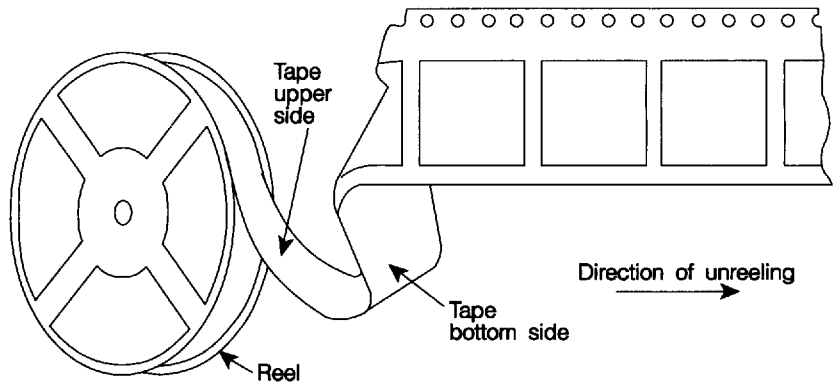

Fig.2 Tape Top and Bottom Orientation

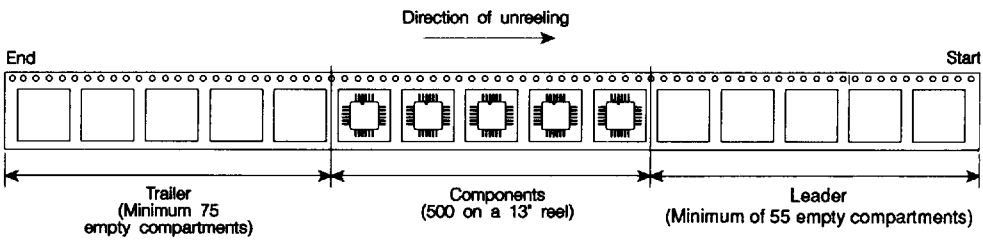

Fig.3 Layout of Tape

3. Materials

3.1 Carrier tape to be made of a conductive grade of polystyrene.

3.2 Conductive polycarbonate is also an approved carrier tape material and may be used under certain circumstances.

3.3 Cover tape is an anti-static grade of polypropylene/polyester film with a strip of pressure sensitive adhesive approximately 1mm wide along each edge.

4. Polarity and Orientation of Components in Tape

4.1 All components will be placed such that Pin 1 is adjacent to the sprocket holes (See Figures 6a and 6b).

4.2 The mounting side of the component shall be oriented to the bottom side of the tape (See Figure 2).

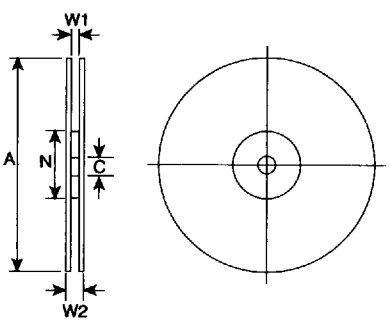

Fig.4 Reel Dimensions

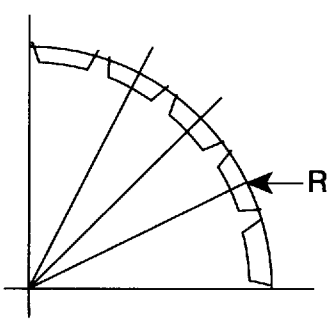

Fig.5 Minimum Radius = 30mm

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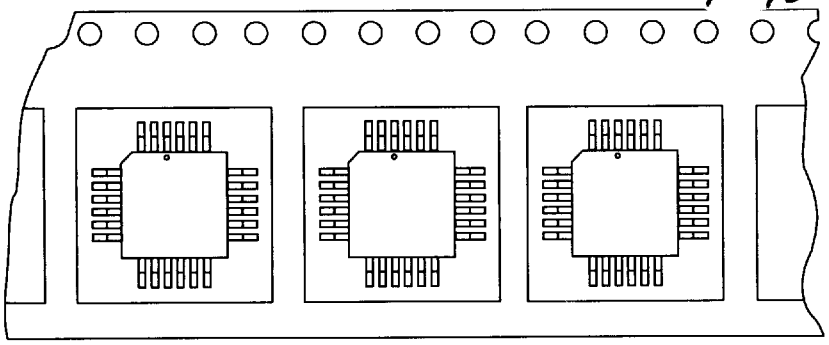
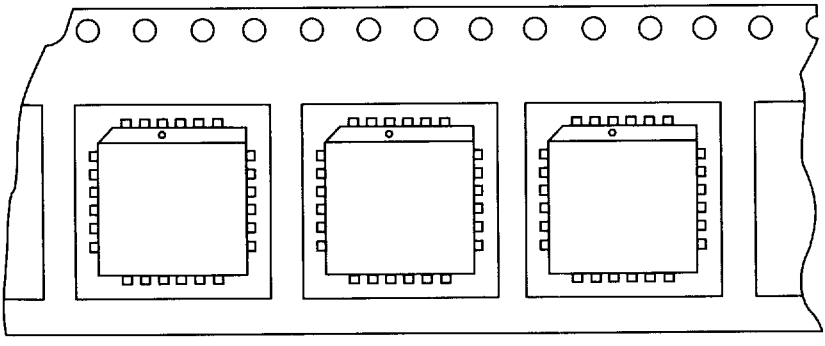
Fig.6a



User direction of feed

Fig.6b



User direction of feed

Fig.6 Component Orientation

5. Fixing of Components in Tape

5.1 Cover tapes shall not cover the sprocket holes.

5.2 Tapes in adjacent layers shall not stick together in the packing.

5.3 The adhesive of the cover tape shall not adversely effect the mechanical and electrical characteristics and marking of the components.

5.4 Components shall not stick to the carrier tape or the cover tape.

5.5 The tapes shall be suitable to withstand storage of the taped components without danger or migration of the terminations or the giving off of vapours which would impair soldering or deteriorate the component properties or termination by chemical action.

5.6 When the tape is bent with a minimum radius (See Figure 5) of 30mm, the tape shall not be damaged and the components shall remain in their position and orientation in the tape.

5.7 The peel strength of the cover tape shall be 50 ±25 grams measured at 175° - 180° with respect to the carrier tape along its longitudinal axis. The peel speed shall be 240mm/min.

5.8 After baking at 60°C for 48 hours or storage in ideal conditions for three months, the peel strength shall remain within the specified limits.

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6. Packaging

6.1 Tape will be wound on anti-static plastic reels (See Figure 4)

Dimensions

6.1.1	A	C	N	W1	W2
	Reel Dia.	Centre Hole	Hub Outer Dia.	Inside Cheek Width	Outside Cheek Width
	330mm	12.7mm	62.5mm	24.5mm	28.8mm

6.2 There will be a leader of a minimum of 55 empty compartments, at the start of the carrier tape (See Figure 3).

6.3 There will be no missing components between the first and last part of working tape in any reel.

6.4 At the end of the tape there will be a trailer of a minimum of 75 empty compartments (See Figure 3).

6.5 The tape shall release from the reel hub as the last portion of the carrier tape unwinds from the reel.

6.6 Components on a reel.

6.6.1 LG = 500
6.6.2 LH = 500
6.6.3 LS = 500

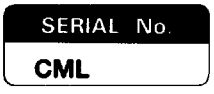
6.7 The tape will be prevented from unreeling by winding a paper tape around the reel and fixing with adhesive tape.

6.8 All reels will display:

1. Device Type
2. Quantity on reel
3. Date code
4. A static hazard warning label
5. CML Serial Number

6.9 Reel packed into anti-static bubble bag then in a cardboard box, with appropriate labelling as in paragraph 6.8.

6.10 Ideal storage conditions are 15°C to 20°C with a relative humidity of 60% - 70%.



Handling Precautions

CML microcircuits are CMOS LSI devices which include input protection. However precautions should be taken, at all times, to prevent static discharges which may cause device damage.

- It is recommended that the user initially stores and transports the microcircuit in the original supplied packaging.
- At all times observe anti-static precautions including the correct use of a conductive wrist-band and cord.
- Keep benches, personnel and test equipment at the same electrical potential.
- Ensure that the microcircuit is stored and operated well away from any potential source of static discharge.
- Do not insert or remove a microcircuit from an application whilst any power remains applied.
- Whenever possible ensure that the microcircuit is inserted after all other components have been mounted.
- Do not apply signals to a microcircuit until the power supply is suitably established.