

Buffers

74F240/74F240A 74F241/74F241A

74F240/240A Octal inverter buffer (3-state)
74F241/241A Octal buffer (3-state)

FEATURES

- Octal bus interface
- 3-state buffer outputs sink 64mA
- 15mA source current
- Guaranteed output skew less than 2.0ns (74F240A/74F241A)
- Reduced ground bounce (74F240A/74F241A)
- Reduced I_{CC} (74F241A only)
- Reduced loading (74F240A $I_{IL} = 100\mu A$, 74F241A $I_{IL} = 40\mu A$)

DESCRIPTION

The 74F240 and 74F241 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA. The device features two output enables, each controlling four of the 3-state outputs.

The 74F240A and 74F241A are functionally equivalent to their non-A counterparts. They have been designed to reduce effects of ground noise. Other advantages are noted in the features.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3ns	37mA
74F240A	3.8ns	40mA
74F241	5.0ns	53mA
74F241A	4.5ns	32mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^\circ C$ to $+70^\circ C$
20-pin plastic DIP	N74F240N, N74F240AN, N74F241N, N74F241AN
20-pin plastic SOL	N74F240D, N74F240AD, N74F241D, N74F241AD

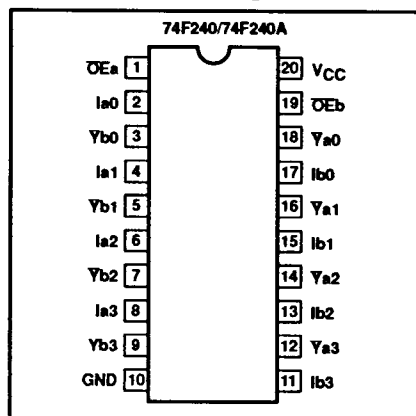
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I _a n, I _b n	Data inputs (74F240)	1.0/1.67	20 μA /1.0mA
	Data inputs (74F240A)	1.0/0.167	20 μA /100 μA
	Data inputs (74F241)	1.0/2.67	20 μA /1.6mA
	Data inputs (74F241A)	1.0/0.067	20 μA /40 μA
$\overline{O}Ea$, $\overline{O}Eb$	Output enable inputs (active low) (74F240)	1.0/0.33	20 μA /0.2mA
	Output enable inputs (active low) (74F240A)	1.0/0.167	20 μA /100 μA
$\overline{O}Ea$, $\overline{O}Eb$	Output enable input (74F241)	1.0/1.67	20 μA /1.0mA
	Output enable input (74F241A)	1.0/0.067	20 μA /40 μA
Y _a n, Y _b n	Data outputs (74F241, 74F241A)	750/106.7	15mA/64mA
$\overline{Y}a$ n, $\overline{Y}b$ n	Data outputs (74F240, 74F240A)	750/106.7	15mA/64mA

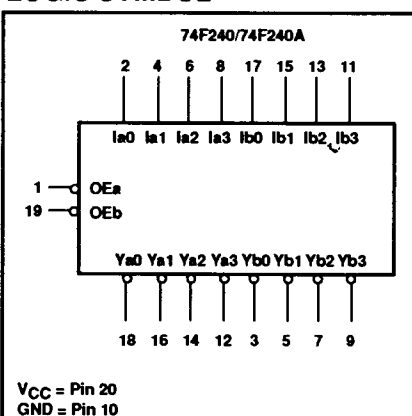
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20 μA in the high state and 0.6mA in the low state.

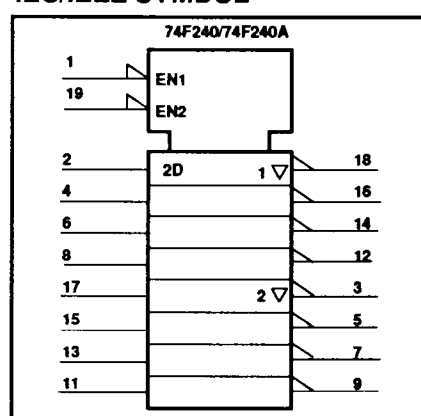
PIN CONFIGURATION



LOGIC SYMBOL



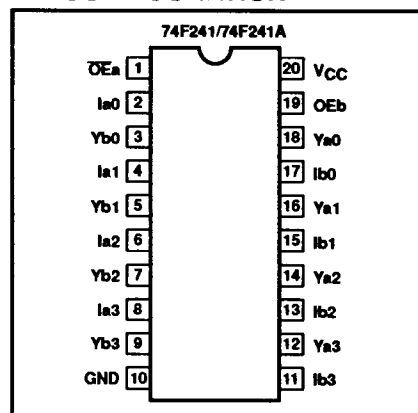
IEC/IEEE SYMBOL



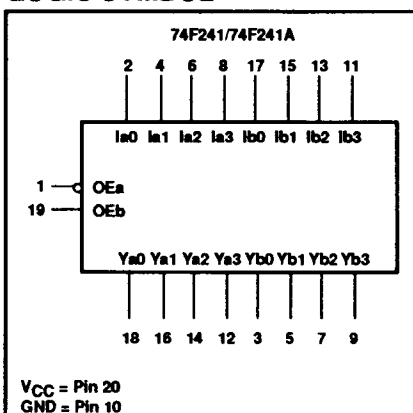
Buffers

74F240/74F240A
74F241/74F241A

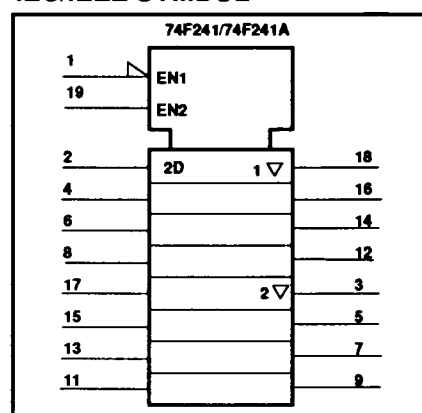
PIN CONFIGURATION



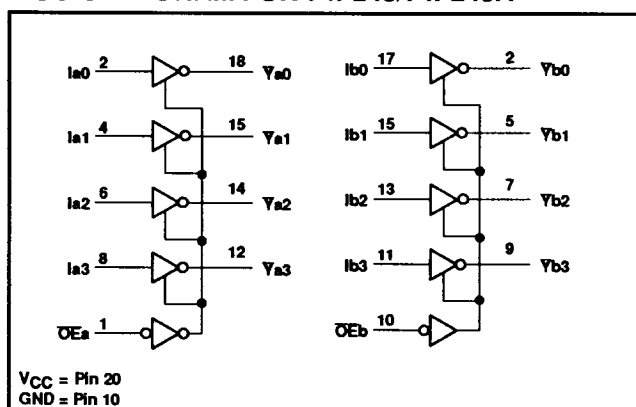
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM FOR 74F240/74F240A



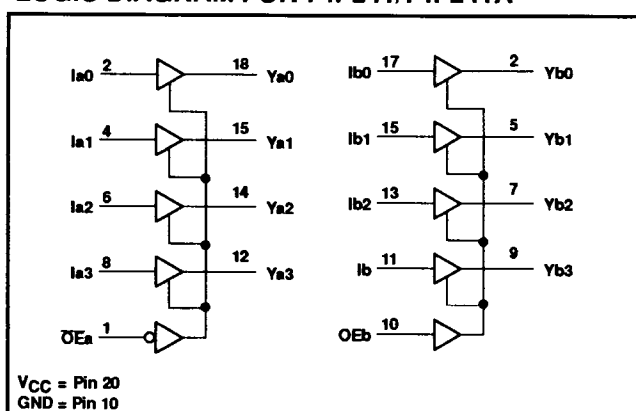
FUNCTION TABLE FOR 74F240/74F240A

INPUTS				OUTPUTS	
OEa	Ia	OEb	Ib	Ya	Yb
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

Notes to function table for 74F240/74F240A

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

LOGIC DIAGRAM FOR 74F241/74F241A



FUNCTION TABLE FOR 74F241/74F241A

INPUTS				OUTPUTS	
OEa	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

Notes to function table for 74F241/74F241A

1. H = High voltage level
2. L = Low voltage level
3. X = Don't care
4. Z = High impedance "off" state

Buffers

74F240/74F240A
74F241/74F241A**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	128	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free air temperature range	0		+70	°C

Buffers

74F240/74F240A
74F241/74F241A

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS ¹			LIMITS			UNIT
							MIN	TYP ²	MAX	
V _{OH}	High-level output voltage			V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -3mA	±10%V _{CC}	2.4			V
						±5%V _{CC}	2.7	3.4		V
					I _{OH} = -15mA	±10%V _{CC}	2.0			V
						±5%V _{CC}	2.0			V
V _{OL}	Low-level output voltage			V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN,	I _{OL} = MAX	±10%V _{CC}			0.50	V
						±5%V _{CC}		0.42	0.50	V
V _{IK}	Input clamp voltage			V _{CC} = MIN, I _I = I _{IK}				-0.73	-1.2	V
I _I	Input current at maximum input voltage			V _{CC} = MAX, V _I = 7.0V					100	μA
I _{IH}	High-level input current			V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL}	Low-level input current	74F240 all inputs	V _{CC} = MAX, V _I = 0.5V			-1.0	mA			
		74F240A all inputs				-100	μA			
		74F241 OEa, OEb				-1.0	mA			
		74F241 Ian, Ibn				-1.6	mA			
		74F241A all inputs				-40	μA			
I _{OZH}	Off-state output current, high-level voltage applied			V _{CC} = MAX, V _O = 2.7V					50	μA
I _{OZL}	Off-state output current, low-level voltage applied			V _{CC} = MAX, V _O = 0.5V					-50	μA
I _{OS}	Short-circuit output current ³			V _{CC} = MAX			-100		-225	mA
I _{CC}	Supply current (total)	74F240	I _{CC} H	V _{CC} = MAX		12	18	mA		
			I _{CC} L			50	70	mA		
			I _{CC} Z			35	45	mA		
		74F240A	I _{CC} H			28	37	mA		
			I _{CC} L			58	75	mA		
			I _{CC} Z			34	50	mA		
		74F241	I _{CC} H		V _{CC} = MAX		40	60	mA	
			I _{CC} L				60	90	mA	
			I _{CC} Z				65	90	mA	
		74F241A	I _{CC} H				20	30	mA	
			I _{CC} L				49	65	mA	
			I _{CC} Z				26	40	mA	

Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{\text{amb}} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Buffers

74F240/74F240A
74F241/74F241A

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to Y _n	74F240	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 5.0	ns
t _{PZH} t _{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	ns
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to Y _n	74F240A	Waveform 1	2.5 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns
t _{PZH} t _{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	2.0 3.5	4.0 5.0	6.5 7.5	2.0 3.0	7.0 8.5	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	3.5 2.5	6.0 5.0	1.5 1.0	6.5 5.5	ns
t _{sk(0)}	Output skew ^{1, 2}		Waveform 5			1.5		2.0	ns
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to Y _n	74F241	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.2 6.5	ns
t _{PZH} t _{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	6.7 8.0	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to Y _n	74F241A	Waveform 2	2.5 2.5	4.5 4.5	5.8 5.8	2.5 2.5	6.5 6.5	ns
t _{PZH} t _{PZL}	Output enable time to high or low level		Waveform 3 Waveform 4	2.5 3.5	4.5 5.0	6.0 7.0	2.0 3.0	6.7 8.0	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low level		Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	6.0 5.5	1.5 1.0	6.5 6.0	ns
t _{sk(0)}	Output skew ^{1, 2}		Waveform 5			1.5		2.0	ns

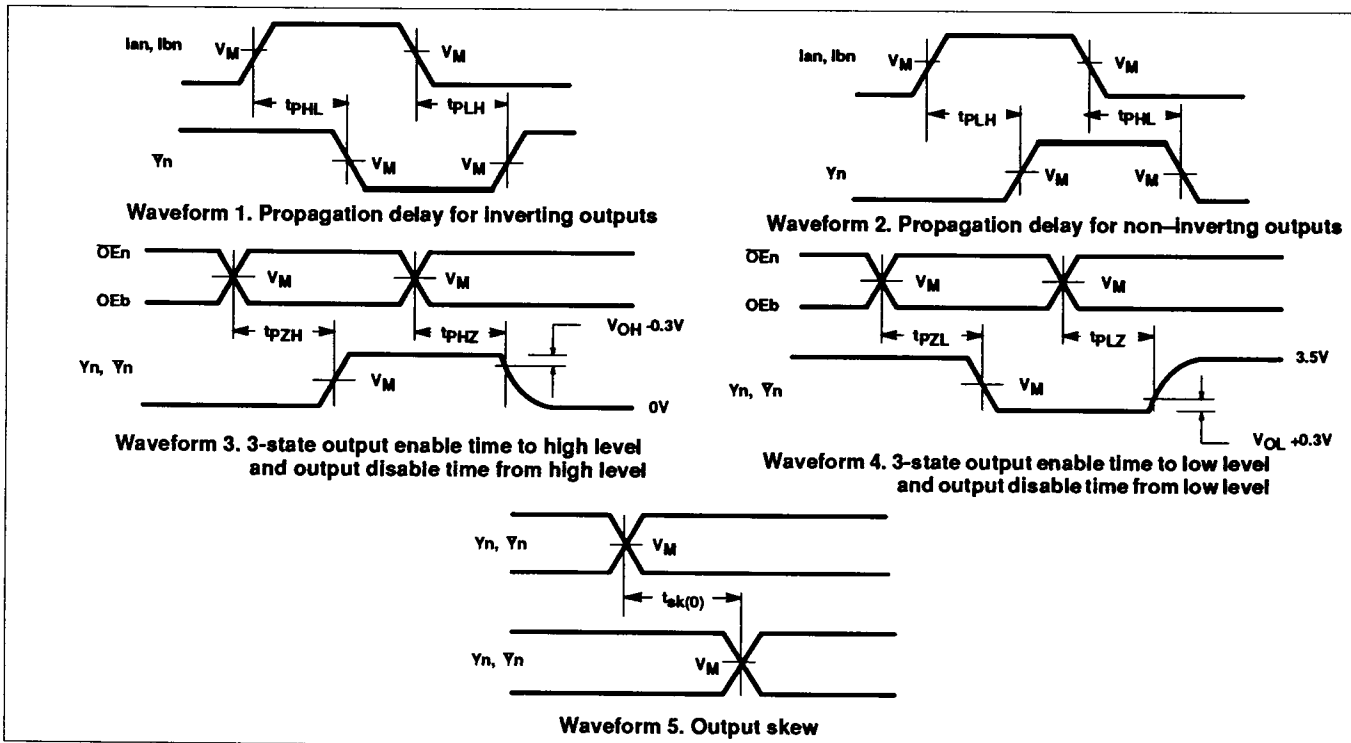
Notes to AC electrical characteristics

1. $|t_{PN} \text{ actual} - t_{PM} \text{ actual}|$ for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC} , loading, etc.).

Buffers

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74F241/74F241A

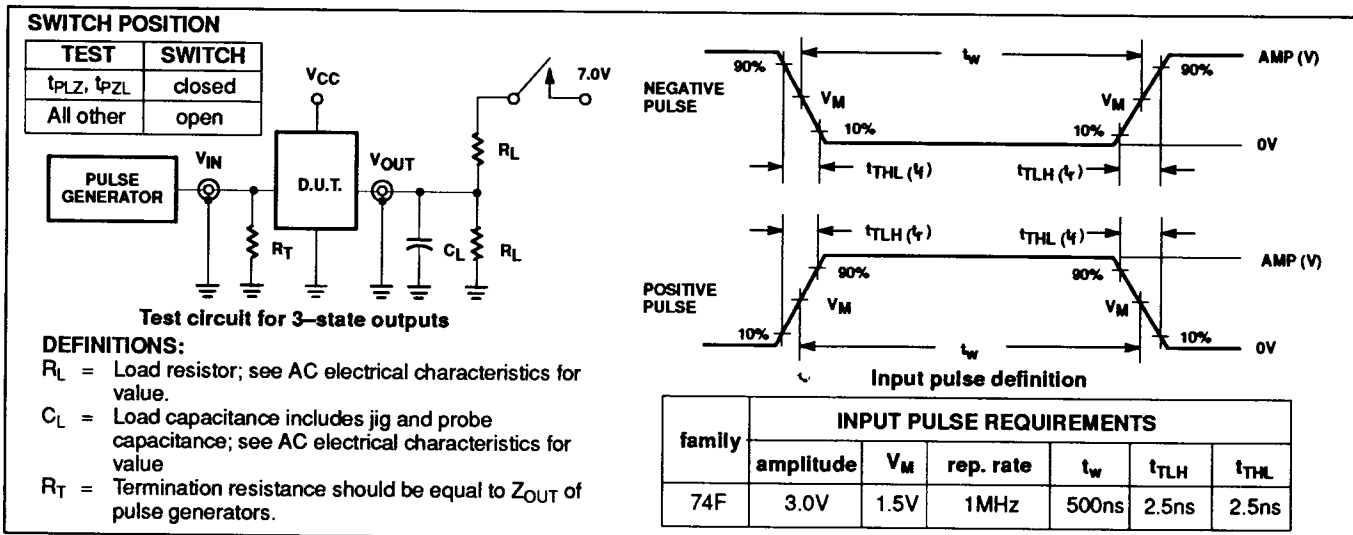
AC WAVEFORMS



Notes to AC waveforms

- For all waveforms, $V_M = 1.5V$.
- The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



VI. COMMERCIAL PRODUCT SPECIAL PROCESSING T-90-20

SUPR II LEVEL B PRICING ADDERS

SUPR II LEVEL B

Signetics Upgraded Product Reliability (SUPR) program is designed to provide customers whose systems require an infant mortality level less than that of our non-burned-in products (which is typically below 1000 PPM).

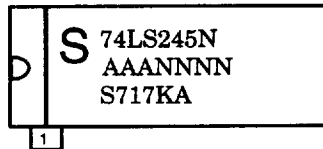
DEVICE AVAILABILITY

Products available for Level B processing are identified in the Price Book with a "B" suffix to the basic part number.

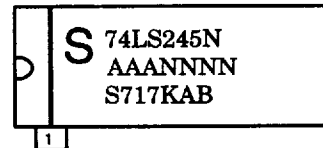
PRODUCT FAMILY	SUGGESTED RESALE ADDERS		
	1-99	100-999	OVER 1000
LIN	.14	.14	.11
LOG (TTL)			
(SSl)	.12	.10	.08
(MSl)	.16	.14	.11
(OCT)	.16	.14	.11
(CTM)	.16	.14	.11
LOG (ECL)			
(SSl)	.25	.23	.20
(MSl)	.25	.23	.20
LOG (LSI)	Consult Factory for Pricing		
(RAM)			
MIC (8X)			
PLD	Consult Factory for Pricing		
MCG	Consult Factory for Pricing		
DAT	Not Available		
MIC			

MARKING FORMAT EXAMPLES

Standard (no Burn-In) Products (Dual-in-line)



SUPR II (Burned-In) Products (Dual-in-line)



NOTE: The "B" in the 7th position on the 3rd line, when present, is the SUPR II Burn-In indicator.

TAPE AND REEL PACKAGING

SPECIFICATIONS

Tape and Reel specifications conform to Electronic Industries Association (EIA) Proposed Specification #EIA-481-A using 13 inch reels. Current incremental quantities reflect the quantities per reel. As more customers are able to handle a larger quantity per reel, this quantity will be increased.

DEVICE AVAILABILITY

Products available in tape and reel packaging are identified in the Price Book with a "T" suffix to the basic part number and are only offered as a product for sale by the reel. Return of product is limited to full reels with unbroken quality seals.

TAPE AND REEL PRICING ADDERS

PRODUCT FAMILY	SUGGESTED RESALE ADDER
MCG	.07
LIN	.07
LOG	.07
DAT MIC	PACKAGE A28 = .20 A44 = .25 A52 = .30 A68 = .40 A84 = .45 D24 = .17

VII. PACKING QUANTITY INFORMATION

T-90-20

CERAMIC DUAL IN-LINE (CERDIP)

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	DEVICES PER BOX
F/FE, BPA, PA	8-pin (300-mil)	48	1920
F, BCA, CA	14-pin (300-mil)	25	1000
F, BEA, EA	16-pin (300-mil)	25	1000
F, BVA, MVA	18-pin (300-mil)	21	840
F/FA, BRA, RA	20-pin (300-mil)	20	800
F, BWA, WA	22-pin (400-mil)	17	544
F/FA/F6, BJA, JA	24-pin (600-mil)	15	360
F/FA/F3/F24, BLA, LA	24-pin (300-mil)	15	600
F, BXA, XA	24-pin (400-mil)	15	480
F/FA/F28, BXA, XA	28-pin (600-mil)	13	312
FA	32-pin (600-mil)	11	264
F/FA/F40, BQA, MQA, QA	40-pin (600-mil)	9	216

CERPAC

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	
BDA/DA/W	14-pin	145	
BFA/FA/W	16-pin	145	
BXA/BYA/W	18-pin	100	
BSA/SA/W/WB	20-pin	100	
BKA/KA/W	24-pin	120	
BYA/YA/W	28-pin	50	

CERQUAD

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TRAY	DEVICES PER BOX
KA/K44	44-pin	6	6
KA/K68	68-pin	4	4
KA	84-pin	42	210

LEADLESS CHIP CARRIER

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	
B2A/2A/GA	20-pin	55	
B3A/3A/GA/GC1	28-pin	43	
YA/YA/GC2	32-pin	35	
BUA/MXA/MUA/UA/XA/GA/GC	44-pin	27	
BZA/BUA/UA/ZA/GA/GC	68-pin	19	

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.

VII. PACKING QUANTITY INFORMATION

T-90-20

PLASTIC DUAL IN-LINE

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	DEVICES PER BOX
N/N8	8-pin (300-mil)	50	2000
N/N14/N16	14- 16-pin (300-mil)	25	1000
N	18-pin (300-mil)	20	800
N/N20	20-pin (300-mil)	18	720
N	22-pin (400-mil)	17	544
N/N6	24-pin (600-mil)	15	360
N/N3/N24	24-pin (300-mil)	15	600
N/N24	24-pin (400-mil)	15	480
N/N28	28-pin (600-mil)	13	312
N/N3	28-pin (300-mil)	13	520
N	32-pin (600-mil)	11	264
N/N40	40-pin (600-mil)	9	216
NB (Shrink)	42-pin (600-mil)	12	288
N/N48	48-pin (600-mil)	7	168
N	50-pin (900-mil)	7	112
N/N64	64-pin (900-mil)	5	80

PLASTIC LEADED CHIP CARRIER (PLCC)

PACKAGE CODE	PIN COUNT	QUANTITIES		
		DEVICES PER TUBE	DEVICES PER BOX	DEVICES PER REEL
A	20-pin	46	3680	1000
A/A28	28-pin	37	2368	750
A	32-pin	31	2232	750
A/A44	44-pin	26	1248	500
A/A52	52-pin	23	1012	500
A/A68	68-pin	18	648	250
A/A84	84-pin	15	420	250

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.

VII. PACKING QUANTITY INFORMATION

T-90-20

PLASTIC SMALL OUTLINE (SO)

PACKAGE CODE	PIN COUNT	QUANTITIES		
		DEVICES PER TUBE	DEVICES PER BOX	DEVICES PER REEL
D/D8	8-pin (150-mil)	100	10000	2500
D	8-pin (300-mil)	64	2560	1000 - 13" 700 - 7"
D/D14	14-pin (150-mil)	57	5700	2500
D	16-pin (150-mil)	50	5000	2500
D	16-pin (300-mil)	48	1920	1000
DK(SSOP)	20-pin (170-mil)	75	6750	2500
D	20-pin (300-mil)	38	1520	1000
D/D24	24-pin (300-mil)	32	1280	1000
D	28-pin (300-mil)	27	1080	1000
D	40-pin (VSO-40)	31	1240	1000 - 13" 300 - 7"
D	56-pin (VSO-56)	22	616	1000

QUAD FLAT PACK*

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TRAY	DEVICES PER BOX
B/B44	44-pin	50	500
B/B44	44-pin	96	480
B	52-pin	119	595
B	80-pin	66	330
B	100-pin	50	250
B	120-pin	24	120
B	120-pin (Philips source)	30	150

- * Quad Flat Pack parts require dry pack handling according to EIA Standard - 583.
These parts are identified in part list section with DRY PACK in the Cross Ref Part No field.

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.