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Status	Product Specification
FAST Products	

FAST 74F298

Multiplexer

Quad 2-Input Multiplexer With Storage

FEATURES

- Fully synchronous operation
- Select from two data sources
- Buffered, negative edge triggered clock
- Provides the equivalent of function capabilities of two separate MSI functions (74F157 and 74F175)

DESCRIPTION

The 74F298 is a high speed Quad 2-Input Multiplexer with storage. It selects 4 bits of data from two sources (ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the High-to-Low transition of the clock (\overline{CP}). The 4-bit register is fully edge triggered. The data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the High-to-Low transition of the clock for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F298	115MHz	30mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
16-pin Plastic DIP	N74F298N
16-pin Plastic SO	N74F298D

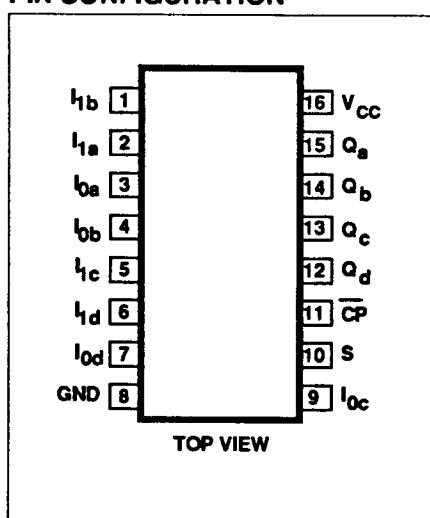
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a}, I_{0b}, I_{0c}, I_{0d}$	Data inputs	1.0/1.0	20 μA /0.6mA
$I_{1a}, I_{1b}, I_{1c}, I_{1d}$	Data inputs	1.0/1.0	20 μA /0.6mA
S	Select input	1.0/1.0	20 μA /0.6mA
\overline{CP}	Clock input (active falling edge)	1.0/1.0	20 μA /0.6mA
Q_a, Q_b, Q_c, Q_d	Data outputs	50/33	1.0mA/20mA

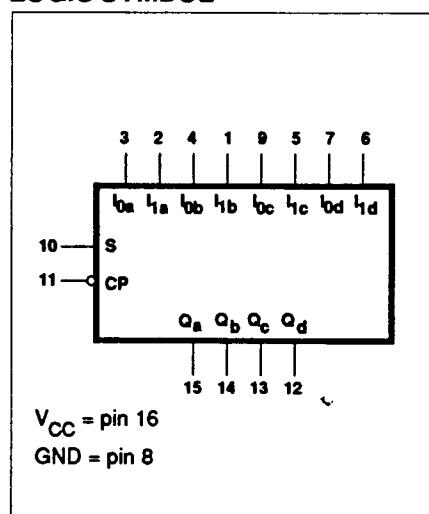
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μA in the High state and 0.6mA in the Low state.

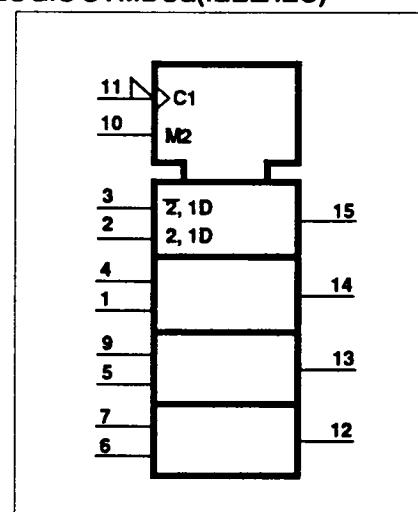
PIN CONFIGURATION



LOGIC SYMBOL



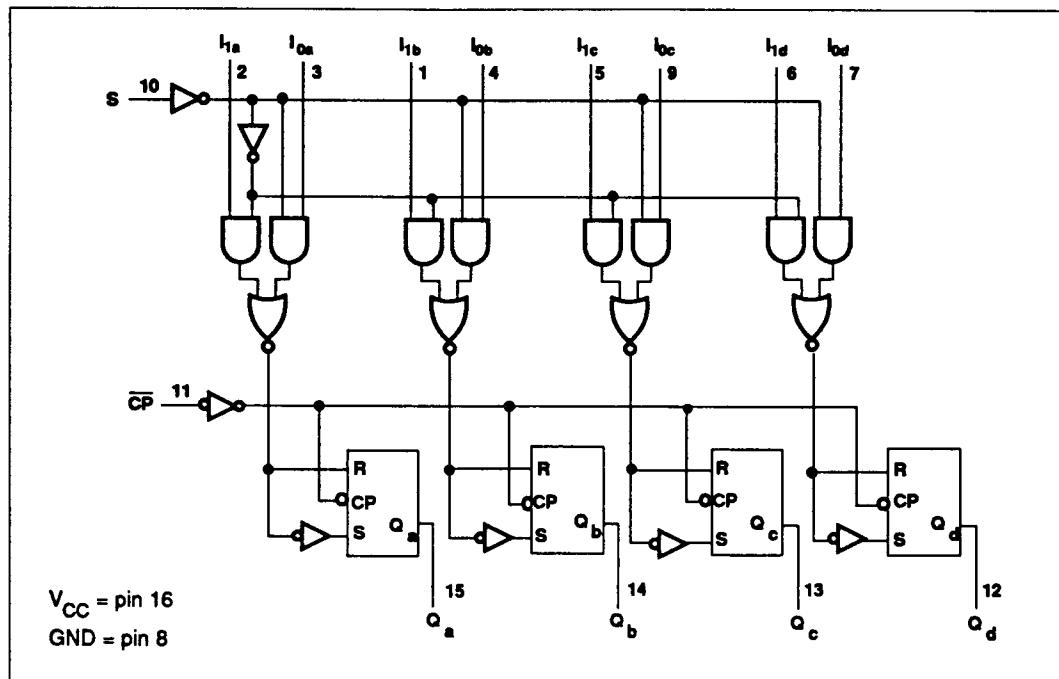
LOGIC SYMBOL(IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT	OPERATING MODE
\overline{CP}	S	I_{in}	I_{in}	Q_n	
↓	I	I	X	L	Load source "0"
↓	I	h	X	H	
↓	h	X	I	L	
↓	h	X	h	H	Load source "1"

H = High voltage level

h = High voltage level one set-up time prior to the High-to-Low clock transition

L = Low voltage level

I = Low voltage level one set-up time prior to the High-to-Low clock transition

X = Don't care

↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹			LIMITS		UNIT	
					Min	Typ ²		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$	$I_{OH} = \text{MAX}$	$\pm 10\% V_{CC}$	2.5		V	
				$\pm 5\% V_{CC}$	2.7	3.4		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$	$\pm 10\% V_{CC}$		0.30	0.50	V
				$\pm 5\% V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7.0V$					100	μA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7V$					20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.5V$					-0.6	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$			30	40	mA
		I_{CCL}				32	40	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25^\circ C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0^\circ C \text{ to } +70^\circ C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	115		105		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q _n	Waveform 1	4.0 4.5	5.5 6.5	7.5 8.5	4.0 4.5	9.0 9.5	ns

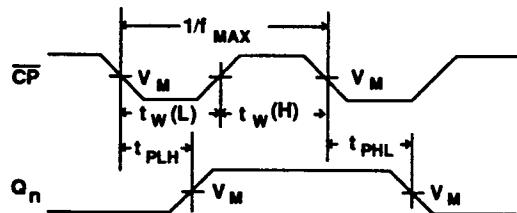
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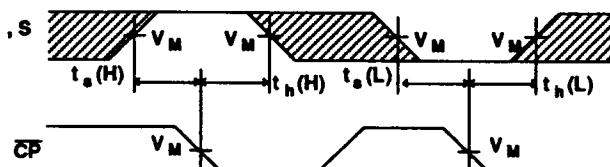
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			$T_A = +25^\circ\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
			Min	Typ	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup time, High or Low I_{on}, I_{in} to \bar{CP}	Waveform 2	2.0 2.0			2.0 2.0		ns	
$t_h(H)$ $t_h(L)$	Hold time, High or Low I_{on}, I_{in} to \bar{CP}	Waveform 2	1.0 1.0			1.0 1.0		ns	
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to \bar{CP}	Waveform 2	6.0 5.0			7.0 6.0		ns	
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to \bar{CP}	Waveform 2	0 0			0 0		ns	
$t_w(H)$ $t_w(L)$	\bar{CP} Pulse width, High or Low	Waveform 1	5.0 5.0			5.0 7.0		ns	

AC WAVEFORMS



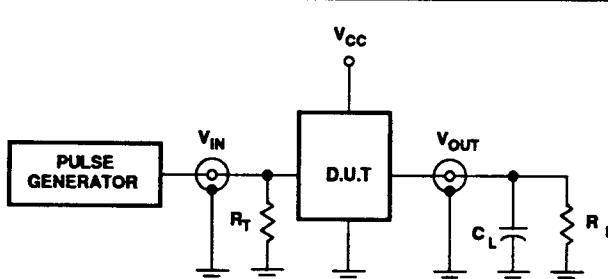
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



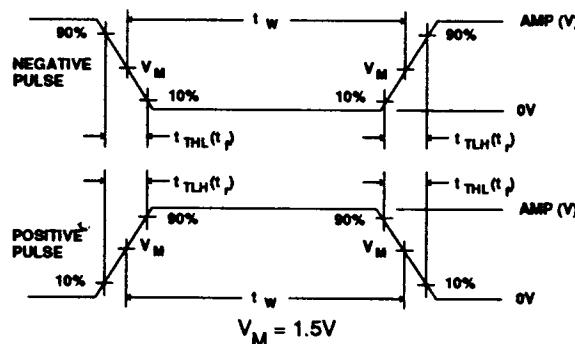
Waveform 2. Data Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5\text{V}$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns