Philips Semiconductors-Signetics

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Status	Product Specification
FAST Products	

FAST 74F538
1-Of-8 Decoder (3-state)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F538	8.5 ns	35mA

DESCRIPTION

The 74F538 decoder/demultiplexer accepts three address (A_0 - A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low or active High. The 'F538 has 3-state outputs, and a High signal on the Output Enables ($\overline{OE}_n$) inputs will force all outputs to the high impedance state. Two active High (E_2, E_3) and active Low ($\overline{E}_0$, $\overline{E}_1$) inputs are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

ORDERING INFORMATION

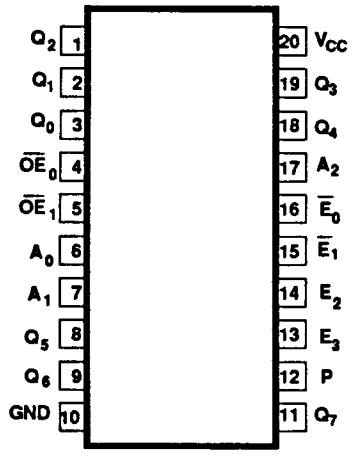
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F538N
20-Pin Plastic SOL	N74F538D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
E_2, E_3	Enable inputs (active High)	1.0/1.0	20µA/0.6mA
P	Polarity control input	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

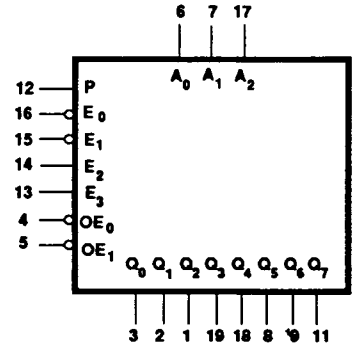
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



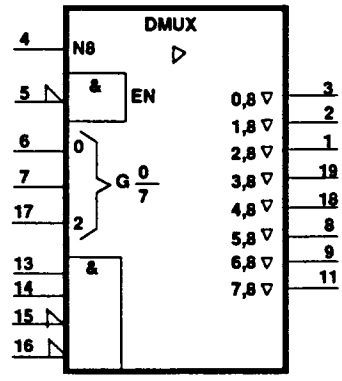
TOP VIEW

LOGIC SYMBOL

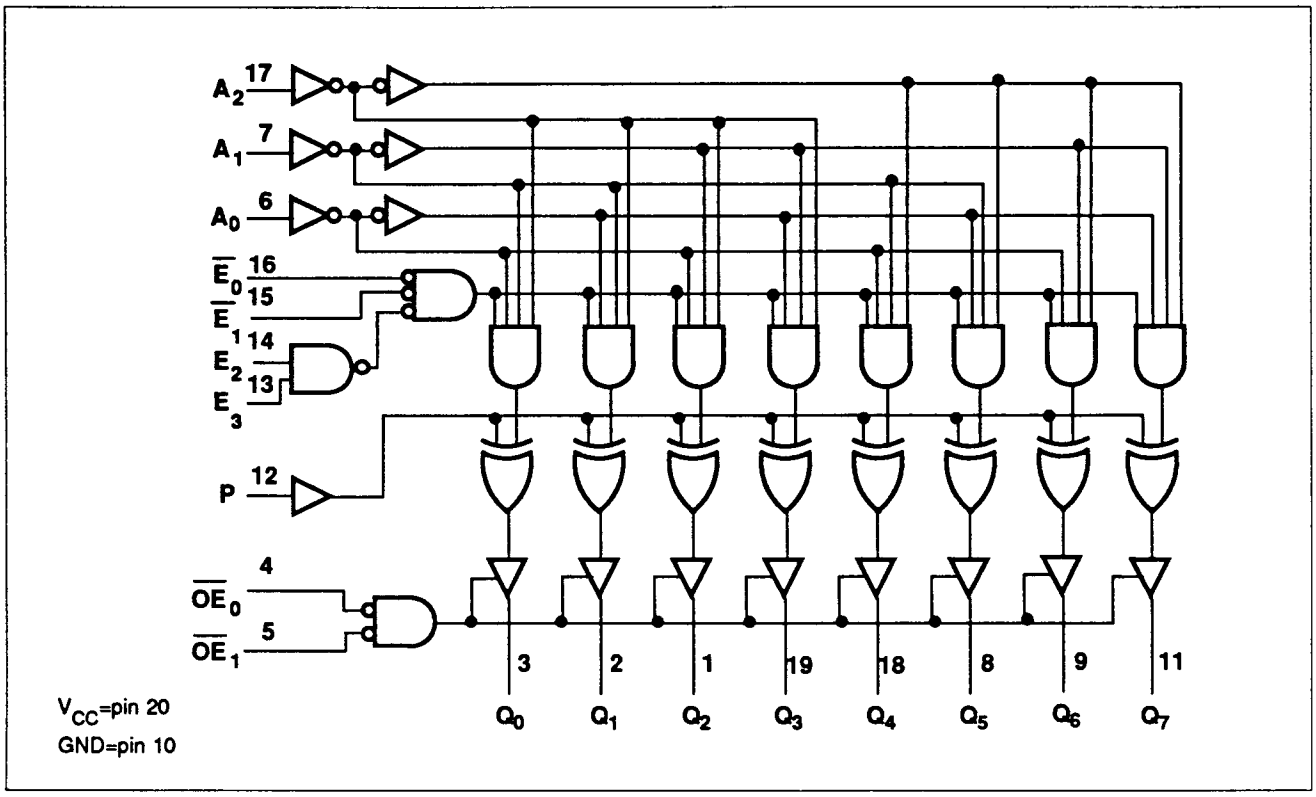


V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS								OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	High impedance
X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	L	H	X	X	X	X	X	X	Outputs equal P input								Disable
L	L	X	H	X	X	X	X	X									
L	L	X	X	L	X	X	X	X									
L	L	X	X	X	L	X	X	X									
L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	Active High output (P=L)
L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L	
L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L	
L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L	
L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	
L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L	
L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L	
L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H	
L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H	Active Low output (P=H)
L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				35	50	mA
		I_{CCZ}				35	50	mA

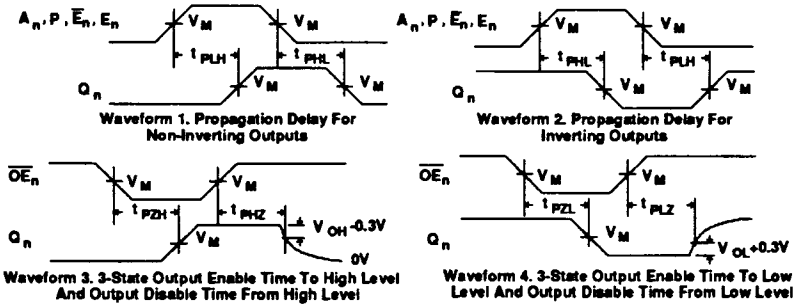
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

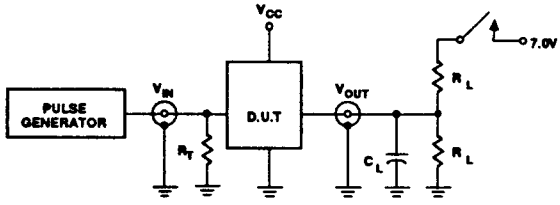
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1, 2	5.5 3.0	8.5 7.5	13.0 12.5	5.0 3.0	14.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to Q_n	Waveform 1, 2	5.5 3.0	8.5 7.5	12.0 12.0	5.0 3.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay E_2 or E_3 to Q_n	Waveform 1, 2	6.5 4.0	9.0 7.0	12.5 12.5	5.5 3.5	13.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1, 2	4.5 3.5	9.5 6.5	15.0 10.0	4.0 3.5	16.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	2.5 6.5	5.5 9.5	9.5 13.5	2.0 6.0	11.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	1.0 1.0	3.0 3.5	6.0 8.5	1.0 1.0	7.0 9.5	ns

AC WAVEFORMS



NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

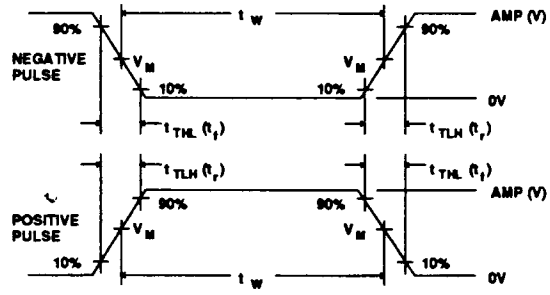
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns