Philips Semiconductors-Signetics

Document No.	853-1368
ECN No.	01258
Date of issue	December 13, 1990
Status	Product Specification
FAST Products	

FAST 74F711A/711-1, 74F712A/712-1 Multiplexers

74F711A Quint 2-to-1 Data Selector Multiplexer (3-State)
74F711-1Quint 2-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance (3-State)
74F712A Quint 3-to-1 Data Selector Multiplexer
74F712-1 Quint 3-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance

FEATURES for 74F711A/711-1

- **Consists of five 2-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **Output inverting/non-inverting option**
- **30 ohm termination impedance on each output-'F711-1**
- **Outputs sink 64mA ('F711A only)**

FEATURES for 74F712A/712-1

- **Consists of five 3-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **30 ohm termination impedance on each output-'F712-1**
- **Outputs sink 64mA ('F712A only)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711A	6.0ns	30mA
74F711-1	6.5ns	29mA
74F712A	5.5ns	25mA
74F712-1	6.5ns	25mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F711AN, N74F711-1N
24-Pin Plastic Slim DIP (300 mil)	N74F712AN, N74F712-1N
20-Pin Plastic SOL	N74F711AD, N74F711-1D
24-Pin Plastic SOL	N74F712AD, N74F712-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F711A/ 'F711-1	D_{na}, D_{nb}	Data inputs	1.0/0.066	20μA/40μA
	S	Select input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input (active Low)	1.0/0.033	20μA/20μA
	$\overline{INV}$	Output Inverting input (active Low)	1.0/0.033	20μA/20μA
	Q_0 - Q_4	Data outputs for 'F711A	750/106.7	15mA/64mA
	Q_0 - Q_4	Data outputs for 'F711-1	750/8.33	15mA/5mA
'F712A/ 'F712-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.066	20μA/40μA
	S_0, S_1	Select inputs	1.0/0.033	20μA/20μA
	Q_0 - Q_4	Data outputs for 'F712A	750/106.7	15mA/64mA
	Q_0 - Q_4	Data outputs for 'F712-1	750/8.33	15mA/5mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F711A/711-1 consist of five 2-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 'F711A has a common select (S) input, an Output Enable ($\overline{OE}$) input and an Output Inverting ($\overline{INV}$) input to control the 3-state outputs. The outputs source 15mA and sink 64mA. The 'F711-1 is the same as the 'F711A except that it has a 30 ohm termination impedance on each output to reduce line noise and the 3-state outputs sink 5mA.

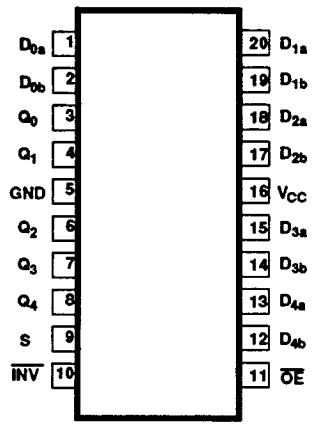
When the inverting input ($\overline{INV}$) is Low, the input data path is inverted.

To improve speed and noise immunity, V_{CC} and GND side pins are used.

The 74F712A/712-1 consist of five 3-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 'F712A has two select (S_0,S_1) inputs to determine which set of five inputs will be propagated to the five outputs. The outputs source 15mA and sink 64mA. The 'F712-1 is the same as the 'F712A except that it has a 30 ohm termination impedance on each output to reduce line noise and the outputs sink 5mA.

PIN CONFIGURATION

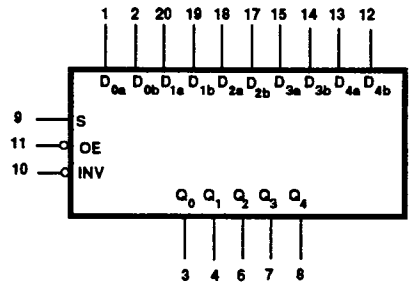
'F711A/'F711-1



TOP VIEW

LOGIC SYMBOL

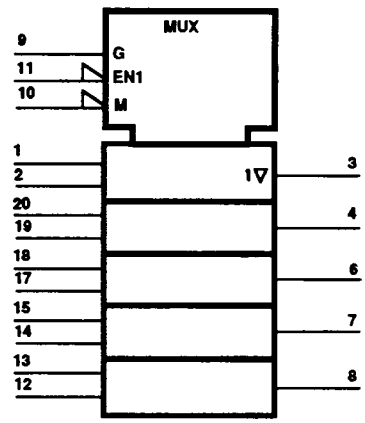
'F711A/'F711-1



V_{CC} = Pin 16
GND = Pin 5

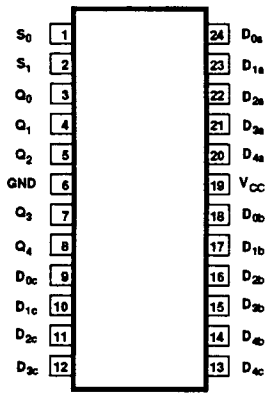
LOGIC SYMBOL(IEEE/IEC)

'F711A/'F711-1



PIN CONFIGURATION

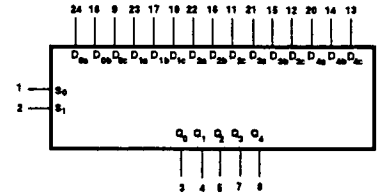
'F712A/'F712-1



TOP VIEW

LOGIC SYMBOL

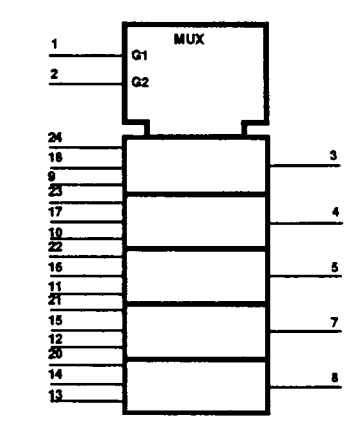
'F712A/'F712-1



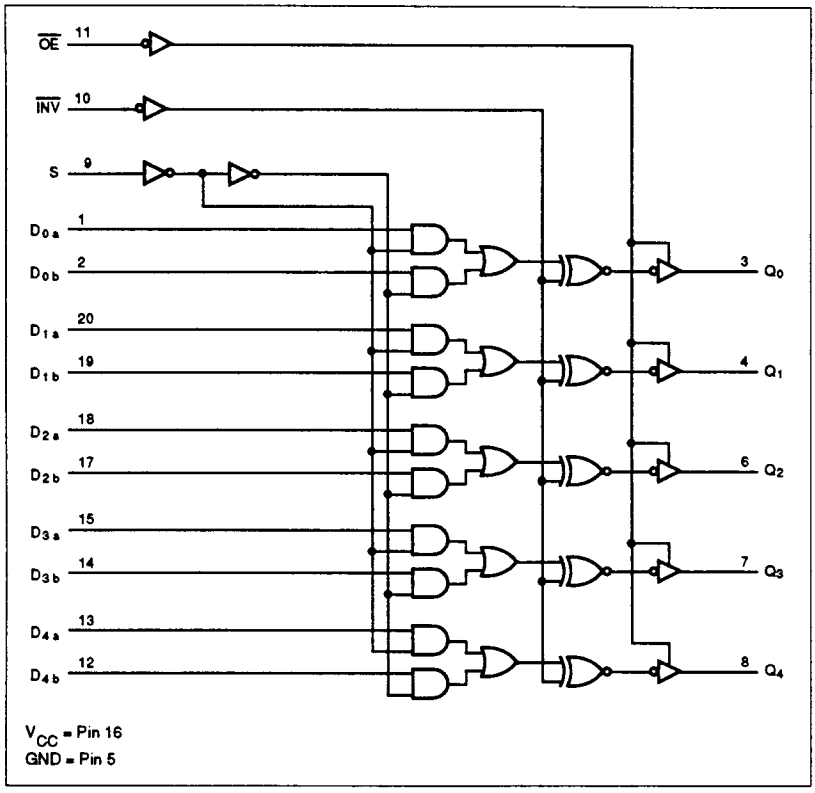
V_{CC} = Pin 19
GND = Pin 6

LOGIC SYMBOL(IEEE/IEC)

'F712A/'F712-1



LOGIC DIAGRAM for 'F711A/'F711-1

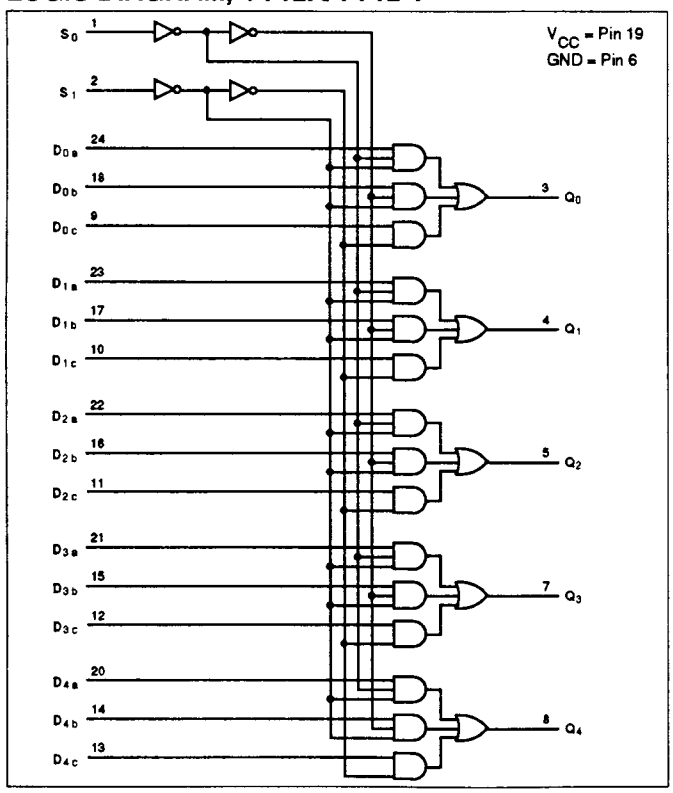


FUNCTION TABLE for 'F711A/'F711-1

INPUTS					OUTPUT
S	INV	OE	D_{na}	D_{nb}	Q_n
L	L	L	data a	data b	data a
H	L	L	data a	data b	data b
L	H	L	data a	data b	data a
H	H	L	data a	data b	data b
X	X	H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM, 'F712A/'F712-1



FUNCTION TABLE for 'F712A/'F712-1

INPUTS					OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	data a	data b	data c	data a
H	L	data a	data b	data c	data b
X	H	data a	data b	data c	data c

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	'F711A, 'F712A	96	mA
		'F711-1, 'F712-1	10	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OL}	High-level output current				-15	mA
I_{OL}	Low-level output current	'F711A, 'F712A			64	mA
		'F711-1, 'F712-1			5	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}= -3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH}= -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	'F711A/ 'F712A only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= MAX	±10%V_{CC}		0.38	0.55	V
				I_{OL}= 5mA	±5%V_{CC}		0.42	0.55	V
		'F711-1/ 'F712-1			±10%V_{CC}		0.38	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					-20	µA
		D_n only						-40	µA
I_{OZH}	Off-state output current High-level voltage applied	'F711A/ 'F711-1 only	V_{CC} = MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	'F711-1/ 'F712-1	V_{CC} = MAX			-60		-150	mA
I_O	Output current[4]	'F711A/ 'F712A	V_{CC} = MAX, V_O= 2.25V			-60		-150	mA
I_{CC}	Supply current (total)	'F711A	I_{CCH}	V_{CC} = MAX			25	35	mA
			I_{CCL}				33	46	mA
			I_{CCZ}				27	40	mA
		'F711-1	I_{CCH}	V_{CC} = MAX			26	40	mA
			I_{CCL}				33	45	mA
			I_{CCZ}				28	45	mA
		'F712A	I_{CCH}	V_{CC} = MAX			20	27	mA
			I_{CCL}				30	40	mA
		'F712-1	I_{CCH}	V_{CC} = MAX			20	30	mA
			I_{CCL}				29	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

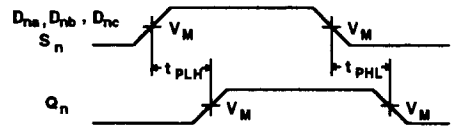
AC ELECTRICAL CHARACTERISTICS for 74F711A/74F711-1

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	74F711A	Waveform 1, 2	2.5 2.5	5.0 4.0	7.5 7.0	2.0 2.0	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S to Q_n		Waveform 1,3	7.0 5.0	9.0 8.0	12.0 11.0	5.5 4.5	13.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{INV}$ to Q_n		Waveform 1,3	6.0 4.0	9.0 8.0	12.5 11.0	5.0 3.5	14.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.5 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 8.0	2.0 2.5	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	74F711-1	Waveform 1, 2	3.0 2.0	4.5 4.5	7.5 7.5	2.0 2.5	9.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S, $\overline{INV}$ to Q_n		Waveform 1,3	6.5 4.5	10.0 8.5	13.5 11.5	5.5 4.0	14.5 12.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	9.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.0 3.5	4.5 5.5	7.0 8.5	2.0 3.0	8.0 9.5	ns

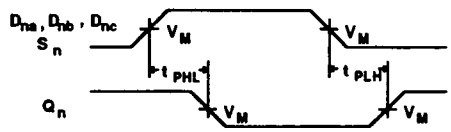
AC ELECTRICAL CHARACTERISTICS for 74F712A/74F712-1

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	74F712A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n		Waveform 1	6.5 5.0	8.0 7.5	11.5 10.0	5.5 4.5	13.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	74F712-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n		Waveform 1	7.0 5.5	9.0 7.5	12.0 10.5	6.0 5.5	13.5 11.0	ns

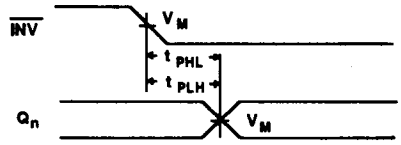
AC WAVEFORMS



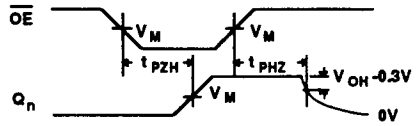
Waveform 1. Propagation Delay For Non-Inverting Output



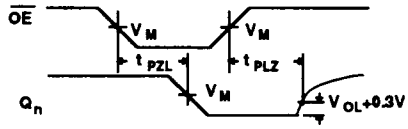
Waveform 2. Propagation Delay For Inverting Output



Waveform 3. Propagation Delay For $\overline{INV}$ To Output



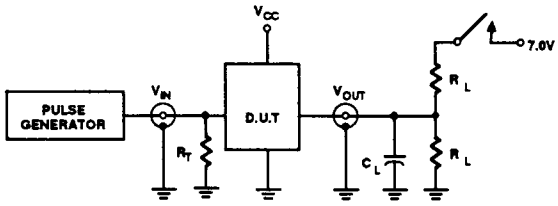
Waveform4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

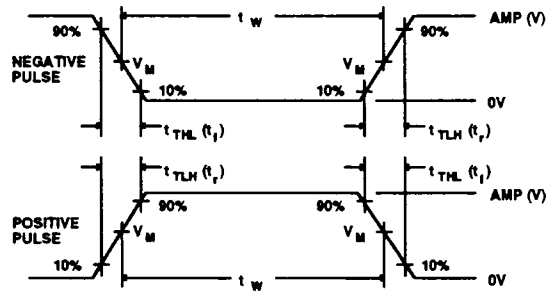
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns