Philips Semiconductors-Signetics

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FAST Products	

FAST 74F732, 74F733 Multiplexers

74F732 Quad Data Multiplexer, Inverting (3-State)
74F733 Quad Data Multiplexer, Non-Inverting (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F732	6.0ns	65mA
74F733	6.0ns	75mA

FEATURES

- **Quad 2-to-1 Multiplexer (two busses to one bus)**
- **Data can flow in either direction between busses (A → B, A → C, B → C, B → A, C → A, C → B)**
- **A built-in "break-before-make" feature eliminates current glitches and simplifies PC board design**
- **Output Enable for each bus to allow flexible contention control**
- **3-State outputs sink 64mA**

DESCRIPTION

The 74F732/74F733 are Quad Data Multiplexers designed to provide a simple means to control the flow of bidirectional data between three data busses.

The 74F732/74F733 consist of four multiplexers. Each multiplexer has three I/O (A_n, B_n, C_n) pins and uses one Output Enable pin ($\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$). There are two Select (S_0, S_1) pins and a Direction (DIR) pin to control data flow paths for all four multiplexers.

ORDERING INFORMATION

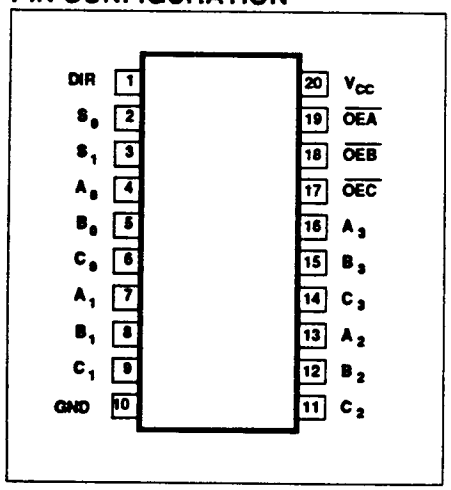
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F732N, N74F733N
20-Pin Plastic SOL	N74F732D, N74F733D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

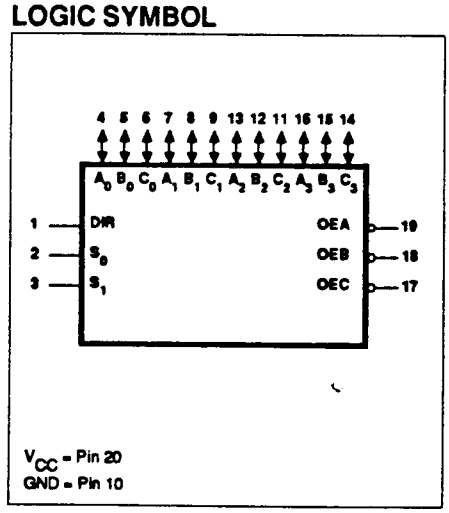
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data inputs for Bus A	3.5/1.0	70µA/0.6mA
B_0 - B_3	Data inputs for Bus B	3.5/1.0	70µA/0.6mA
C_0 - C_3	Data inputs for Bus C	3.5/1.0	70µA/0.6mA
DIR	Direction control input	1.0/1.0	20µA/0.6mA
S_0, S_1	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$	Output Enable inputs (Active Low)	1.0/1.0	20µA/0.6mA
A_0 - A_3	Data output for Bus A	750/106.7	15mA/64mA
B_0 - B_3	Data output for Bus B	750/106.7	15mA/64mA
C_0 - C_3	Data output for Bus C	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

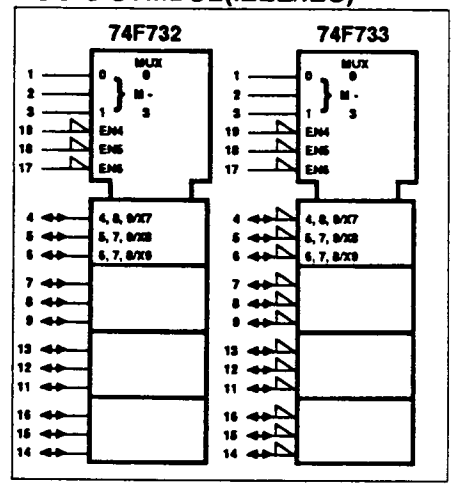
PIN CONFIGURATION



LOGIC SYMBOL

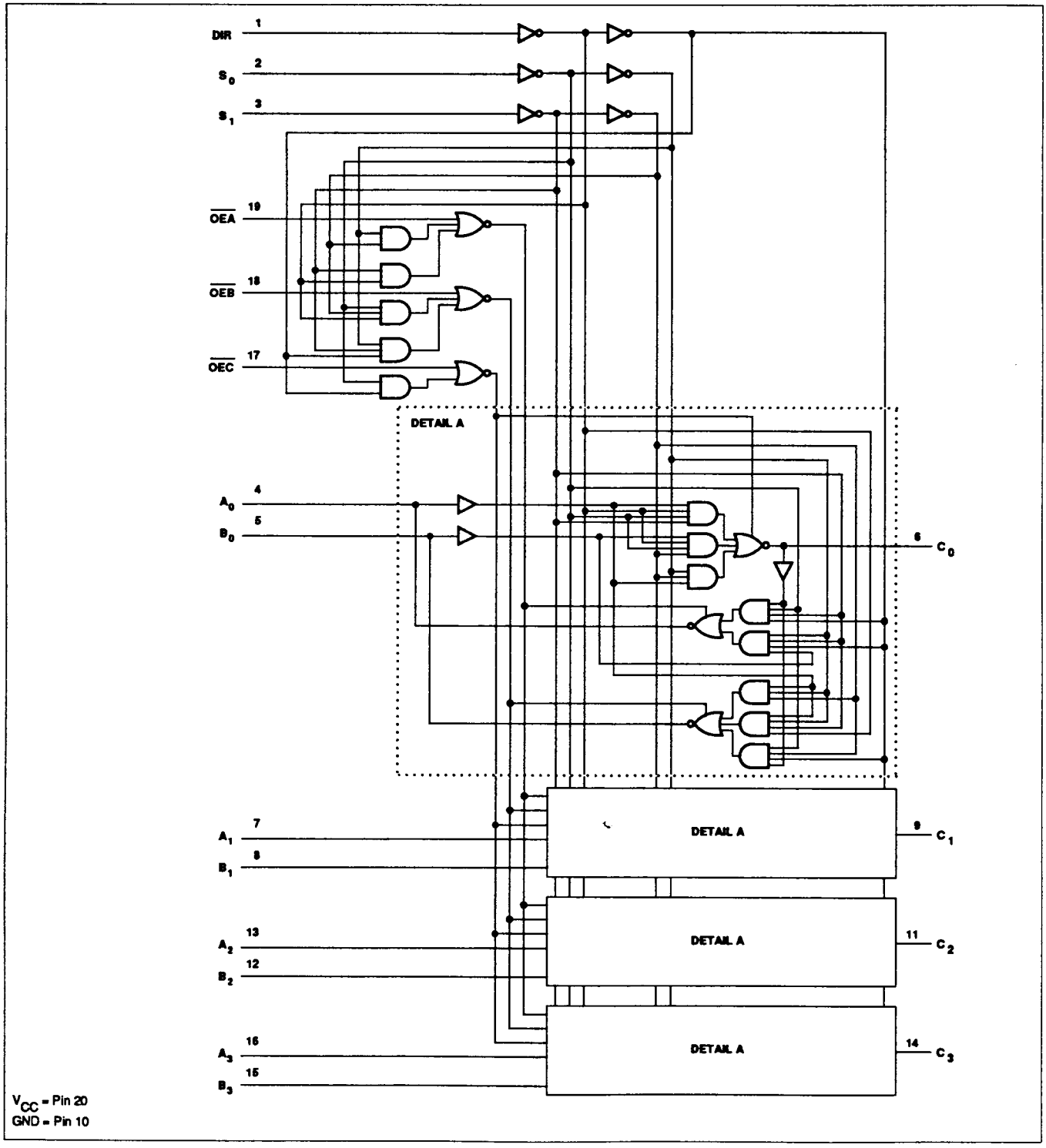


LOGIC SYMBOL(IEEE/IEC)

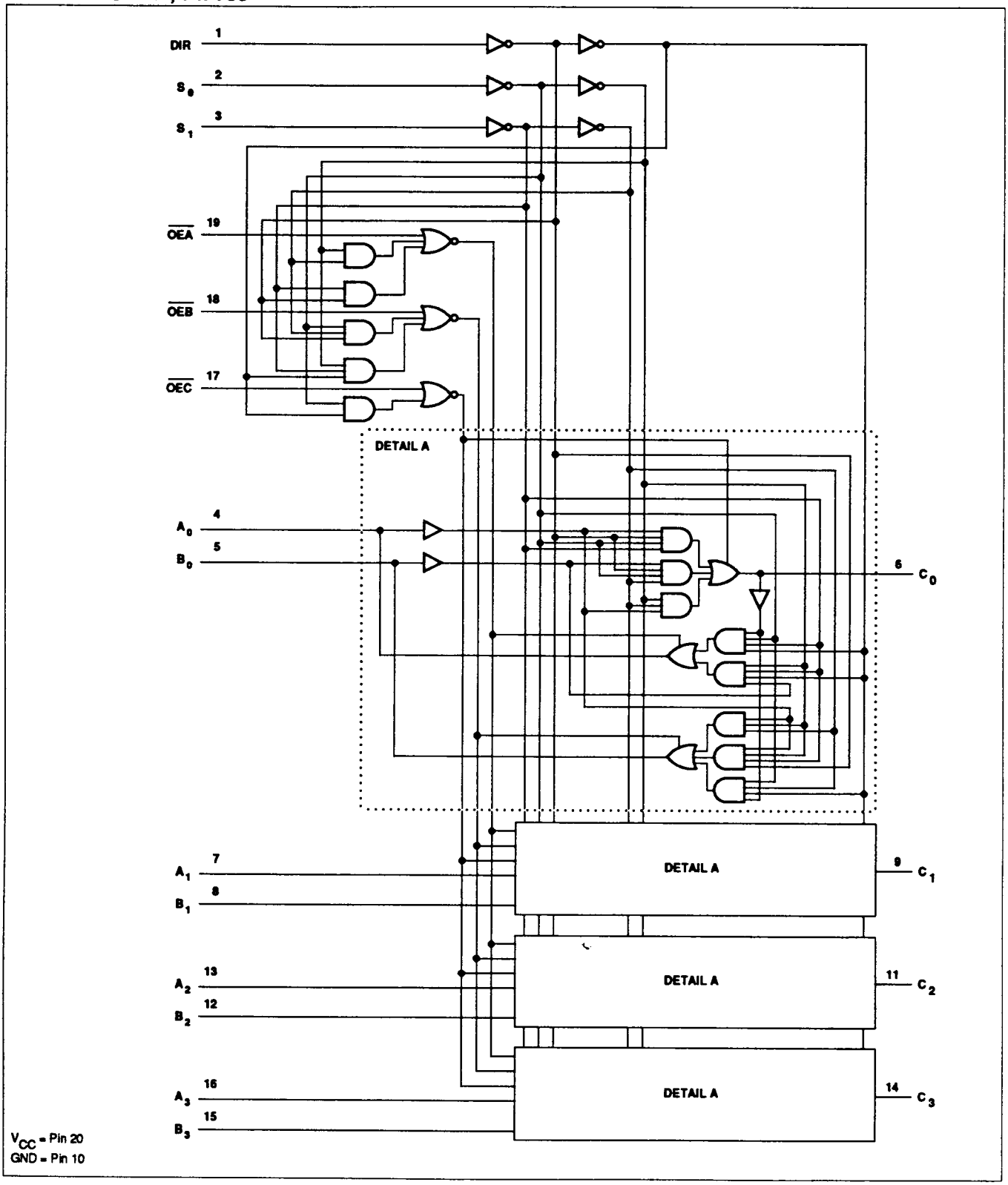


With the Select control, data can flow in the following directions between busses: A to B, A to C, B to A, B to C, C to B, A to B and C. A built-in "break-before-make" feature eliminates current glitches common to systems using 3-State transceivers to accomplish the same function.

LOGIC DIAGRAM, 74F732



LOGIC DIAGRAM, 74F733



FUNCTION TABLE

INPUTS						OPERATING MODE
DIR	S_0	S_1	$\overline{OEA}$	$\overline{OEB}$	$\overline{OEC}$	
X	X	X	H	X	X	Bus A disabled except for input
X	X	X	X	H	X	Bus B disabled except for input
X	X	X	X	X	H	Bus C disabled except for input
L	L	L	X	H*	L	Data flow from Bus A to Bus C
H	L	L	L	H*	X	Data flow from Bus C to Bus A
L	L	H	H*	X	L	Data flow from Bus B to Bus C
H	L	H	H*	L	X	Data flow from Bus C to Bus B
L	H	L	X	L	H*	Data flow from Bus A to Bus B
H	H	L	L	X	H*	Data flow from Bus B to Bus A
X	H	H	X	L	L	Data flow from Bus A to Bus B and Bus C
X	H	H	X	H	L	Data flow from Bus A to Bus C
X	H	H	X	L	H	Data flow from Bus A to Bus B

H = High voltage level
L = Low voltage level
X = Don't care
* = If this is not High then the corresponding outputs will be High (74F732) or Low (74F733)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.4		V
				I_{OH} = -15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ DIR, S_0, S_1	V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ DIR, S_0, S_1	V_{CC} = MAX, V_I = 0.5 V					-0.6	mA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_3 B_0 - B_3 C_0 - C_3	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_3 B_0 - B_3 C_0 - C_3	V_{CC} = MAX, V_O = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F732	I_{CCH}	V_{CC} = MAX			55	80	mA
			I_{CCL}				75	105	mA
			I_{CCZ}				65	100	mA
		74F733	I_{CCH}	V_{CC} = MAX			70	100	mA
			I_{CCL}				80	115	mA
			I_{CCZ}				80	110	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F732

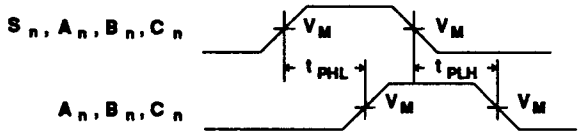
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to A_n, B_n, C_n	Waveform 1, 2	2.0 1.0	4.5 3.0	8.0 6.0	2.0 1.0	8.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (NINV)	Waveform 1	4.5 4.5	7.0 7.0	10.0 10.0	4.0 4.0	11.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (INV)	Waveform 2	5.0 2.5	7.0 4.5	10.0 7.5	4.5 2.5	10.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 4.0	4.5 6.5	7.5 9.5	1.5 3.5	8.5 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	7.0 7.0	1.5 2.0	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	4.0 5.5	7.5 8.5	11.0 11.5	3.0 5.0	13.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	1.0 1.0	6.0 4.5	9.0 7.5	1.0 1.0	10.0 8.0	ns

AC ELECTRICAL CHARACTERISTICS for 74F733

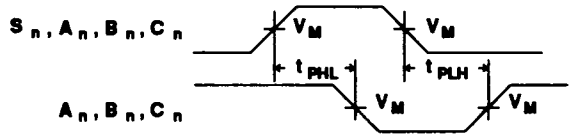
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to A_n, B_n, C_n	Waveform 1, 2	1.5 1.5	4.0 4.0	7.0 7.0	1.0 1.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (NINV)	Waveform 1	3.0 4.0	5.0 6.0	7.5 9.0	2.5 3.5	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (INV)	Waveform 2	5.0 3.0	7.5 5.0	10.5 8.0	4.5 3.0	13.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.5 3.5	5.0 5.5	7.5 8.5	2.0 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 2.0	4.0 4.5	7.0 7.0	1.5 2.0	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	4.5 5.5	7.5 8.5	11.0 12.0	4.0 5.0	13.0 13.5	ns
t_{PHZ}* t_{PLZ}*	Output Disable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	1.5 7.0	4.5 11.5	7.5 14.5	1.0 7.0	8.0 16.0	ns

* Because of the 3-state output characteristics, the pick-off point is V_{OL} +0.8V.

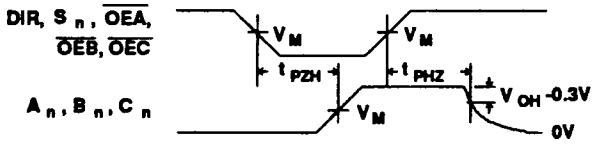
AC WAVEFORMS



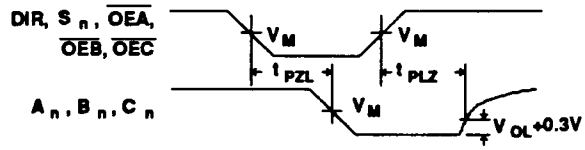
Waveform 1. Propagation Delay, Select And Data Busses



Waveform 2. Propagation Delay, Select And Data Busses



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

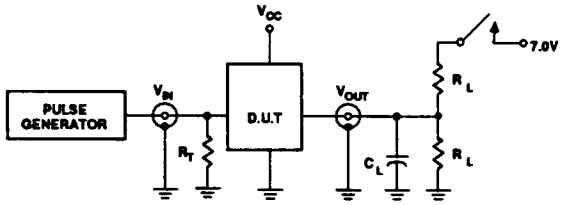


Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

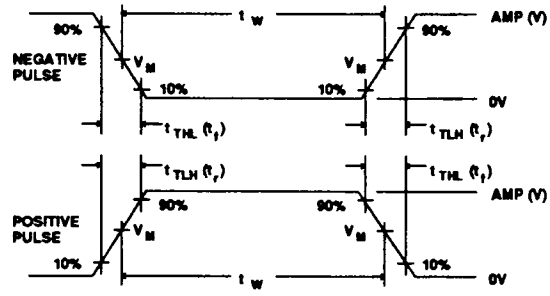
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns