AMD 80EC287™

Enhanced 80-Bit CMOS Math Coprocessor

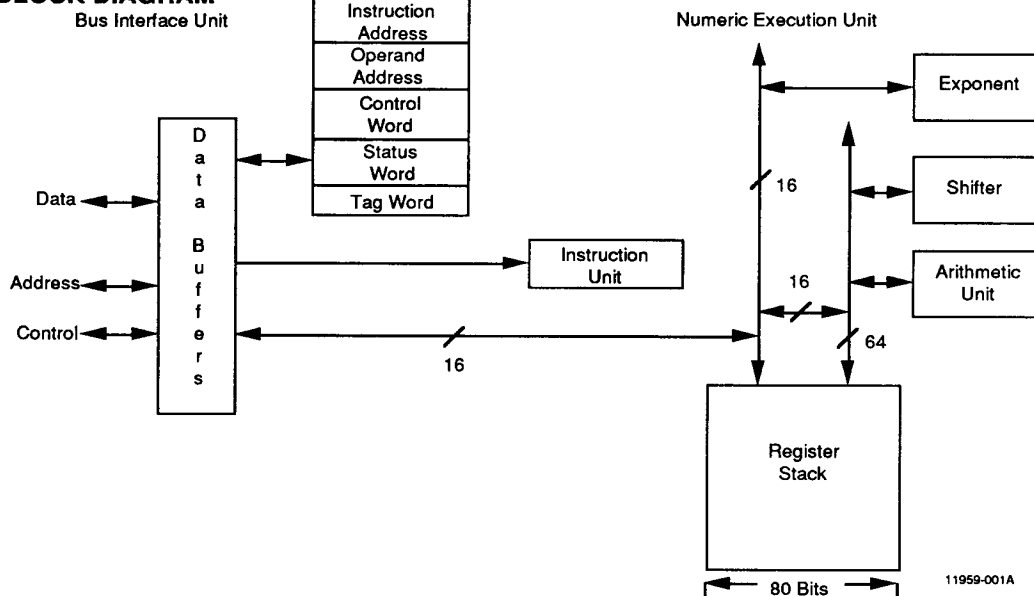## DISTINCTIVE CHARACTERISTICS

- Pin compatible and functionally equivalent to the Intel 80287

- High-performance CMOS process yields 10-, and 12-MHz speed grades

- Enhanced sleep feature automatically shuts off the internal clock when no instruction is executing, reducing power consumption. This feature is transparent to the user

- Available in space-saving 44-pin PLCC as well as 40-pin DIP

- 80-bit numeric accelerator for 80C286- and 80286-based systems

- Compatible with IEEE floating point Standard 754

- Static CMOS design does not require a minimum clock rate, resulting in significantly lower power dissipation

- Performs single-, double-, and extended-precision floating point, as well as word, short, and long integer and 18-digit BCD conversions

- Adds trigonometric, logarithmic, exponential, and arithmetic instructions to the 80C286 instruction set
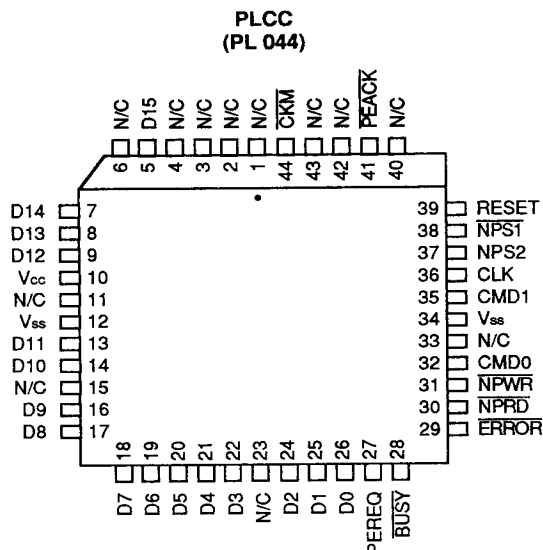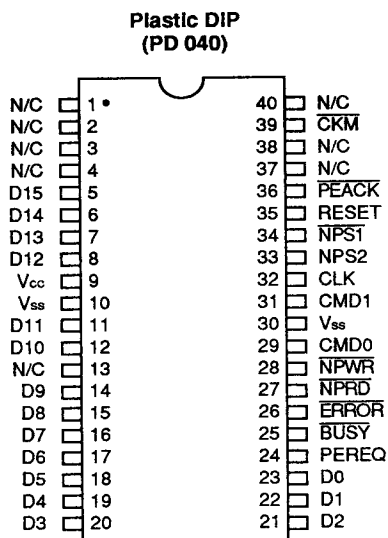
GENERAL DESCRIPTION

The AMD 80EC287 processor is implemented in AMD's advanced static CMOS process that allows for significantly higher speeds at a much lower power dissipation than traditional NMOS versions or standard CMOS. The AMD 80EC287 processor is a high-performance arithmetic processor that expands the 80C286 instruction set with floating-point instructions including transcendentals, and integer and BCD conversions. The AMD 80EC287 processor is functionally equivalent to the Intel 80287 and AMD 80C287 math coprocessor plus adds a low-power sleep feature for battery powered applications. This enhanced AMD 80EC287 processor can be a direct replacement for an AMD 80C287 processor. The sleep feature is an automatic inherent feature of the device and thus requires no external entry. The floating point operations comply with the IEEE Standard 754. The device is available in 10- and 12-MHz speed grades and is provided in 44-pin PLCC and 40-pin DIP packages. When coupled with the 80C286, the AMD 80EC287 processor provides a complete solution for high-performance numeric processing applications.

BLOCK DIAGRAM

CONNECTION DIAGRAMS

Plastic DIP (PD 040)

N/C	1 •		40	N/C
N/C	2		39	$\overline{CKM}$
N/C	3		38	N/C
N/C	4		37	N/C
D15	5		36	$\overline{PEACK}$
D14	6		35	RESET
D13	7		34	$\overline{NPS1}$
D12	8		33	NPS2
Vcc	9		32	CLK
Vss	10		31	CMD1
D11	11		30	Vss
D10	12		29	CMD0
N/C	13		28	$\overline{NPWR}$
D9	14		27	$\overline{NPRD}$
D8	15		26	$\overline{ERROR}$
D7	16		25	$\overline{BUSY}$
D6	17		24	PEREQ
D5	18		23	D0
D4	19		22	D1
D3	20		21	D2

PLCC (PL 044)

D14	7		39	RESET
D13	8		38	$\overline{NPS1}$
D12	9		37	NPS2
Vcc	10		36	CLK
N/C	11		35	CMD1
Vss	12		34	Vss
D11	13		33	N/C
D10	14		32	CMD0
N/C	15		31	$\overline{NPWR}$
D9	16		30	$\overline{NPRD}$
D8	17		29	$\overline{ERROR}$

Top pins: N/C, D15, N/C, N/C, N/C, N/C, $\overline{CKM}$, N/C, N/C, $\overline{PEACK}$, N/C (pins 6,5,4,3,2,1,44,43,42,41,40)

Bottom pins: D7, D6, D5, D4, D3, N/C, D2, D1, D0, PEREQ, $\overline{BUSY}$ (pins 18,19,20,21,22,23,24,25,26,27,28)

Notes: N/C pins should not be connected.
Pin 1 is marked for orientation

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PIN DESCRIPTION

$\overline{BUSY}$
Busy Status (Output; Active Low)

A Low level indicates that the AMD 80EC287 math coprocessor is currently executing a command.

CKM
Clock Mode Signal (Input)

When CKM is High, the CLK is used directly. When CKM is Low, CLK is divided by three. This input must be either High or Low 20-CLK cycles before RESET goes Low.

CLK
Clock (Input)

Provides timing for AMD 80EC287 math coprocessor operations.

CMD1, CMD0
Command Lines (Inputs)

CMD1 and CMD0, along with select inputs, allow the CPU to direct the AMD 80EC287 math coprocessor operations. These inputs are timed relative to the read and write strobes.

D15–D0
Data (Inputs/Outputs)

Bi-directional data bus. These inputs are timed relative to the read and write strobes.

$\overline{ERROR}$
Error Status (Output; Active Low)

Reflects the error summary status bit of the status word. A Low level indicates that an unmasked exception condition exists.

$\overline{NPRD}$
Numeric Processor Read (Input; Active Low)

A Low level enables transfer of data from the AMD 80EC287 math coprocessor. This input may be asyn-chronous to the AMD 80EC287 clock.

$\overline{NPS1}$, NPS2
Numeric Processor Selects (Inputs)

Indicates the CPU is transferring data to and from the AMD 80EC287 math coprocessor. Asserting both signals ($\overline{NPS1}$ Low and NPS2 High) enables the AMD 80EC287 math coprocessor to transfer floating-point data or instructions. No data transfers involving the AMD 80EC287 math coprocessor will occur unless the AMD 80EC287 math coprocessor is selected via $\overline{NPS1}$ and NPS2. These inputs are timed relative to the read and write strobes.

$\overline{NPWR}$
Numeric Processor Write (Input; Active Low)

A Low level enables transfer of data to the AMD 80EC287 math coprocessor. This input may be asynchronous to the AMD 80EC287 clock.

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PEACK
Processor Extension Acknowledge
(Input; Active Low)

A Low level indicates that the request signal (PEREQ) has been recognized. PEACK causes the request (PEREQ) to be withdrawn when no more transfers are required. PEACK may be asynchronous to the AMD 80EC287 clock.

PEREQ
Processor Extension Request (Output)

A High level indicates that the AMD 80EC287 math coprocessor is ready to transfer data. PEREQ will be disabled upon assertion of PEACK or upon actual data transfer, whichever occurs first, when no more transfers are required.

RESET
System Reset (Input)

Reset causes the AMD 80EC287 math coprocessor to immediately terminate its present activity and enter a dormant state. Reset must be High for more than four CLK cycles. For proper initialization the High-Low transition must occur no sooner than 50 μs after V_{CC} and CLK meet their DC and AC specifications.

V_{cc}
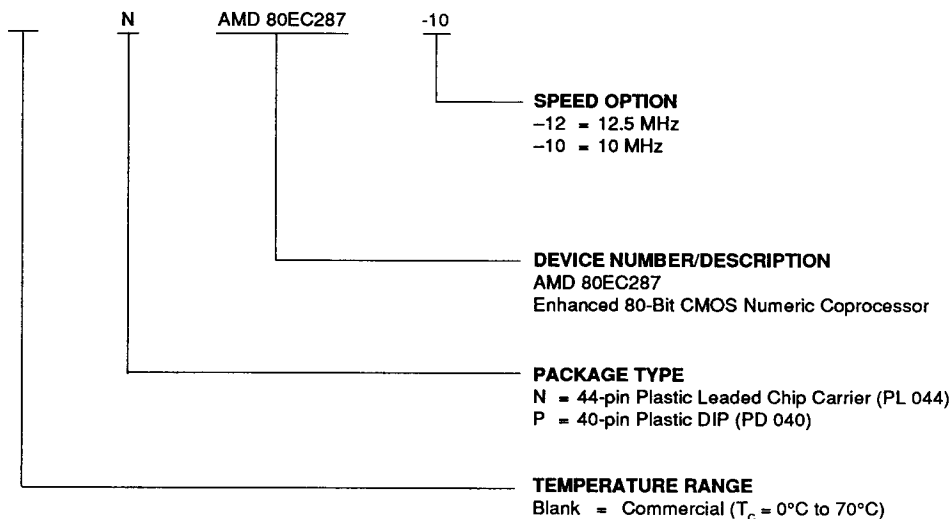## +5 V Supply (Input)

V_{ss}
System Ground (Input)

Both pins must be connected to ground.

ORDERING INFORMATION

Commodity Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

```
N        AMD 80EC287        -10
```

SPEED OPTION
-12 = 12.5 MHz
-10 = 10 MHz

DEVICE NUMBER/DESCRIPTION
AMD 80EC287
Enhanced 80-Bit CMOS Numeric Coprocessor

PACKAGE TYPE
N = 44-pin Plastic Leaded Chip Carrier (PL 044)
P = 40-pin Plastic DIP (PD 040)

TEMPERATURE RANGE
Blank = Commercial (T_c = 0°C to 70°C)

Valid Combination	
N, P	AMD 80EC287 –12
	AMD 80EC287 –10

Valid Combination

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released valid combinations.

SIMPLIFIED FUNCTIONAL DESCRIPTION

The AMD 80EC287 numeric processor is internally divided into two basic processing units: the numeric execution unit, and the bus interface unit as shown in the block diagram. The numeric execution unit performs numeric instructions. The bus interface unit receives and decodes instructions, executes processor control instructions, and requests operands transfers to and from memory. The 80C286 may execute non-numeric instruction concurrently with numeric instruction executed on the AMD 80EC287 processor. Synchronization and error recognition occurs when the next numeric instruction is decoded by the 80C286.

The Numeric Execution Unit

The numeric execution data path is 80-bits wide. All operands are converted to the internal 80-bit format before use. These instructions include arithmetic, transcendental, constant, and data transfer instructions.

The Bus Interface Unit

The Bus Interface Unit decodes the ESC instruction executed by the 80C286. The signal $\overline{BUSY}$ is activated for AMD 80C286/80EC287 processor synchronization and the signal $\overline{ERROR}$ is activated for error detection. $\overline{BUSY}$ is activated when an instruction is transferred and deactivated when the instruction completes. $\overline{ERROR}$ will be asserted if an error has occurred when $\overline{BUSY}$ is deactivated.

The signals PEREQ, $\overline{PEACK}$, $\overline{NPRD}$, $\overline{NPWR}$, $\overline{NPS1}$, CMD0, CMD1, and NPS2 control data transfers between the AMD 80EC287 processor and the 80C286. The 80C286 performs the actual data transfer with memory.

The Register Stack

The register stack contains eight 80-bit data registers, organized as a push down stack. Operations are performed on the stack top, between the stack top and another register, or between the stack top and memory.

System Configuration with 80C286

A simplified block diagram of the AMD 80EC287 processor interface to a 80C286 CPU is shown in Figure 1. The AMD 80EC287 processor can operate concurrently with the host CPU. The signals PEREQ, $\overline{PEACK}$, $\overline{BUSY}$, $\overline{NPRD}$, $\overline{NPWR}$, CMD0, and CMD1 allow the AMD 80EC287 processor to receive instructions and data from the 80C286. Detection of errors are indicated to the CPU by asserting the signal $\overline{ERROR}$. The address decode logic, bus control and timing logic is shown in this implementation using AMD PAL® devices but may also be accomplished using standard chip sets.

The AMD 80EC287 processor operates either directly from the CPU clock or with a dedicated clock. The AMD 80EC287 processor functions at two-thirds the frequency of the 80C286 when operating with the CPU clock (i.e., for a 16-MHz 80C286, the 32-MHz clock is divided down to 10.6 MHz).

Sleep Feature

The AMD 80EC287 processor clock runs only while an instruction is executing. The internal clock shuts itself off when no instruction is executing, thus reducing power consumption. This feature is completely transparent to the user and requires no external circuitry or design interface.
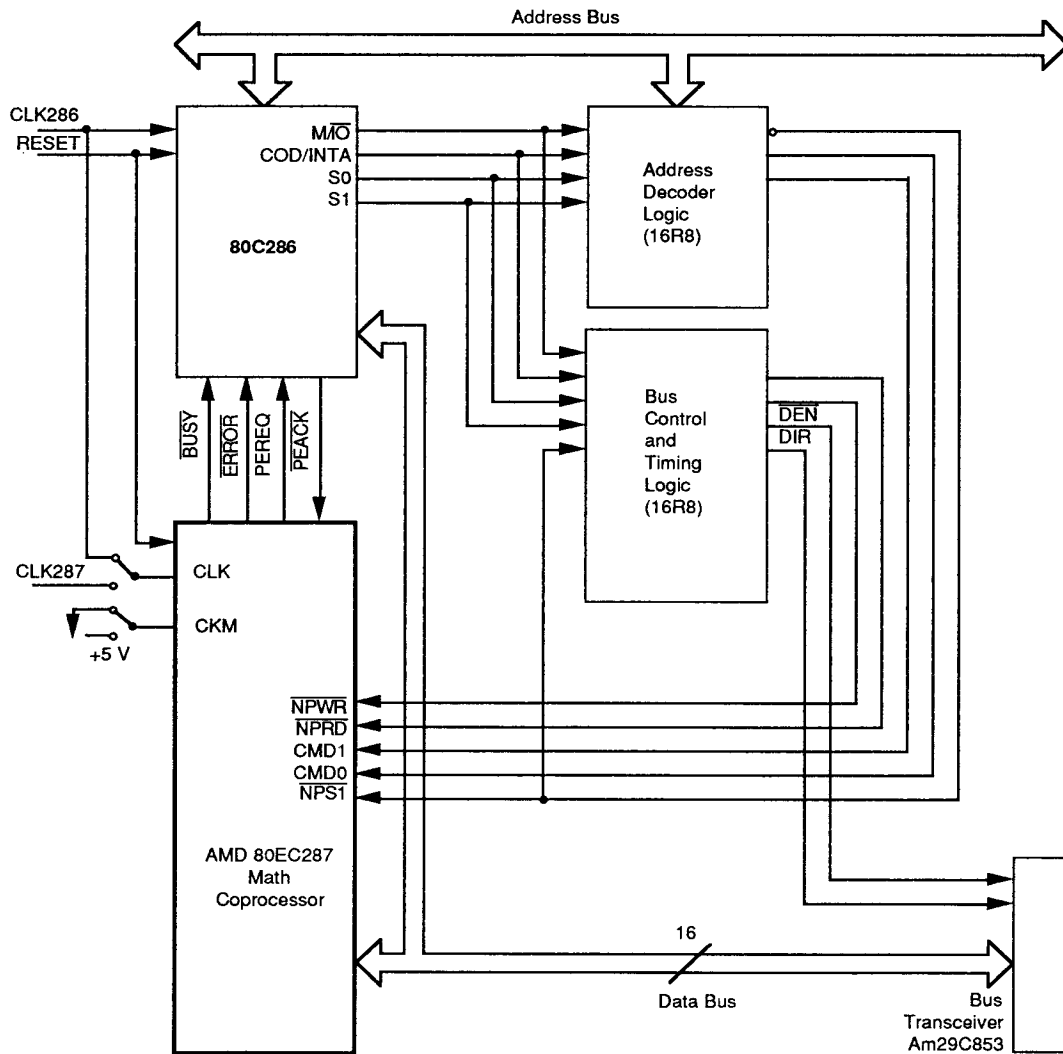
Address Bus

Figure 1. AMD 80C286/80EC287 Simplified System
Configuration

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AMD 80EC287 Processor

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ....−65°C to +150° C
Ambient Temperature Under Bias ....−55°C to +125° C
Supply Voltage to Ground Potential
    Continuous ....−1.0 to +7.0 V
DC Voltage Applied to Outputs
    for High Output State ....−0.3 V to + V_{CC} +0.3 V
DC Input Voltage ....−0.3 to V_{CC} +0.3 V
DC Output Current, into Low Outputs ....30 mA
DC Input Current ....−10 to +10 mA
Power Dissipation (Max) ....0.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect devices reliability.

OPERATING RANGES

Commercial (C) Devices
    Temperature, Ambient (T_A) ....0°C to +70°C
    (also meets 0 to 100°C Case Temperature (T_c) for
    laptop requirements)
    Supply Voltage (V_{CC}) ....+ 4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min V_{IN} = V_{IL} or V_{IH}	I_{OH} = −0.4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min V_{IN} = V_{IL} or V_{IH}	I_{OL} = 3 mA		0.45	
V_{IH}	Guaranteed Input Logical High Voltage (Note 1)			2.0	V_{CC} +0.5	V
V_{IL}	Guaranteed Input Logical Low Voltage (Note 1)			−0.5	0.8	V
V_{IHC}	Clock Input High Voltage CKM = 1			2.0	V_{CC} +1.0	V
	CKM = 0			3.8	V_{CC} +1.0	V
V_{ILC}	Clock Input Low Voltage CKM = 1 CKM = 0			−0.5 −0.5	0.8 0.6	V V
I_{LI}	Input Leakage Current	0 V ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZH}	Off-State (High Impedance) Output Current	V_{CC} = Max, V_O = 2.4 V			10	µA
I_{OZL}	Off-State (High Impedance) Output Current	V_{CC} = Max, V_O = 0.45 V			−10	µA
I_{CCS}	Power Supply Current, Static	V_{CC} = Max, V_{IN} − V_{CC} or GND, I_O= 0 µA		20 mA		
I_{CCD}	Supply Current, operating	V_{CC} = Max Outputs Unloaded		10 mA + 5 mA/MHz (Note 2)		
Icc_{SM}	Power Supply Current, Sleep Mode	V_{CC} = Max Outputs Unloaded		10 mA + 1 mA/MHz		

Notes: 1. These input levels provide zero-noise immunity and should only be statically tested in a noise-free environment (not functionally tested).
     2. This reduces to I_{CCSM} when no instruction is executing, reducing overall power consumption.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

| No.	Parameter Description	Test Conditions	AMD 80EC287-10		AMD 80EC287-12		Unit
			Min	Max	Min	Max	
1	Clock Period						
	CKM = 1		100		80		ns
	CKM = 0		32		26		ns
2	Clock Low Time						
	CKM = 1		45		35		ns
	CKM = 0		11		9		ns
3	Clock High Time						
	CKM = 1		28		22		ns
	CKM = 0		11		9		ns
4	Clock Rise Time			10		8	ns
5	Clock Fall Time			10		8	ns
6	Data Setup to NPWR Inactive		75		75		ns
7	Data Hold from NPWR Inactive		18		10		ns
8	NPWR, NPRD Active Time		90		70		ns
9	Command Valid Setup Time		0		0		ns
10	PEREQ Active to NPRD Active		100		80		ns
11	PEACK Active Time		60		50		ns
12	PEACK Inactive Time		200		160		ns
13	PEACK Inactive to NPRD, NPWR Inactive		40		32		ns
14	NPRD, NPWR Inactive to PEACK Active		–30		–30		ns
15	Command Valid Hold Time		22		18		ns
16	PEACK Active Setup to NPRD, NPWR		40		30		ns
17	NPRD, NPWR to CLK Setup		53		40		ns
18	NPRD, NPWR CLK Hold		37		29		ns
19	RESET to CLK Setup		20		20		ns
20	RESET from CLK Hold		20		20		ns
21	NPRD Inactive to Data Float			21		17	ns
22	NPRD Active to Data Valid			60		50	ns
23	ERROR Active to BUSY Inactive		100		100		ns
24	NPWR, Active to BUSY Active			100		80	ns
25	PEACK Active to PEREQ Inactive			100		80	ns
26	NPRD, NPWR Active to PEREQ Inactive			100		80	ns
27	Command Inactive Time						
	Write to Write		75		60		ns
	Read to Read		75		60		ns
	Write to Read		75		60		ns
	Read to Write		75		60		ns
28	Data Hold from Time NPRD Inactive		3		1		ns

SWITCHING WAVEFORMS
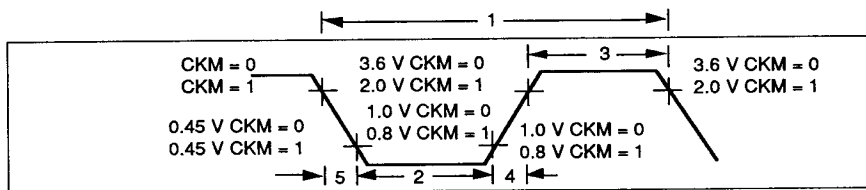
AC Drive and Measurement Points—CLK Input
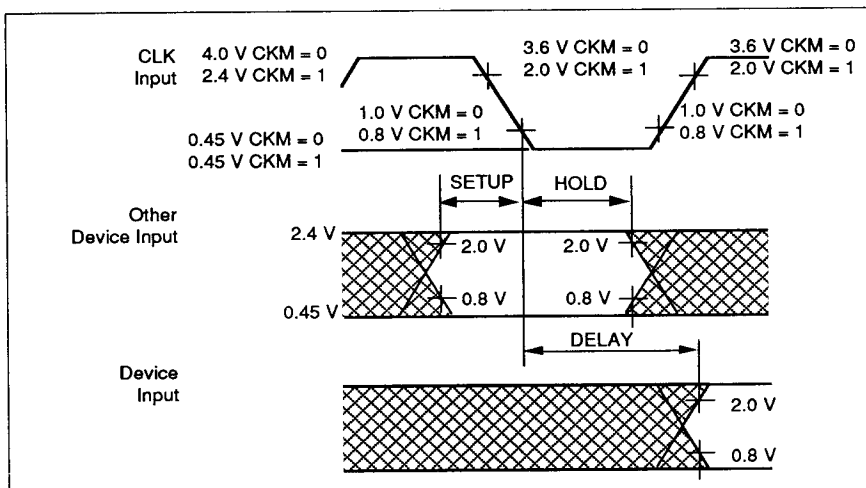
AC Setup, Hold and Delay Time Measurement—General
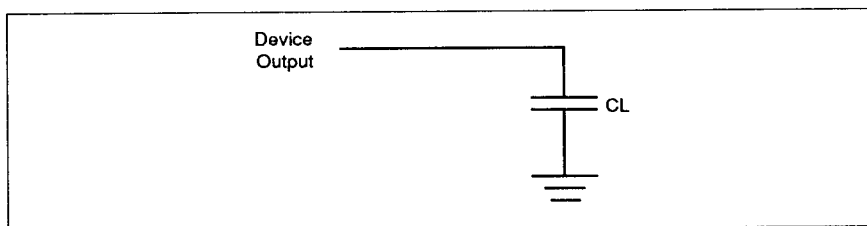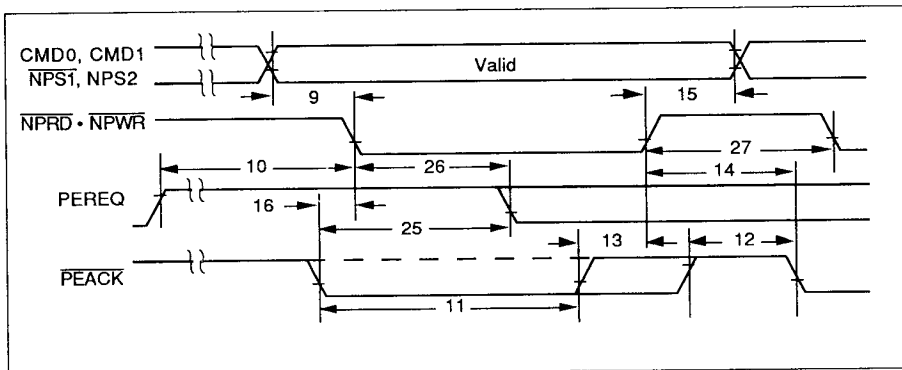

AC Test Loading on Outputs

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AMD 80EC287 Processor

SWITCHING WAVEFORMS (continued)
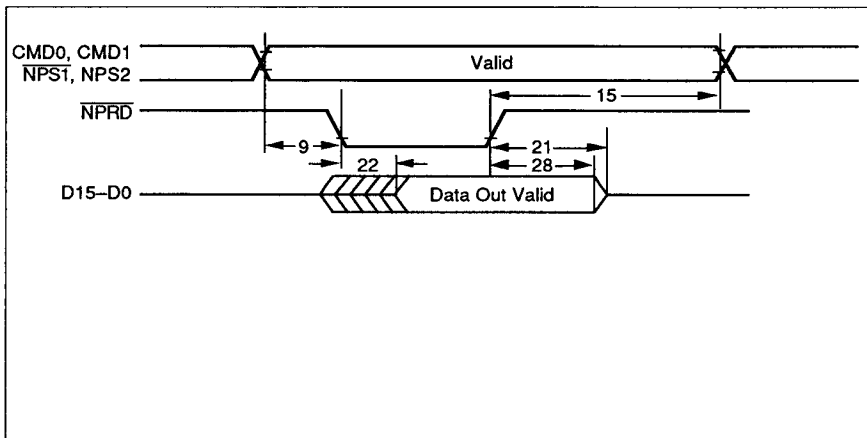
Read Timing from AMD 80EC287 Processor
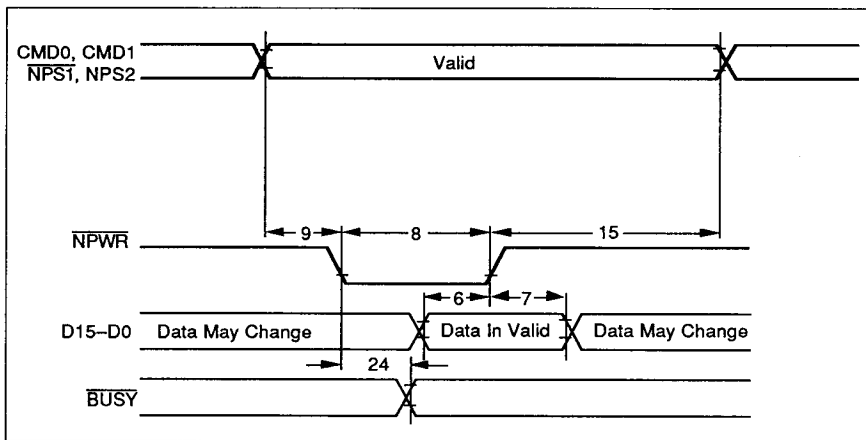
Write Timing from AMD 80EC287 Processor

11959-005

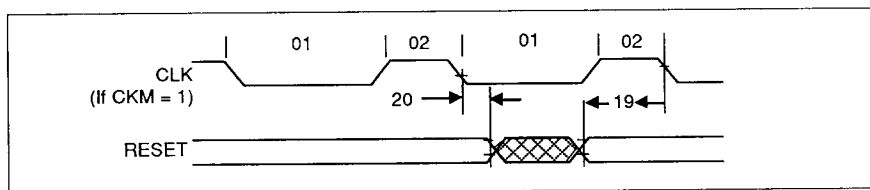**AMD 80EC287 Processor**

SWITCHING WAVEFORMS (continued)

Data Channel Timing (Initiated by AMD 80EC287 Processor)
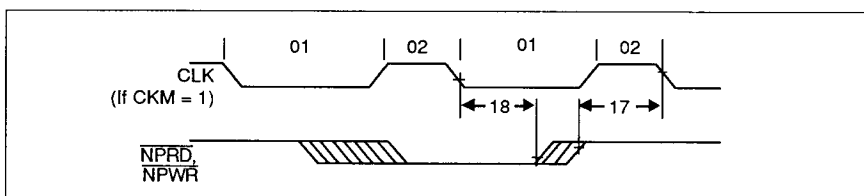
11959-006A
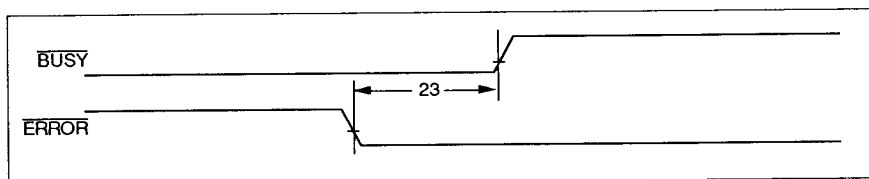
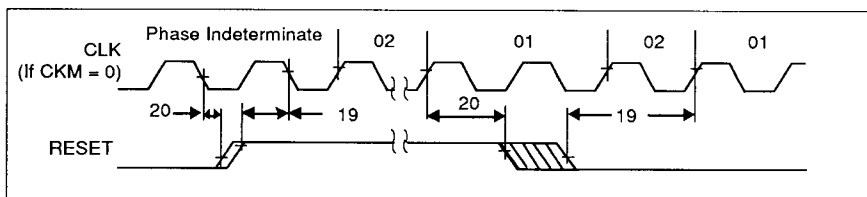**Error Output Timing**

CLK, Reset Timing (CKM = 1)

11959-007

Note: Reset, $\overline{NPWR}$, $\overline{NPRD}$ are inputs asynchronous to CLK. Timing requirements above are given for testing purposes only to assure recognition at a specific CLK edge.

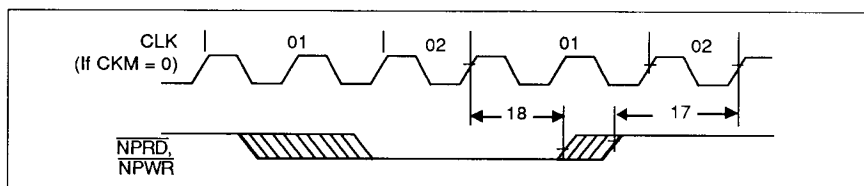## SWITCHING WAVEFORMS (continued)

CLK, $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Timing (CKM = 1)

CLK, RESET Timing (CKM = 0)

Note: Reset must meet timing shown to guarantee known phase of internal ÷ 3 circuit.

11959-008A

CLK, $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ Timing (CKM = 0)