82230/82231
HIGH INTEGRATION AT*-COMPATIBLE CHIP SET

- **Fully IBM PC-AT* System Compatible**
- **Two Chip Set Replaces the Major Logic Functions of the IBM PC-AT Motherboard Including the Functions of all the Microprocessor Peripherals:**
  - **— 8259A Programmable Interrupt Controller (Master)**
  - **— 8259A Programmable Interrupt Controller (Slave)**
  - **— 8254 Programmable Interval Timer**
  - **— 8284A Clock Generator**
  - **— 82284 Clock Generator & Ready Interface**
  - **— 82288 Bus Controller**
  - **— 8237 DMA Controller (2)**
  - **— 6818 Real Time Clock**
  - **— 74LS612 Memory Mapper**
- **Includes:**
  - **— Refresh Generation Logic**
  - **— Refresh/DMA Arbitration**
  - **— Address/Data Bus Control**
  - **— 16- to 8-Bit Conversion Logic**
- **Memory Refresh Controller Drives Up to 4 Mb DRAMs**
- **Numeric Processor Control Logic**
- **Up to 12 MHz System Clock Utilizing RAMs with Zero Wait States**
- **Single +5V Power Supply**
- **CHMOS Technology**
- **84 Pin PLCC Packages**
  (See Packaging Specification Order #231369-004)

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The 82230 and 82231 are a two-chip implementation of LSI/MSI/SSI logic controlling the IBM Personal Computer AT. The devices provide a low power, highly integrated PC-AT design solution that may be applied to any 80286-based system.

The 82230 performs the functions of the 82284 Clock Generator & Ready Interface, 82288 Bus Controller for 80286 processors, 6818 Real Time Clock/RAM, and the Master-Slave implementation of the dual 8259A Programmable Interrupt Controllers as well as Command Delay, Shut Down, Address/Data Bus Control and Ready Generation logic.

The 82231 includes the 8254 Programmable Interval Timer, 8284A Clock Generator, LS612 Memory Mapper and the dual 8237 DMA Controller functions as well as Refresh Generation and Refresh/DMA Arbitration Logic.

NOTE:
"+" and "−" in front of signal names is consistent with PC-AT Documentation.

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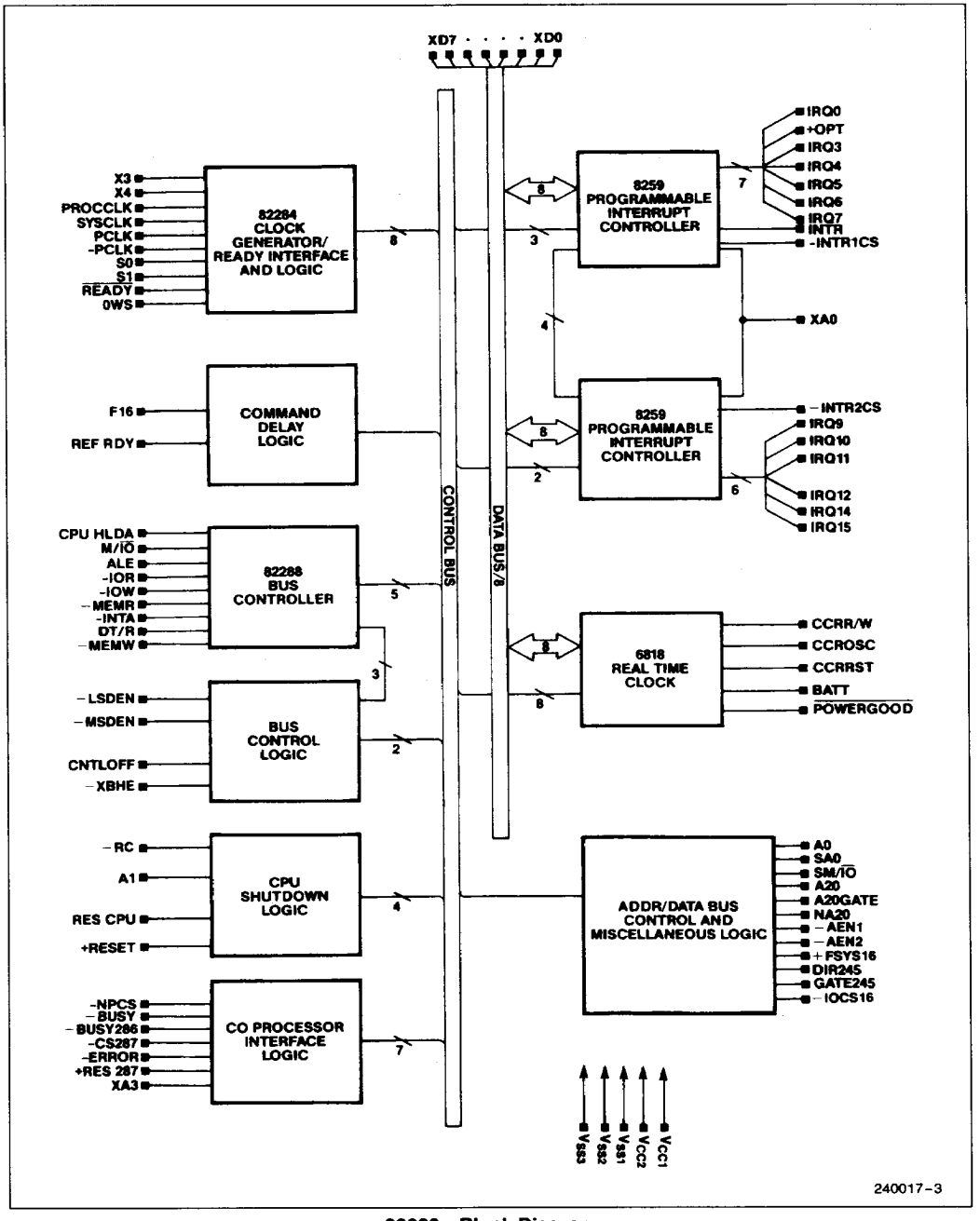
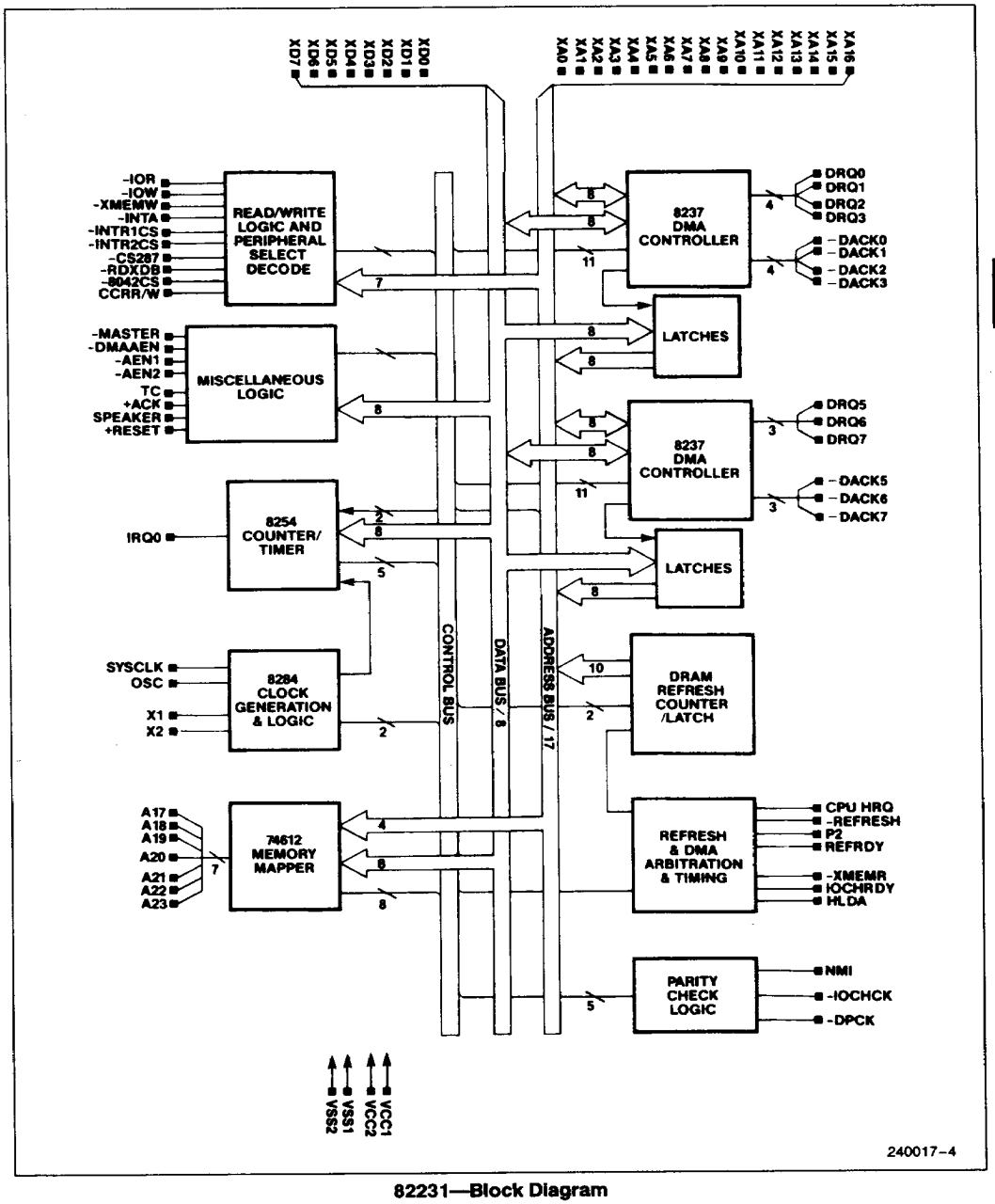
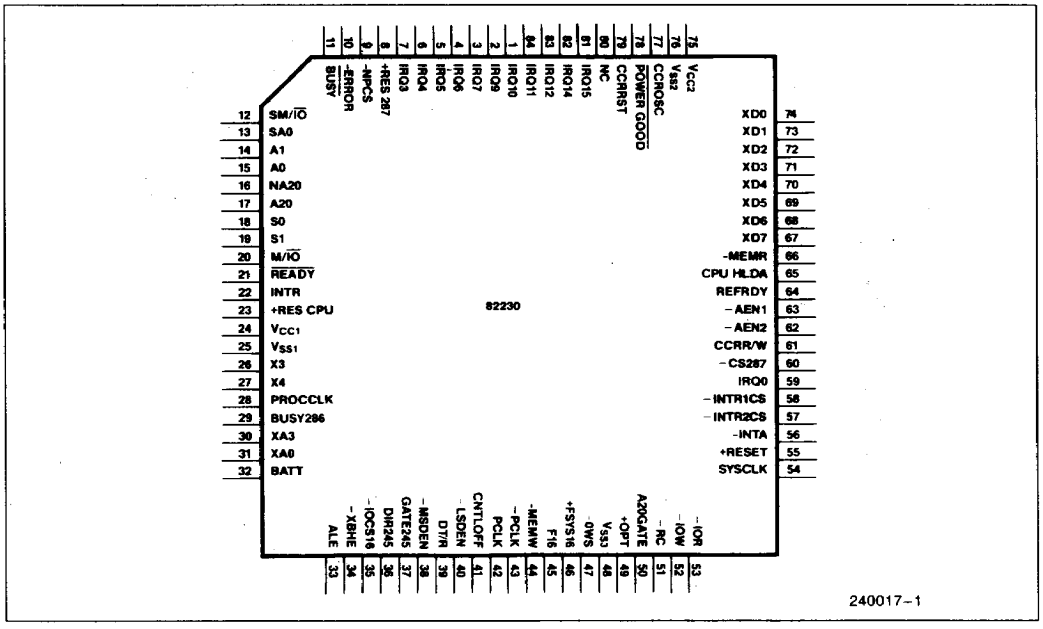


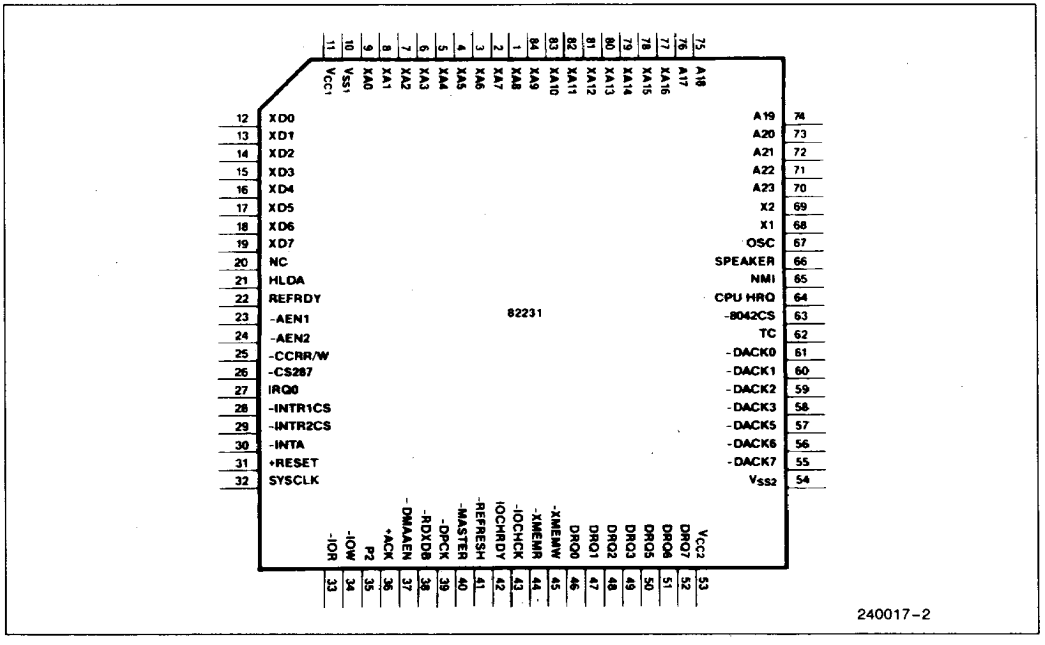
82230—Block Diagram



82231—Block Diagram



Pin Diagram 82230



Pin Diagram 82231

82230 PIN DESCRIPTION

Symbol	Pin No.	Type	Description
A0	15	I	ADDRESS 0 input from the CPU. It is used to generate SA0.
A1	14	I	ADDRESS 1 input from the CPU. It is used in conjunction with M/$\overline{IO}$, S0 and S1 to detect a CPU Shutdown condition.
A20	17	O	ADDRESS 20 is the A20 (NA20) line from the CPU after conditioning by the A20GATE signal. During a CPU Hold A20 goes to a high impedance state.
A20GATE	50	I	A20GATE from the Keyboard Controller is used to force A20 low. When A20GATE is low, A20 on the CPU Address Bus is forced low. When A20GATE is high, A20 follows the CPU Address 20. Tie directly to the P21 Pin of the Keyboard Controller.
−AEN2 −AEN1	62 63	I	ADDRESS ENABLE 1 & 2 from DMA's 1 & 2, respectively. The signal is the result of the DMA's AEN pin NAND'd with −MASTER. Tie directly from the −AEN1 and −AEN2 pins of 82231.
ALE	33	O	ADDRESS LATCH ENABLE is an active high signal that controls the address latches used to hold addresses during bus cycles. ALE is held inactive for Halt bus cycles.
BATT	32	I	BATTERY Power to the Clock Calendar and RAM.
−BUSY286	29	O	−BUSY286 is an active low output indicating the operating condition of the 80287 coprocessor to the processor. It is normally tied to the processor −BUSY pin.
−BUSY	11	I	−BUSY is an active low input from the 80287 to indicate that it is currently executing a command. It is used to generate the −BUSY286 output signal.
CCROSC	77	I	CLOCK CALENDAR OSCILLATOR; 32.768 KHz signal.
CCRRST	79	I	CLOCK CALENDAR RESET signal for the Real Time Clock. This is an active low input.
CCRR/W	61	I	CLOCK CALENDAR READ/WRITE signal for the Real Time Clock. A high enables READ/WRITE operation to the real-time clock. Tie directly from the CCRR/W Pin of 82231.
CNTLOFF	41	O	CONTROL OFF is used to enable the low byte data bus latch during byte accesses. This signal is active high.
CPU HLDA	65	I	CPU HOLD ACKNOWLEDGE is an active high input from the processor. An active condition indicates that the CPU has relinquished the bus to another bus master in the system.
−CS287	60	I	CHIP SELECT 287 is used to derive the −NPCS signal. Tie directly from the −CS287 pin of 82231.
DIR245	36	O	DIRECTION-245 controls the high to low byte and low to high byte conversion during data transfers to and from 8-bit peripherals.

82230 PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Description
DT/$\overline{R}$	39	O	DATA TRANSMIT/RECEIVE establishes the data direction to and from the local data bus. When high, this output signals a CPU write bus cycle. A low indicates a CPU read bus cycle is being performed. This signal is always high when no bus cycle is active.
−ERROR	10	I	ERROR is a negative edge triggered input from the numeric processor indicating that an unmasked error condition exists. Tie directly from the −ERROR Pin of the 80287.
F16	45	I	F16 is an active high input indicating a word memory access. It is used to inhibit command delays for memory accesses.
+FSYS16	46	I	A latched version of F16.
−GATE245	37	O	GATE245 is an active low output. When active it enables the bus transceiver that performs the high to low byte conversion with the DIR245 signal. Conversion does not take place if A0 = 0 which indicates a word transfer.
−INTA	56	O	INTERRUPT ACKNOWLEDGE instructs an interrupting device that its interrupt request is being acknowledged. This signal is active low. −INTA is tri-stated when CPU HLDA is high and CNTLOFF is low. Tie directly to the −INTA pin of 82231.
INTR	22	O	INTERRUPT REQUEST is connected directly to the CPU's interrupt pin. INTR is active high, and is generated when a valid interrupt request has been asserted.
−INTR1CS	58	I	INTERRUPT CONTROLLER 1 (MASTER) CHIP SELECT is an active low input that is used to select the Interrupt Controller as an I/O device. This allows communication between the master interrupt controller and the CPU via the 'X' Data Bus. Tie directly from the −INTR1CS pin of 82231.
−INTR2CS	57	I	INTERRUPT CONTROLLER 2 (SLAVE) CHIP SELECT is an active low input that is used to select the Interrupt Controller as an I/O device. This allows communication between the slave interrupt controller and the CPU via the 'X' data bus. Tie directly from the −INTR2CS Pin of 82231.
−IO CS 16	35	I	I/O 16-BIT CHIP SELECT signals the system that the current data transfer is a 16-bit, one wait-state, I/O cycle. It is derived from an address decode and is an active low signal.
−IOR	53	I/O	I/O READ signal instructs a selected I/O device to drive its data onto the data bus. The −IOR signal is active low. It is tri-stated when CPU HLDA is high and CNTLOFF if low.
−IOW	52	I/O	I/O WRITE signal instructs a selected I/O device to read the data on the data bus. The −IOW signal is active low. It is tri-stated when CPU HLDA is high and CNTLOFF is low.

82230 PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Description
IRQ0	59	I	INTERRUPT REQUEST 0 (system timer) receives interrupt requests from channel 0 of the timer/counter. Tie directly from the IRQ0 pin of 82231.
IRQ7–IRQ3 IRQ10–IRQ9 IRQ12–IRQ11 IRQ15–IRQ14	3-7 1-2 83-84 81-82	I I I I	INTERRUPT REQUESTS 3–7, 9–12, and 14–15 are used to signal the CPU that an I/O device needs attention. The interrupt requests are prioritized with IRQ9–IRQ12 and IRQ14–IRQ15 having the highest priority (IRQ9 highest) and IRQ3–IRQ7 having the lowest priority (IRQ7 lowest). IRQn signals are active high. The requesting signal is held high until the CPU acknowledges the interrupt request.
–LSDEN	40	O	LEAST SIGNIFICANT DATA ENABLE is an active low output. When active, it enables the transceiver/receiver connected to the least significant byte of the local data bus.
–MEMR	66	I/O	MEMORY READ COMMAND instructs a memory device to drive data onto the data bus. This signal is active low. –MEMR is active on all memory read cycles. It is tri-stated when CPU HLDA is high and CNTLOFF Output is low.
–MEMW	44	I/O	MEMORY WRITE COMMAND instructs a memory device to read the data on the data bus. This signal is active low. –MEMW is active on all memory write cycles. It is tri-stated when CPU HLDA is high and CNTLOFF Output is low.
–MSDEN	38	O	MOST SIGNIFICANT DATA ENABLE is an active low output. When active, it enables the transceiver connected to the most significant byte of the local data bus.
M/$\overline{IO}$	20	I	MEMORY-$\overline{INPUT\ OUTPUT}$ is the M/$\overline{IO}$ signal from the CPU. When high, it indicates a memory access. When low, it indicates an I/O access. It is used to generate the memory and I/O signals for the system.
NA20	16	I	NA20 is the CPU address 20. 82230 conditions this signal with A20GATE to produce A20. NA20 is tied directly from the CPU A20 output.
NC	80		Do Not Connect.
–NPCS	9	O	NUMERICAL PROCESSOR CHIP SELECT is an active low output used to select the 80287 Numerical Processor. It is tied directly to the $\overline{NPS1}$ pin of the 80287.
+OPT	49	I	KEYBOARD OUTPUT BUFFER FULL is an active high signal from the Keyboard Controller P24 Pin. The signal is an interrupt request (IRQ1) signaling a full keyboard buffer.
–0WS	47	I	ZERO WAIT STATE option. When pulled active (low), the current processor cycle can be terminated.

82230 PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Description
PCLK	42	O	PERIPHERAL CLOCK is half the frequency of PROCCLK. It is used to clock peripheral controllers, specifically XTAL1 of the Keyboard Controller.
−PCLK	43	O	PERIPHERAL CLOCK INVERTED is the inverse of PCLK. It has been made available specifically for XTAL2 of the Keyboard Controller.
PROCCLK	28	O	PROCESSOR CLOCK provides the clock signal for the CPU and 80287 Numerical Processor. It is equal to the frequency of the crystal across pins X3 and X4. Tie directly to the CLK Pins of the 80286 and 80287.
$\overline{\text{POWER GOOD}}$	78	I	$\overline{\text{POWER GOOD}}$ is an active low input that indicates that system power is sufficient to maintain the integrity of the system. If high, it will force a system reset.
RC	51	I	RESET CPU from the keyboard controller P21 Pin.
$\overline{\text{READY}}$	21	O	$\overline{\text{READY}}$ is an active low output which signals that the current bus cycle is to be completed. S0, S1, $\overline{\text{POWER GOOD}}$, and 0WS control the $\overline{\text{READY}}$.
REFRDY	64	I	REFRESH/IO-CHANNEL-READY is generated by 82231. It is used to preset the READY Interface Asynchronous READY ($\overline{\text{ARDY}}$).
+ RES 287	8	O	RESET 80287 is the reset signal for the 80287 Numerical Processor.
RES CPU	23	O	RESET CPU is the reset signal for the CPU. Active high, RESCPU is generated when either $\overline{\text{POWERGOOD}}$ or RC become active, or when the CPU generates a shut down status by forcing M/$\overline{\text{IO}}$ high. S0, S1 and A1 low. If this signal is initiated by RC, or by M/$\overline{\text{IO}}$, S0, S1 and A1, it will remain active for 16 PROCCLK cycles.
+ RESET	55	O	RESET (SYSTEM) is an active high output derived from the $\overline{\text{POWER GOOD}}$ input. + RESET is used to force the system into an initial state. When + RESET is active, $\overline{\text{READY}}$ will also be active (Low).
S0, S1	18, 19	I	STATUS inputs from the CPU. The status signals are used by the bus controller to determine the state of the CPU.
SA0	13	O	ADDRESS 0 of the CPU bus. SA0 outputs A0 from the CPU during local CPU cycles. During a CPU Hold SA0 goes to a high impedance state so that another master on the expansion bus can take control. During an interrupt acknowledge this signal will be forced low.
SM/$\overline{\text{IO}}$	12	I	SYSTEM MEMORY-INPUT OUTPUT is the M/$\overline{\text{IO}}$ signal from the CPU, conditioned by ALE.
SYSCLK	54	O	SYSTEM CLOCK is the result of PROCCLK divided by two, thus synchronized to the processor's T-states. It may be used to clock peripheral devices that must be synchronized to the CPU.

82230 PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Description
V_{CC1} V_{CC2}	24 75		POWER: +5V supply.
V_{SS1} V_{SS2} V_{SS3}	25 76 48		GROUND.
X3 X4	26 27	I O	CRYSTAL inputs used to generate PROCCLK and SYSCLK. The crystal frequency must be twice the processor clock frequency. Alternatively, an oscillator may be connected to X3.
XA0	31	I	ADDRESS 0 is used by the 8259A to decipher command words the CPU issues. XA0 works in conjunction with the read, write and chip select signals to the interrupt controller in determining whether the CPU wishes to issue a command or read the status of the controller.
XA3	30	I	ADDRESS 3 is used for generating the chip select and reset signals for the 80287.
−XBHE	34	I/O	BUS HIGH ENABLE is an active low signal which is used by 82230 to generate the MSDEN signal.
XD7−XD0	67−74	I/O	Data Bus 0−7 for the peripheral bus. The direction of the bus is determined by the −RDXDB signal from 82231. It is used by the 8259A to decipher command words the CPU issues.

82231 PIN DESCRIPTION

Symbol	Pin No.	Type	Description
−8042CS	63	O	8042 CHIP SELECT is an active low, chip select signal for the Keyboard Controller.
A23−A17	70−76	O	A23−A17 are the Address bits 17−23 of the CPU Address bus. They are outputs directly from the Memory Mapper Pins MO1−MO7 and supply page information during DMA transfers. These outputs are tri-stated unless HLDA and −MASTER are high.
+ACK	36	O	ACKNOWLEDGE is an active low output. When active it enables the bus transceiver between the system and peripheral (XBUS) bus. +ACK is used in conjunction with −RDXDB which controls the direction of the bus transceiver.
−AEN1 −AEN2	23 24	O O	ADDRESS ENABLE FROM DMAs 1 & 2, respectively. The signal is the result of the DMA's AEN signal NAND'd with −MASTER. Tie directly to the −AEN1 and −AEN2 pins of 82230.
CCRR/W	25	O	CLOCK CALENDAR READ/WRITE signal for the real-time clock. A high enables READ/WRITE operations to the real-time clock. Tie directly to the CCRR/W pin of 82230.
CPU HRQ	64	O	CPU HOLD REQUEST is an active high output indicating a DMA request to the CPU. It is also active during refresh cycles. CPU HRQ is normally connected to the 80286 HOLD Pin.

82231 PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Description
−CS287	26	O	CHIP SELECT 287 is used by 82230 to derive the −NPCS signal. Tie directly to the −CS287 pin of 82230.
−DACK0-3 −DACK5-7	61-58 57-55	O O	DMA ACKNOWLEDGE 0-3 and 5-7 are used to acknowledge DMA requests (DRQ0-3 & 5-7). The output signal is an active low.
−DMAAEN	37	O	DMA ADDRESS ENABLE is an active low signal and is active when an I/O device is making a DMA access to system memory or during refresh.
−DPCK	39	I	DATA PARITY CHECK is used to generate NMI. This input is active low.
DRQ0-3 DRQ5-7	46-49 50-52	I I	DMA REQUEST 0-3 & 5-7 are synchronous channel requests used by peripheral devices and I/O processors to gain DMA service. The requests are prioritized with DRQ0 having the highest and DRQ7 having the lowest priorities. A DRQ line must be held active (high) until the corresponding DACK line goes active.
HLDA	21	I	HOLD ACKNOWLEDGE is an active high input that is equivalent to CPU HLDA. An active condition inidicates that the CPU has relinquished the bus to another bus master in the system.
−INTA	30	I	INTERRUPT ACKNOWLEDGE instructs an interrupting device that its interrupt is being acknowledged, and the device may place its interrupt vector onto the data bus. This input signal is active low. −INTA is used by 82231 in the generation of −RDXDB. Tie directly from 82230 Pin 56.
−INTR1CS	28	O	INTERRUPT CONTROLLER 1 (MASTER) CHIP SELECT is an active low output that is used by 82230 to select the Interrupt Controller as an I/O device. This allows communication between the Master Interrupt Controller and the CPU via the 'X' Data Bus. Tie directly to the −INTR1CS pin of 82230.
−INTR2CS	29	O	INTERRUPT CONTROLLER 2 (SLAVE) CHIP SELECT is an active low output that is used by 82230 to select the Interrupt Controller as an I/O device. This allows communication between the Slave Interrupt Controller and the CPU via the 'X' Data Bus. Tie directly to the −INTR2CS Pin of 82230.
−IOCHCK	43	I	I/O CHANNEL CHECK is an active low input. It is used to indicate an uncorrectable system error. It provides the system with parity error information about memory or devices on the I/O channel.
IOCHRDY	42	I	I/O CHANNEL READY is generated by an I/O device. When low it indicates a 'not ready' condition and forces the insertion of wait states in I/O or Memory accesses by the I/O device. When active (high), it will allow the completion of a memory or an I/O access by the I/O device.

82231 PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Description
−IOR	33	I/O	I/O READ signal instructs a selected I/O device to drive its data onto the data bus. The −IOR signal is active low. It is used for data transfers between the CPU and I/O devices and by DMA transfers.
−IOW	34	I/O	I/O WRITE signal instructs a selected I/O device to read the data on the data bus. The −IOW signal is active low. It is used for data transfers between the CPU and I/O devices and by DMA transfers.
IRQ0	27	O	INTERRUPT REQUEST 0 (System Timer) from Channel 0 of the Timer/Counter. Tie directly to the IRQ0 Pin of 82230.
−MASTER	40	I	−MASTER is an active low input used in conjunction with a DRQ line to gain control of the system. A DMA controller or processor on the I/O channel may issue a DRQ to a DMA channel and receive a −DACK. The I/O processor may then activate −MASTER which will allow it to control the system address, data, and control lines.
NC	20		Do Not Connect.
NMI	65	O	NON-MASKABLE INTERRUPT is an active high output that is connected to the CPU NMI pin.
OSC	67	O	OSCILLATOR output is the clock frequency of the crystal connected across X1−X2. It is the OSC output from the Clock Generator.
P2	35	O	P2 is an active high output indicating that a valid refresh address is available on the XA bus.
−RDXDB	38	O	READ X-DATA BUS controls the direction of the bidirectional buffer between the least significant byte of the 'S' Data Bus and the 'X' Data Bus. −RDXDB is used in conjunction with +ACK to control XBUS activity. When +ACK is active (low) and −RDXDB is low, data is to be read from the peripheral bus. When +ACK is active (low) and −RDXDB is high, data is to be written to the peripheral bus.
REFRDY	22	O	REFRESH/IO-CHANNEL-READY is generated by +REFRESH OR'd with IOCHRDY. It is used by 82230 to preset the Clock Generator & Ready Interface Asynchronous Ready ($\overline{ARDY}$).
−REFRESH	41	I/O	REFRESH is an active low output used to initiate a refresh cycle for the dynamic RAMs.
+RESET	31	I	RESET (SYSTEM) is an active high input from 82230. +RESET is used to force 82231, as well as the system, into an initial state. Tie directly from 82230 Pin 55.
SPEAKER	66	O	SPEAKER DATA is an output of the Programmable interval timer tone signal used to drive the speaker.
SYSCLK	32	I	SYSTEM CLOCK input from 82230. It is used to synchronize 82231 to the system. Tie directly from 82230 SYSCLK Pin.
TC	62	O	TERMINAL COUNT provides a pulse when the terminal count for any DMA channel is reached.

82231 PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Description
V_{CC1} V_{CC2}	11 53		POWER: +5V supply.
V_{SS1} V_{SS2}	10 54		GROUND.
X1 X2	68 69	I O	CRYSTAL inputs for the internal oscillator used to generate clocking for I/O devices. A parallel resonant fundamental frequency mode crystal is required. An alternative oscillator may be connected to X1.
XA8–XA0 XA9 XA16–XA10	1–9 84 77–83	I/O I/O O	XBUS ADDRESSES 0–16 are the peripheral addresses for the local I/O bus.
XD0–XD7	12–19	I/O	Data Bus 0–7 for the peripheral bus. The direction of the bus is determined by the −RDXDB signal from 82231.
−XMEMR	44	I/O	MEMORY READ signal indicating a DMA read operation from peripheral devices or memory.
−XMEMW	45	O	MEMORY WRITE signal indicating a DMA write operation to peripheral devices or memory. It is tri-stated except during DMA transfers.

FUNCTIONAL DESCRIPTION

Introduction

The 82230 and 82231 are a two-chip implementation of LSI/MSI/SSI logic controlling the IBM Personal Computer AT. The devices provide a low power, highly integrated PC-AT design solution that may also be applied to any 80286-based system. With the 82230 and 82231, a PC-AT system can be designed to operate at 12 MHz with zero wait state RAM accesses.

These standard cell products contain most of the logic peripheral to the microprocessors and memory on the "standard" AT motherboard. The LSI peripherals which support the AT design reside as supercells on the 82230/82231 chips. These peripherals are compatible with the products they replace and the user should refer to the standard product data sheets for additional information on the operation of these devices.

The PC-AT schematics in the IBM PC-AT Technical Reference Manual are also a good source of information about the 82230/82231's internal logic.

The 82230 performs the functions of the 82284 Clock Generator & Ready Interface, 82288 Bus Controller, 6818 Real Time Clock/RAM, and the Master-Slave implementation of the dual 8259A Programmable Interrupt Controllers as well as Command Delay, Shut Down, Address/Data Bus Control and Ready Generation logic.

The 82231 includes the 8254 Programmable Interrupt Timer, 8284A Clock Generator, LS612 Memory Mapper and the dual 8237 DMA Controller functions as well as Refresh Generation and Refresh/DMA Arbitration Logic.

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PC-AT BLOCK DIAGRAM

The block diagram is shown below in Figure 1 which shows the 82230 and 82231 being used in a PC-AT compatible design. Note how the basic structure of the PC-AT is retained in the design. The five address busses and four data busses are present. The 82230 and 82231 'sit' on the X Address and Data Busses and monitor the status and control line outputs from the 80286 in order to operate the peripheral supercells.

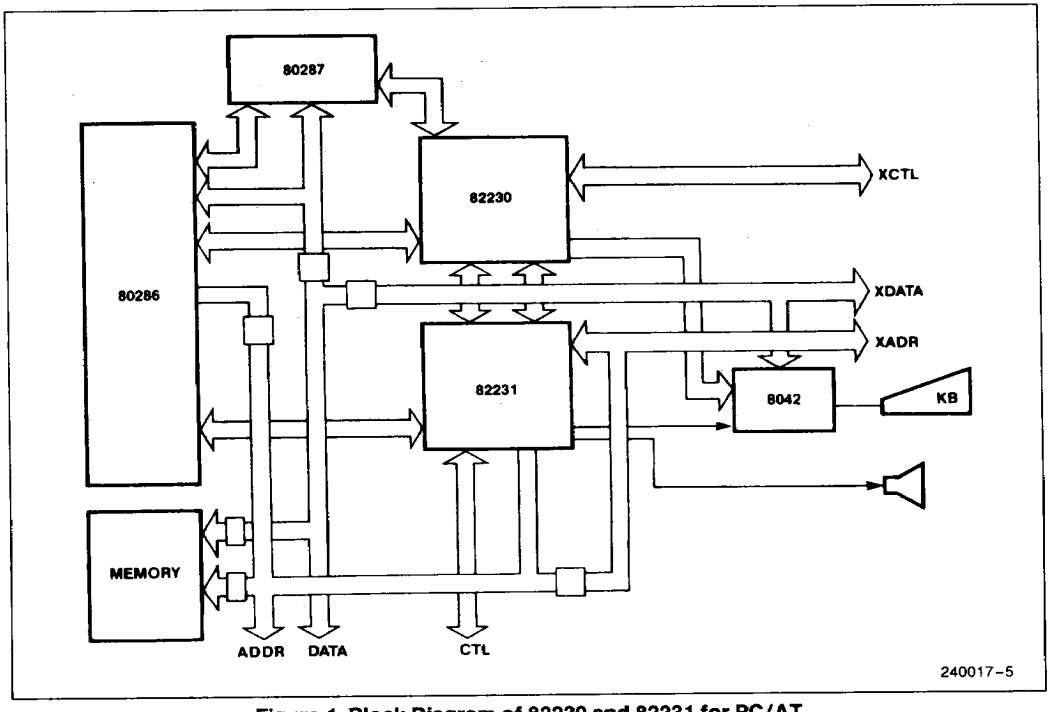


Figure 1. Block Diagram of 82230 and 82231 for PC/AT

A brief description of each of the basic PC-AT busses is included in order to show how a system design using the 82230/82231 allows for the retention of the PC-AT bus structure.

ADDRESS BUSSES

The 82230/82231 allows a straightforward PC-AT design which preserves the five basic address busses. System designers can interact with these busses, create new busses, or eliminate busses, depending upon design objectives. Each bus must be independently buffered and separated by buffers/latches. Most handshake signals are generated by the 82230/82231.

The Local Address Bus is comprised of the 24 address pins emanating from the 80286. External buffers are required in order to separate the local address bus from the system address bus. A0, however, is input directly into the 82230 and is used in conjunction with XBHE in order to enable the appropriate memory bank. The 82230 inputs CPU address bit NA20 and outputs A20.

The System Address Bus is the main AT address bus. This is a latched version of the local address bus, and is a 20-bit bus. SA0 is an output of the 82230 and SA1–SA19 are latched from the local address bus. The latch signal is ALE, which is generated by the 82288 supercell in the 82230. CPU HLDA, generated by the 80286 and active high, should be used as the output enable signal.

The Memory Address Bus applies to the RAM on the PC-AT system board only. It is a multiplexed version of the System Address Bus with nine address lines, MA0–MA8. External multiplexers are used to generate the row and column addresses.

The X Address Bus is separated from the System Address Bus. The X address lines are input/outputs into the 82230/82231. The X Address Bus is a motherboard address bus which is used to address ROM (BIOS) and motherboard I/O. In addition, the X Address Bus generates addresses for DMA and memory refresh.

The L Address Bus is an unlatched 7-bit address bus. LA17–LA23 can allow a PC-AT design up to 16 MBytes of address space. The L Address Bus should be made available at the expansion bus connector.

DATA BUSSES

The Local Data Bus is the name for the data bus lines emanating directly from the 80286. The local data bus has 16 lines, D0–D15. Because the 80286 can do word and byte transfers and because word transfers need not be aligned, it is necessary to design a bus interface which differentiates between the high bus byte and the low bus byte.

The System Data Bus is the main data bus of a PC-AT system and interfaces with all other data busses. The 82230 and 82231 are designed to control these interfaces in order to simplify system design and maximize bus flexibility.

The Memory Data Bus interfaces both DRAM and ROM. It is a 16-bit bus and connects with the System Data Bus through buffers.

The X Data Bus is the bus intended primarily for system board I/O functions. It interfaces to functions such as the DMA controllers, Interrupt controllers, Keyboard controller, and Real Time Clock.

82230/82231 Interface

The 82230 and 82231 are relatively independent of each other; the 82230 generates most of the timing and control signals and the 82231 controls the X Address Bus for DMA and refresh. Both chips have additional functions but because of the desire to partition the system design such that the 82230 and the 82231 could be assembled in low cost 84-pin PLCC packages, each chip relies on the other for certain functions. This entails introducing dedicated interface signals between the 82230 and 82231 into a system design. The 82230/82231 interface requires 14 pins on each device and these pins are described below.

- REFRDY is generated by the 82231 and used to tell the 82230 to insert wait-states in response to the 82231 input IOCHRDY. IOCHRDY is active high.
- −AEN1 and −AEN2 are signals generated by the 82231 which indicate DMA byte (−AEN1) or word (−AEN2) transfers, and are used by the 82230 to generate bus buffer control signals.
- CCRR/W is generated by the 82231 and used by the 82230 as part of the 6818 chip select.
- −INTR1CS and −INTR2CS are generated by the 82231 and used by the 82230 as the interrupt controller chip selects.
- −CS287 is generated by the 82231 and is used by the 82230 to generate 80287 control signals.
- IRQ0 is the output of the 8254 timer 0 on the 82231 and is connected to interrupt request 0 on the master interrupt controller in the 82230.

- +RESET is generated by the 82230 in response to POWERGOOD and is used by the 82231 for initialization.
- SYSCLK is PROCCLK divided by two.
- −INTA, −MEMR, −IOR, and −IOW are commands generated by the 82230 in response to the 80286 status inputs S0 and S1, and are used by the 82231 as basic system commands.

Coprocessor Interface

The 82230 contains a coprocessor interface logic block to allow interfacing with an 80287 math coprocessor. The coprocessor interface includes the IBM PC-AT compatible error handling hardware.

Memory Operations

When the 82230 and 82231 are used in a PC-AT system design, the system can be designed to operate with the full 16 MBytes of memory that the 24 address lines of the 80286 allow.

The 82230/82231 chipset normally operates with one wait state inserted for memory operations and four wait-states inserted for I/O operations. The number of wait states may be increased for slow memory or I/O devices, or decreased if use of high-speed memory or I/O devices is desired in order to provide higher system performance.

During normal operation, the number of ROM accesses are relatively few compared to RAM accesses, so ROM subsystem speed does not significantly affect system performance. When designing high performance PC-AT systems, it should be verified that the ROM subsystem is fast enough for operation. Note also that older versions of the IBM BIOS may not operate in systems faster than 8 MHz. Modifications of both RAM and ROM subsystem performance are covered in detail in the Intel 286EX Application Note.

System Clocks and Oscillators

Because of the high level of integration of the 82230/82231, several different clock frequencies are present on the chips. Figure 2 shows the relationships between the various clock signals.

PROCCLK is the main system clock which is used in a PC-AT system to generate all the basic system and bus timings. The clock is generated by the 82230 and operates at twice the system clock frequency. See Table 1 for processor clock capacitance. The tolerance of the PROCCLK oscillator is independent of the 82230/82231 and is primarily determined by the requirements of the 80286 and 80287 processors. For reliable operation at the specified V_{DD} and temperature condition, the processor timing specifications must not be exceeded.

Table 1. Recommended Fundamental Mode Crystal Characteristics and Recommended Load Capacitance for PROCCLK

Oscillator	Crystal Freq.	C_{LOAD} (pF)	C_{IN} (pF) X3	C_{OUT} (pF) X4
PROCCLK	12 MHz	20	30	10
PROCCLK	16 MHz	20	30	10
PROCCLK	20 MHz	20	27	8
PROCCLK	24 MHz	20	22	8

SYSCLK is PROCCLK divided by two, and should be used as the expansion bus clock. SYSCLK is an output of the 82230. To ensure compatibility with expansion cards, SYSCLK should not be above 8 MHz.

X1 is an input to the 82231 which is 12 times the frequency used to clock the three counters in the 8254 timer on the 82231. In order to be compatible with AT hardware and software, it should be a 14.318 MHz fundamental mode crystal with C_{LOAD} = 32 pF, and a 27 pF capacitor should be placed in series with the crystal. Alternately, a 14 MHz funda-

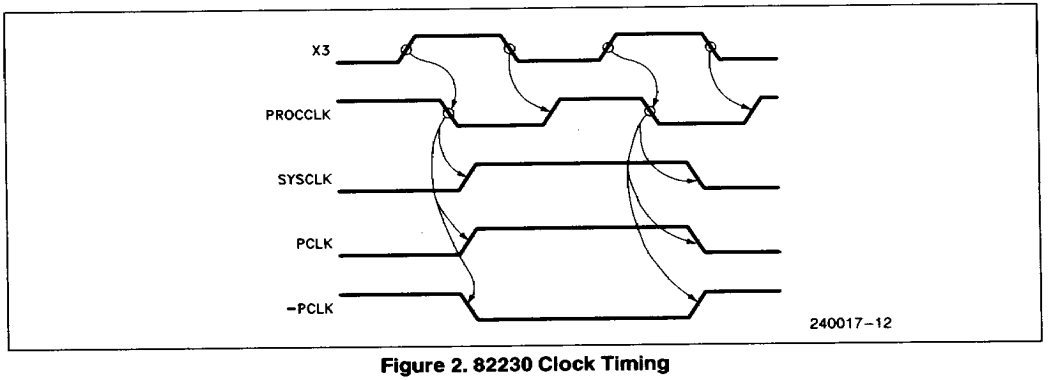


Figure 2. 82230 Clock Timing

mental mode crystal (C_{LOAD} = 32 pF) may be trimmed with a 5–50 pF trimmer capacitor in series for high accuracy applications such as NTSC or RS170 video-compatibility with chroma colorburst.

Note that the trim cap must be adjusted with a low-capacitance nylon or teflon tuning wand for accurate trimming. Tolerance for this clock is 0.1% or less for non-video or non time-critical use, 0.01% or greater if used for video color-burst or time-critical applications.

The CCR clock is the low-frequency oscillator used to clock the 6818 Clock/Calendar/RAM on the 82230. CCROSC tolerance is variable and dependent upon real-time clock accuracy requirements. See Table 2 for CCROSC clock tolerance and accuracy.

Table 2. CCROSC Tolerance/Accuracy

Tolerance	Accuracy
0.001% or 10 ppm	5 minutes/year trimming required
0.01% or 100 ppm	1 minute/week no trimming required
0.02% or 200 ppm	2 minutes/week no trimming required
0.05% or 500 ppm	5 minutes/week no trimming required

EXTERNAL OSCILLATORS

External CMOS output drive oscillators may be used for either PROCCLK or OSC. Simply connect the external oscillator outputs to PROCCLK inputs X1 or X3. TTL output oscillators may be used if the output drive V_{OH} is greater than 4.1V; pull-up resistors will generally suffice. The oscillator invertor outputs X2 and X4 may be left open, or may be used to drive one moderate rise-time CMOS load if needed.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with Respect to Ground .... −0.5V to V_{CC} +0.5V
Power Dissipation 1W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

82230/82231 DC CHARACTERISTICS

V_{CC} = 5V ±5%, V_{BAT} = 2.8V to V_{CC}, T_A = 0°C to +70°C

Parameter	Conditions	Min	Max	Units
V_{IL}			0.5	V
V_{IH}		2.0		V
V_{IL} 82230 Pins 26, 77, 78, 79 82231 Pins 41, 42, 68			0.5	V
V_{IH} 82230 Pins 26, 77, 78, 79 82231 Pins 41, 42, 68		V_{CC} − 0.5		V
V_{IH} 82230 Pin 47		V_{CC} − 0.5(1)		V
I_{I0}	V_{IN} = 0	−100		µA
I_{I0} 82230 Pins 26, 77, 78, 79	V_{IN} = 0	−10		µA
I_{I1}	V_{IN} = V_{CC}		10	µA
I_{OH} Except for 82231 Pin 41(2)	V_{OH} = 2.4		−4	mA
I_{OL}	V_{OL} = 0.45V	4		mA
I_{OL} 82230 Pins 13, 28, 44, 52, 53 54, 56, 66 82231 Pins 33 34, 67	V_{OL} = 0.45V	16		mA
I_{OL} 82231 Pin 41	V_{OL} = 0.45V	18		mA
I_{OZ}	V_O = 0 to V_{CC}	−10	+10	µA
I_{CC} 82230	F = 10 MHz F = 12 MHz		55 60	mA mA
I_{CC} 82231	F = 10 MHz F = 12 MHz		45 50	mA mA
I_{CC} 82230 from Battery	F = 32.768 KHz V_{BAT} = 5V V_{CC} = 0V		25	µA
I_{CC} 82230 from Battery	F = 32.768 KHz V_{BAT} = 2.8V V_{CC} = 0V		20	µA

NOTES:
1. −0WS (82230 Pin 47) is driven by an open collector output. It is pulled up to CMOS voltage levels of V_{CC} − 0.5V by a pullup resistor.
2. −REFRESH (82231 Pin 41) is an open collector output.
3. CCROSC is the only signal that should switch in the battery back up mode. For back up operation with V_{BATT} < 4.75V, CCROSC, $\overline{\text{POWERGOOD}}$ and CCRRST input levels V_{IL}/V_{IH} should be 10% and 90% of V_{BATT}, respectively.

82230 AC CHARACTERISTICS (V_{DD} = 5V ±5%, T_A = 0°C to 70°C)

Symbol — Figure	Parameter	10 MHz		12 MHz		Units	Notes
		Min	Max	Min	Max		
53–15 54–15	−0WS Setup Time to PROCCLK ↓ −0WS Hold Time from PROCCLK ↓	25 0		25 0		ns ns	13 13
	−0WS Setup Time to PROCCLK ↓ −0WS Hold Time from PROCCLK ↓	36 0		36 0		ns ns	11 11
69–22	A0 Setup Time to ALE A0 Hold Time from ALE	30 0		25 0		ns ns	
26–6 27–6	A1 Setup Time to S1, S0 A1 Hold Time from S1, S0	27 0		22 0		ns ns	
43–13 44–13 45–13 46–13	A20 Delay from NA20 A20 Delay from A20GATE A20 Disable Delay from CPUHLDA ↑ A20 Enable Delay from CPUHLDA ↓		27 37 35 35		22 32 30 30	ns ns ns ns	 4
17–3 18–3	ALE Active Delay from PROCCLK ↓ ALE Inactive Delay from PROCCLK ↓		25 30		23 25	ns ns	
68–21	$\overline{\text{BUSY286}}$ Delay from $\overline{\text{BUSY}}$, −IOW		35		35	ns	
	CCROSC High Time CCROSC Low Time CCROSC Input Rise/Fall Time	25 25	 20	25 25	 20	µs µs ns	5 5 12
39–10, 11 40–10, 11	CCRR/W Setup Time to IOR/IOW ↓ CCRR/W Hold Time from IOR/IOW ↑	0 17		0 15		ns ns	
	CCRRST Pulse Width	100		83		ns	
67–20	CNTLOFF Delay from PROCCLK ↓		30		25	ns	
70–23 71–23	CPUHLDA Setup Time to PROCCLK ↓ CPUHLDA Hold Time from PROCCLK ↓	20 0		15 0		ns ns	
49–14 49–14	DIR245 Delay from −IOR ↓, −IOW ↓ DIR245 Delay from −MEMR, −MEMW DIR245 Delay from −AEN1, −AEN2		17 17 40		15 15 35	ns ns ns	
55–16 56–16	DT/R Delay High from PROCCLK ↓ DT/R Delay Low from PROCCLK ↓		45 45		40 40	ns ns	
60–16 61–16	F16 Setup Time to PROCCLK ↓ F16 Hold Time from PROCCLK ↓	30 0		30 0		ns ns	
	+FSYS16 Setup Time to PROCCLK ↓ +FSYS16 Hold Time from PROCCLK ↓	100 50		83 40		ns ns	
50–14 50–14	−GATE245 Delay from −IOR ↓, −IOW ↓ −GATE245 Delay from −MEMR, −MEMW −GATE245 Delay from −AEN1, −AEN2		22 22 45		20 20 40	ns ns ns	

82230 AC CHARACTERISTICS (V_{DD} = 5V ±5%, T_A = 0°C to 70°C) (Continued)

Symbol – Figure	Parameter	10 MHz		12 MHz		Units	Notes
		Min	Max	Min	Max		
37–9	Interrupt Request Pulse Width	100		100		ns	8
29–7, 8	–IOR, –IOW Active Delay from PROCCLK ↓	3	15	3	15	ns	
30–7, 8	–IOR, –IOW Inactive Delay from PROCCLK ↓	3	15	3	15	ns	
	–IOR, –IOW Enable/Disable Delay from CPUHLDA		40		40	ns	
	–INTA Active Delay from PROCCLK ↓	3	45	3	35	ns	
	–INTA Inactive Delay from PROCCLK ↓	3	45	3	35	ns	
	–INTA Enable/Disable Delay from CPUHLDA		40		40	ns	
38–9	INTR Delay from Interrupt		175		150	ns	
33–7, 8	–INTR1CS, – INTR2CS Setup Time to –IOR, –IOW ↓	0		0		ns	
34–7, 8	–INTR1CS, – INTR2CS Hold Time from –IOR, –IOW ↑	0		0		ns	
72–24	–IO CS 16 Setup Time to SYSCLK ↓	85		75		ns	
73–24	–IO CS 16 Hold Time from SYSCLK ↓	0		0		ns	
57–16	–LSDEN, –MSDEN Active Delay from PROCCLK ↓		45		40	ns	
58–16	–LSDEN, –MSDEN Inactive Delay from PROCCLK ↓		35		30	ns	
66–19	–LSDEN, –MSDEN Delay from –NPCS		15		15	ns	
	–LSDEN, –MSDEN Active Delay from SM/$\overline{IO}$ after –CS287 Inactive		30		30	ns	
79–16	–MEMR, –MEMW Active Delay from PROCCLK ↓	3	15	3	15	ns	
80–16	–MEMR, –MEMW Inactive Delay from PROCCLK ↓	3	15	3	15	ns	
	–MEMR, –MEMW Enable/Disable Delay from CPUHLDA		40		40	ns	
64–17	–MSDEN Delay from –XHBE		27		25	ns	
62–16	M/$\overline{IO}$ Setup Time to PROCCLK ↓	28		25		ns	
63–16	M/$\overline{IO}$ Hold Time from PROCCLK ↓	0		0		ns	
65–18	–NPCS Delay from SM/$\overline{IO}$ –CS287, XA3, –INTA		40		35	ns	
11–2	PCLK, –PCLK High Time	45		35		ns	
12–2	PCLK, –PCLK Low Time	45		35		ns	
13–2	PCLK, –PCLK Delay from PROCCLK		45		40	ns	
14–2	PCLK, –PCLK Rise/Fall Times		7.5		5	ns	12
19–4	$\overline{POWER\ GOOD}$ Setup Time to PROCCLK ↓	26		26		ns	3
	$\overline{POWER\ GOOD}$ Hold Time from PROCCLK ↓	50		41		ns	3
8–4	$\overline{POWER\ GOOD}$ Rise/Fall Times		20		20	ns	12
	$\overline{POWER\ GOOD}$ Inactive Pulse Width	1		1		μs	
5–2	PROCCLK Delay from X3	5	25	5	20	ns	
6–2	PROCCLK High Time	16		13		ns	
7–2	PROCCLK Low Time	12		11		ns	
9–2	PROCCLK Rise/Fall Time		8		8	ns	12
22-5	–RC Setup Time to SYSCLK ↑	30		30		ns	3
23-5	–RC Pulse Width	100		83		ns	
51–15	$\overline{READY}$ Active Delay from PROCCLK ↓		22		18	ns	
52–15	$\overline{READY}$ Inactive Delay from PROCCLK ↓		70		60	ns	

82230 AC CHARACTERISTICS (V_{DD} = 5V ±5%, T_A = 0°C to 70°C) (Continued)

Symbol – Figure	Parameter	10 MHz		12 MHz		Units	Notes
		Min	Max	Min	Max		
	REFRDY Pulse Width	50		40		ns	
	REFRDY Hold Time from PROCCLK ↓	34		34		ns	
	REFRDY Setup Time to PROCCLK ↓	−14		−14		ns	
74–25	RES 287 Delay from −IOW		60		50	ns	
21–4	RES CPU Delay from PROCCLK ↓		27		22	ns	
20–4	+RESET Delay from PROCCLK ↓		50		50	ns	
41–12	SA0 Enable Time from CPU HLDA		60		50	ns	
42–12	SA0 Disable Time from CPU HLDA		60		50	ns	4
15–3	S1, S0 Setup Time to PROCCLK ↓	28		15		ns	
16–3	S1, S0 Hold Time from PROCCLK ↓	0		0		ns	
10–2	SYSCLK Delay from PROCCLK ↓	5	20	5	20	ns	
1–2	X3 Period	50		41.7		ns	
2–2	X3 Low Time	17		15		ns	
3–2	X3 High Time	23		20		ns	
4–2	X3 Rise/Fall Times		5		3	ns	12
35–8, 11	XD0–XD7 Delay Time from −IOR ↓		45		40	ns	
36–8, 11	XD0–XD7 Hold Time from −IOR ↑		17		15	ns	
31–7	XD0–XD7 Setup Time to −IOW ↑	100		83		ns	
32–7	XD0–XD7 Hold Time from −IOW ↑	0		0		ns	

82231 AC CHARACTERISTICS (V_{DD} = 5V ±5%, T_A = 0°C to 70°C)

Symbol – Figure	Parameter	10 MHz		12 MHz		Units	Notes
		Min	Max	Min	Max		
96–27	−8042CS Delay from XA_X		60		48	ns	
98–28	A17–A23 Delay from SYSCLK ↑		150		125	ns	
99–28	A17–A23 Enable Delay from HLDA or −MASTER		100		83	ns	
97–28	A17–A23 Disable Delay from HLDA or −MASTER		100		83	ns	4
100–29	+ACK Delay from HLDA		45		40	ns	
101–29	+ACK Delay from −MASTER		45		40	ns	
109–30	−AEN1, −AEN2 Delay from SYSCLK ↑		130		115	ns	
94–27	CCRR/W Delay from XA_X		60		48	ns	
102–29	CCRR/W Delay from HLDA or −MASTER		50		41	ns	
108–30, 39	CPU HRQ Delay from SYSCLK ↑		80		70	ns	
95–26	−CS287 Delay from XA_X		60		48	ns	
103–29	−CS287 Delay from HLDA or −MASTER		50		41	ns	
113–30	−DACK0–3, −DACK5–7 Delay from SYSCLK ↑		110		100	ns	
110–30	−DMAAEN Delay from SYSCLK ↑		140		120	ns	

82231 AC CHARACTERISTICS (V_{DD} = 5V ±5%, T_A = 0°C to 70°C) (Continued)

Symbol – Figure	Parameter	10 MHz		12 MHz		Units	Notes
		Min	Max	Min	Max		
132–32	–DPCK Setup Time to –XMEMR ↑	8		6		ns	
133–32	–DPCK Hold Time from –XMEMR ↑	5		5		ns	
107–30	–DRQ0–3, –DRQ5–7 Setup Time to SYSCLK ↑	0			0	ns	3, 7
	HLDA Setup Time to SYSCLK ↑	70		65		ns	
	HLDA Hold Time from SYSCLK ↑	0		0		ns	
28–7	–INTR1CS, –INTR2CS Delay from XA_X		60		41	ns	
104–29	–INTR1CS, –INTR2CS Delay from HLDA or –MASTER		60		41	ns	
134–33	–IOCHCK Pulse Width		25		20	ns	
	IOCHRDY Setup Time to SYSCLK ↑ (During Refresh)	25		25		ns	
	IOCHRDY Hold Time from SYSCLK ↑ (During Refresh)	25		25		ns	
114–30	–IOR, –IOW Active Delay from SYSCLK ↑ (During DMA Transfers)		125		100	ns	
115–30	–IOR, –IOW Inactive Delay from SYSCLK ↑ (During DMA Transfers)		115		100	ns	
116–30	–IOR, –IOW Float to Inactive Delay from SYSCLK ↑ (During DMA Transfers)		120		100	ns	
117–30	–IOR, –IOW Inactive to Float Delay from SYSCLK ↑ (During DMA Transfers)		170		156	ns	4
152–37	–IOW Active Pulse Width (During CPU Transfers)	90		75		ns	
137–34	IRQ0 Delay from X1		100		100	ns	
	NMI Delay from –XMEMR ↑		100		83	ns	
135–33	NMI Delay from –IOCHCK ↓		100		83	ns	
143-35	OSC Low Time	20		20		ns	
144-35	OSC High Time	20		20		ns	
145-35	OSC Rise/Fall Times		15		15	ns	12
146-35	OSC Delay from X1		30		24	ns	
	P2 Delay from SYSCLK ↑		100		83	ns	
148–36	–RDXDB Delay from –IOR		100		83	ns	
149–36	–RDXDB Delay from –INTA		100		83	ns	
	REFRDY Delay from IOCHRDY	10	35	10	35	ns	
157–39	–REFRESH Delay from HLDA		28		24	ns	
158–39	–REFRESH Delay from SYSCLK ↑		100		83	ns	
	+RESET Active Pulse Width	200		160		ns	
138–34	SPEAKER Delay from X1		100		100	ns	
91–26	SYSCLK Period	100		83		ns	
92–26	SYSCLK Low Time	40		30		ns	
93–26	SYSCLK High Time	40		30		ns	

82231 AC CHARACTERISTICS (V_{DD} = 5V ±5%, T_A = 0°C to 70°C) (Continued)

Symbol – Figure	Parameter	10 MHz		12 MHz		Units	Notes
		Min	Max	Min	Max		
124–30	TC Delay from SYSCLK ↑		110		100	ns	
140–35	X1 Low Time	30		30		ns	
141–35	X1 High Time	30		30		ns	
142–35	X1 Rise/Fall Times		5		5	ns	12
150–37	XA_X Input Setup Time to –IOW ↓ (During CPU Transfers to 82231)	100		83		ns	
151–37	XA_X Input Hold Time from –IOW ↑ (During CPU Transfers to 82231)	45		40		ns	
	XA_X Input Hold Time from –IOR ↑ (During CPU Transfers to 82231)	100		67		ns	
111–30	XA_X Valid Delay from SYSCLK ↑ (During DMA Transfers)		160		150	ns	
159–39	XA_X Valid Delay from SYSCLK ↑ (During Refresh)		90		75	ns	
112–30	XA_X Disable Delay from SYSCLK ↑ (During DMA Transfers)		150		130	ns	4
153-37	XD_X Input Setup Time to –IOW ↑	100		83		ns	
154-37	XD_X Input Hold Time from –IOW ↑	17		15		ns	
155-38	XD_X Output Delay from –IOR ↓		125		100	ns	
156-38	XD_X Output Hold Time from –IOR ↑	17	70	15	60	ns	
125–31	–XMEMR Active Delay from SYSCLK ↑		110		100	ns	
126–31	–XMEMR Inactive Delay from SYSCLK ↑		110		100	ns	
127–31	–XMEMR Enable/Disable Delay from SYSCLK ↑		120		120	ns	4, 12
121–30	–XMEMW Active Delay from SYSCLK ↑		110		100	ns	
122–30	–XMEMW Inactive Delay from SYSCLK ↑		110		100	ns	
123–30	–XMEMW Enable/Disable Delay from SYSCLK ↑		120		120	ns	4, 12

NOTES:
1. To provide clearly understood information, the complex timing diagrams depict operation in a standard IBM PC AT system design. Combinational logic data paths are shown with less complex timing diagrams. The signal source (82230, 82231, PROCESSOR, LOGIC, etc.) follows the signal name.
2. The direction control signals are delayed to PROCCLK ↓ on an –IOW cycle. This is done to avoid changing the direction of the byte-swapping bus transceivers while data is still on the bus.
3. This signal is an asynchronous input. The timing specification is provided for testing purposes only to assure recognition at a specific clock edge.
4. The output float or high impedance condition occurs when output current is less than I_{OZ} in magnitude.
5. The frequency of CCROSC sets the count rate for the real time clock. CCROSC frequency, accuracy and stability, should be maintained as close as possible to 32.768 KHz to insure the validity of time and data information.
6. Input rise and fall times are assumed to be less than 20 ns unless otherwise specified.
7. DRQ_X must be held active with $DACK_X$ is returned.
8. The interrupt request inputs include IRQ0, IRQ3–7, IRQ9–12, IRQ14–15 and +OPT.
9. Address XA_{0-15} are output for byte DMA operations. XA_{0-16} are output for word DMA operations, with XA0 low.
10. A minimum of 16 PROCCLK cycles must occur before $\overline{\text{POWERGOOD}}$ becomes valid.
11. At the end of TC phase 1 after TCW2 or TCW3 for 16-bit transfer to 8-bit source/destination, for the first 8 bits of transfer.
12. These are not tested. They are guaranteed by design characterization.
13. At the end of TC phase 1 for 16 bit back plane memory transfers and 8-bit transfers after TCW2 or TCW3.

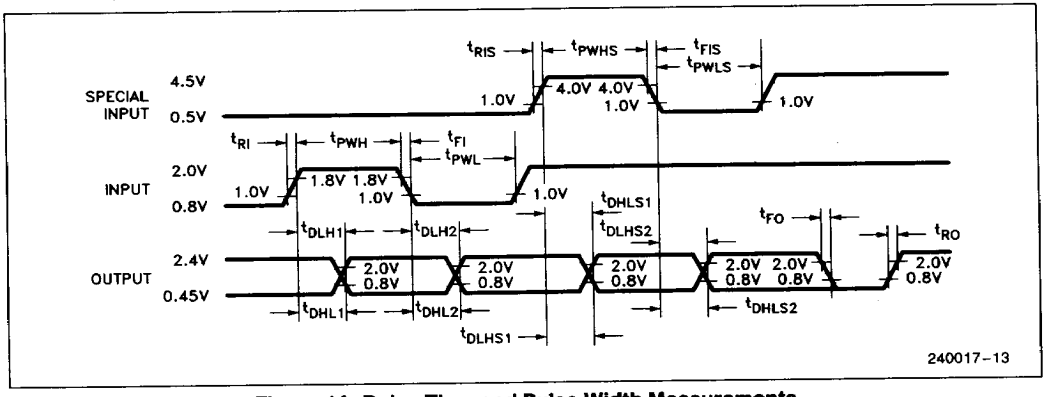


Figure 1A. Delay Time and Pulse Width Measurements

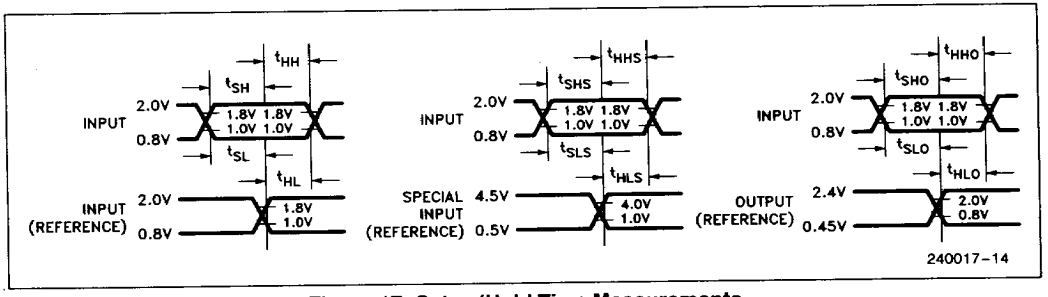


Figure 1B. Setup/Hold Time Measurements

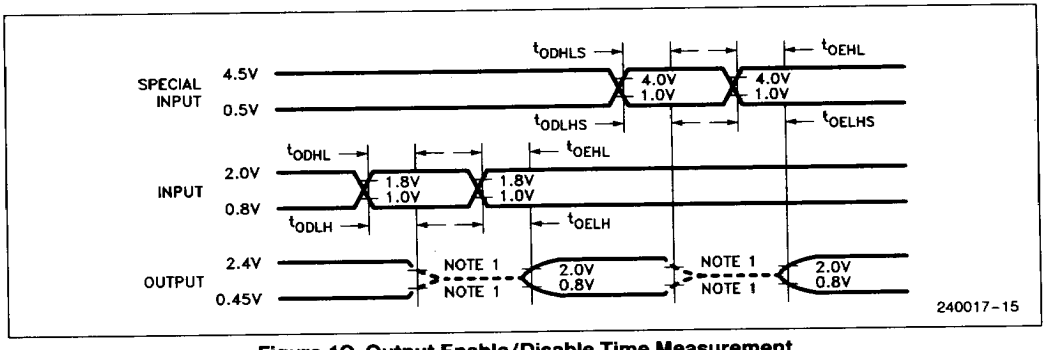


Figure 1C. Output Enable/Disable Time Measurement

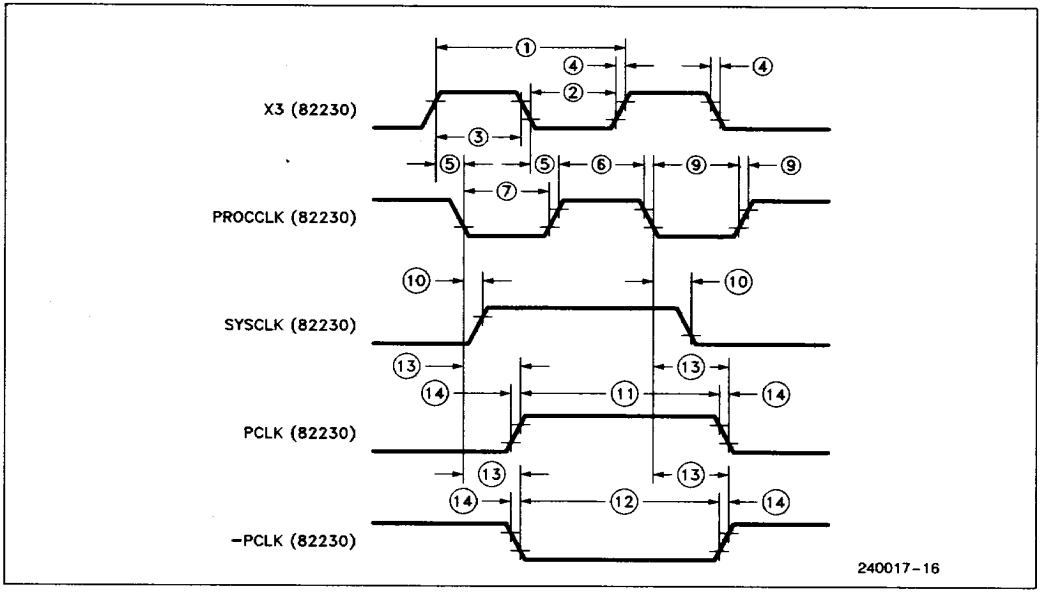


Figure 2. 82230 Clock Timing

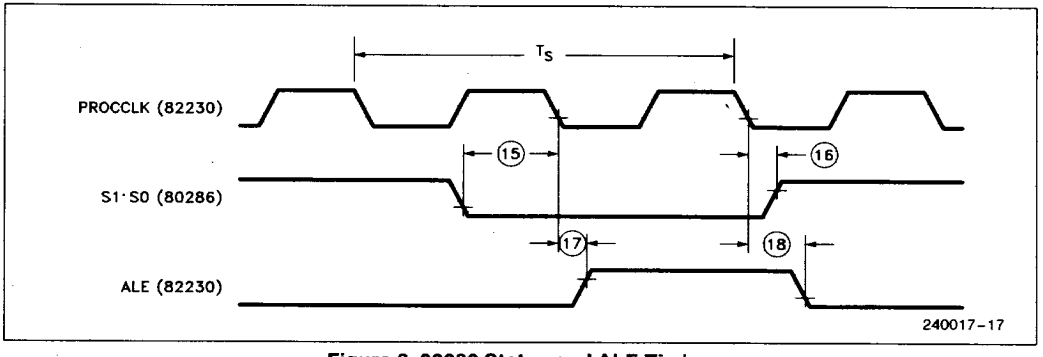


Figure 3. 82230 Status and ALE Timing

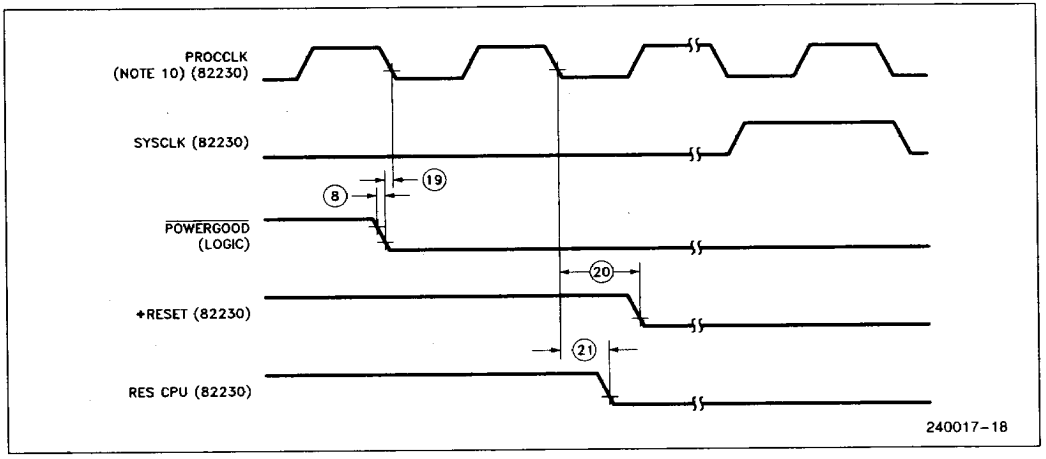


Figure 4. 82230 Power on Initiated Reset

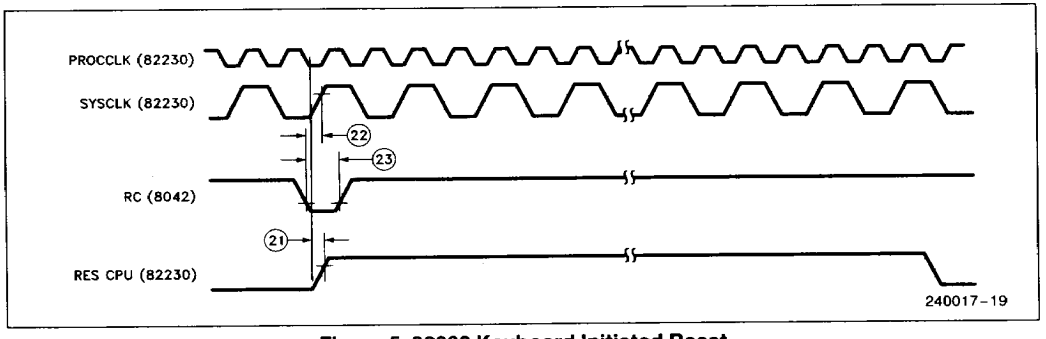


Figure 5. 82230 Keyboard Initiated Reset

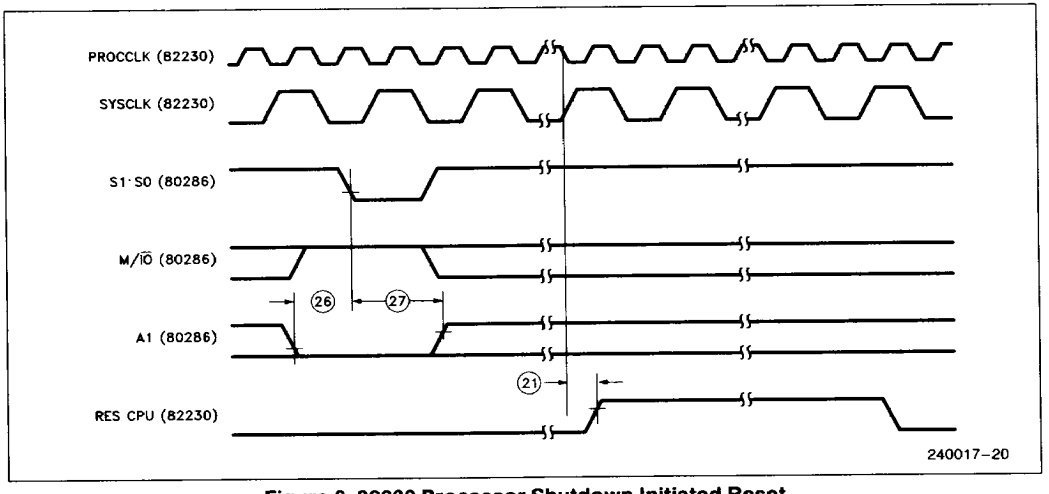


Figure 6. 82230 Processor Shutdown Initiated Reset

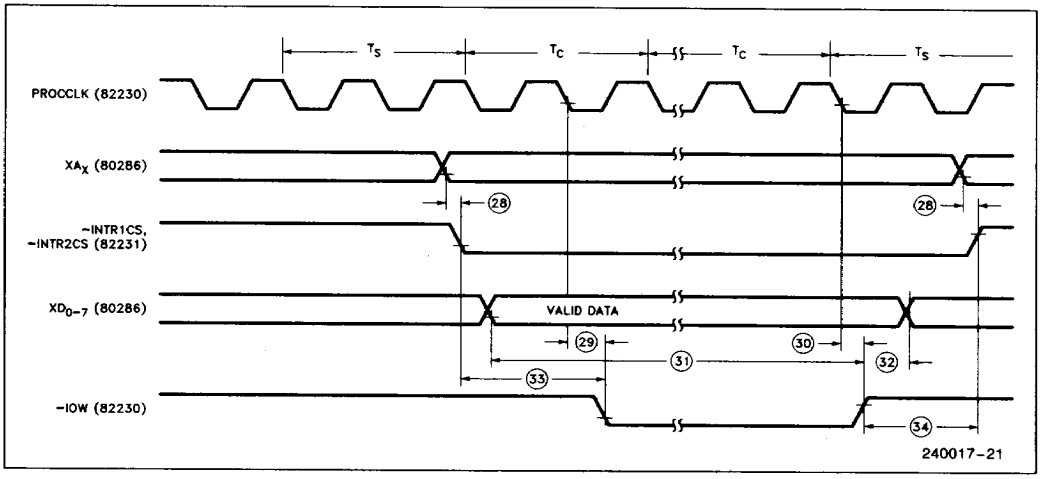


Figure 7. 82230 8254 Bus Write Timing

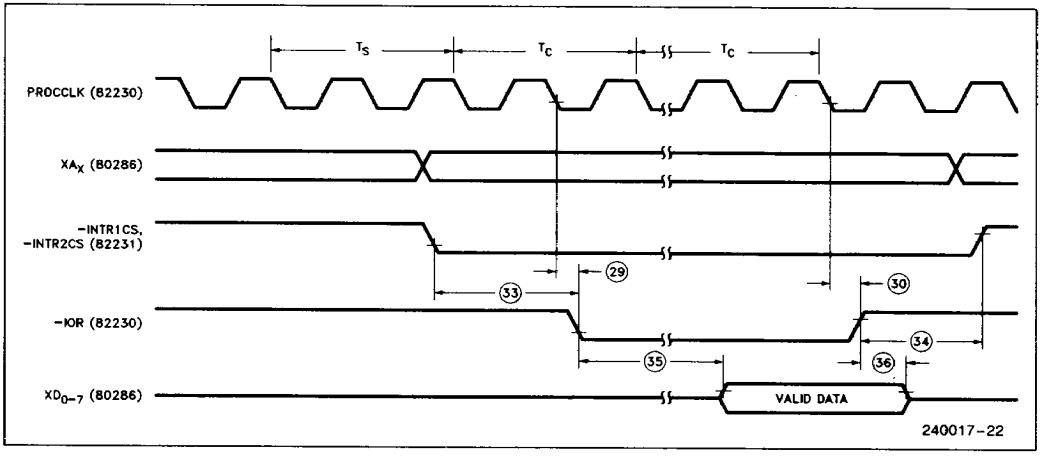


Figure 8. 82230 8254 Bus Read Timing

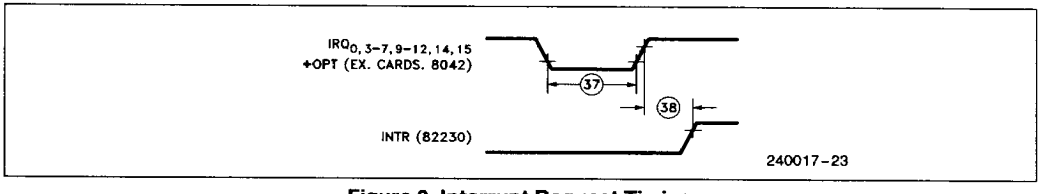


Figure 9. Interrupt Request Timing

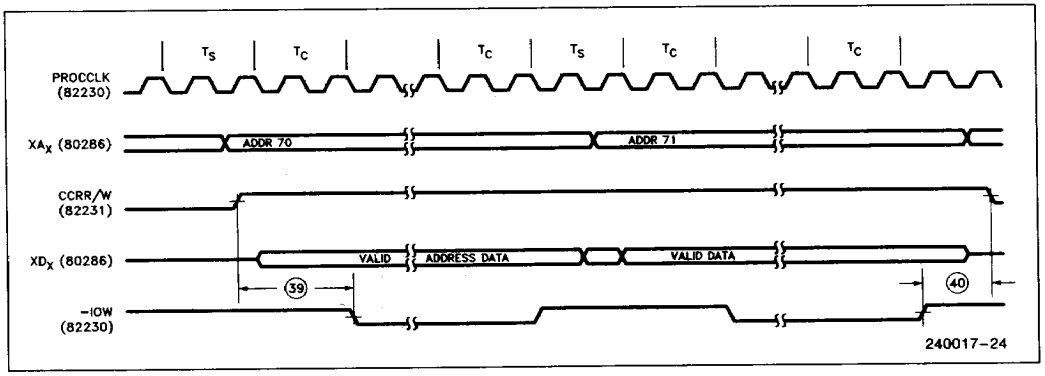


Figure 10. 82230 6818 Write Cycle

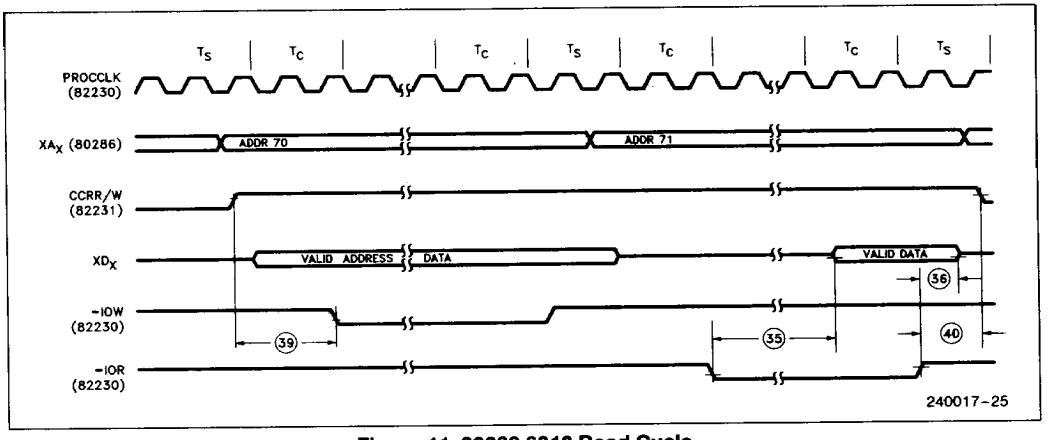


Figure 11. 82230 6818 Read Cycle

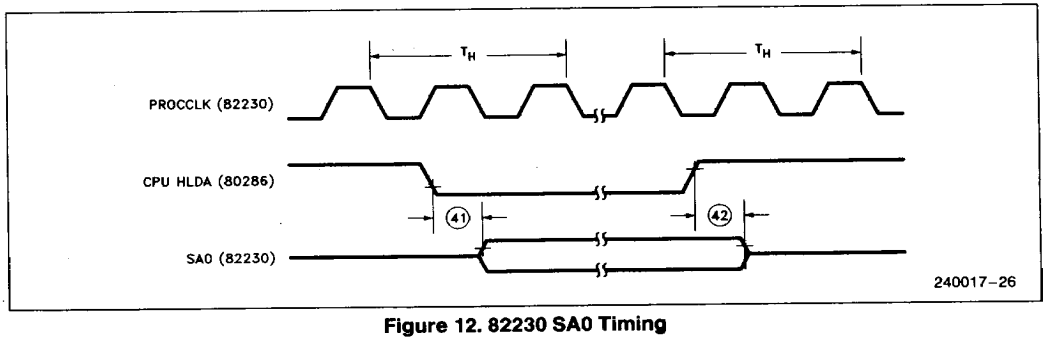


Figure 12. 82230 SA0 Timing

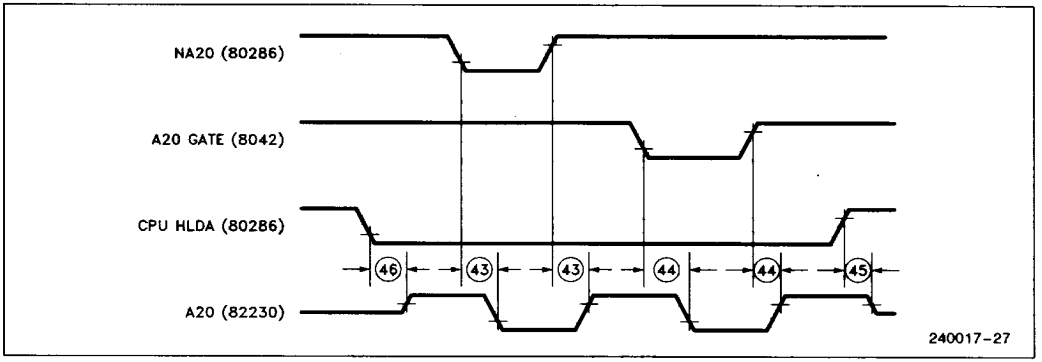


Figure 13. 82230 A20 Timing

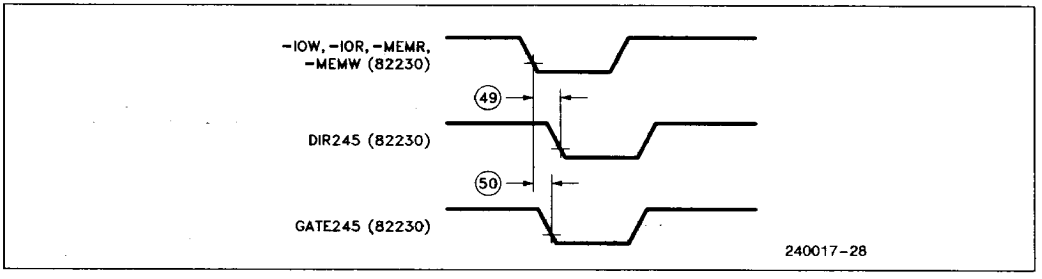


Figure 14. 82230 DIR245, GATE245 Timing

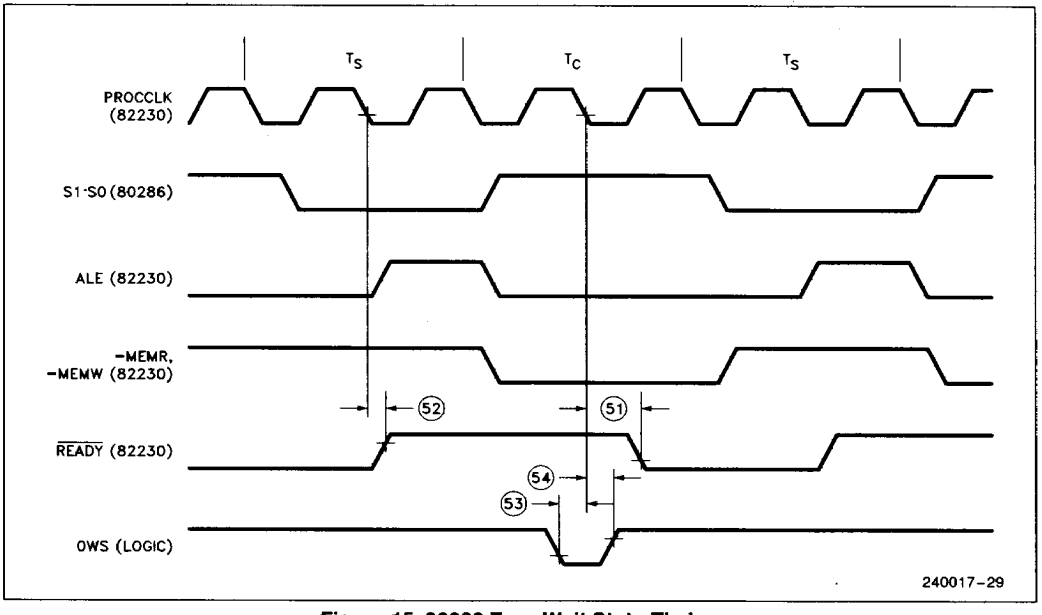


Figure 15. 82230 Zero Wait State Timing

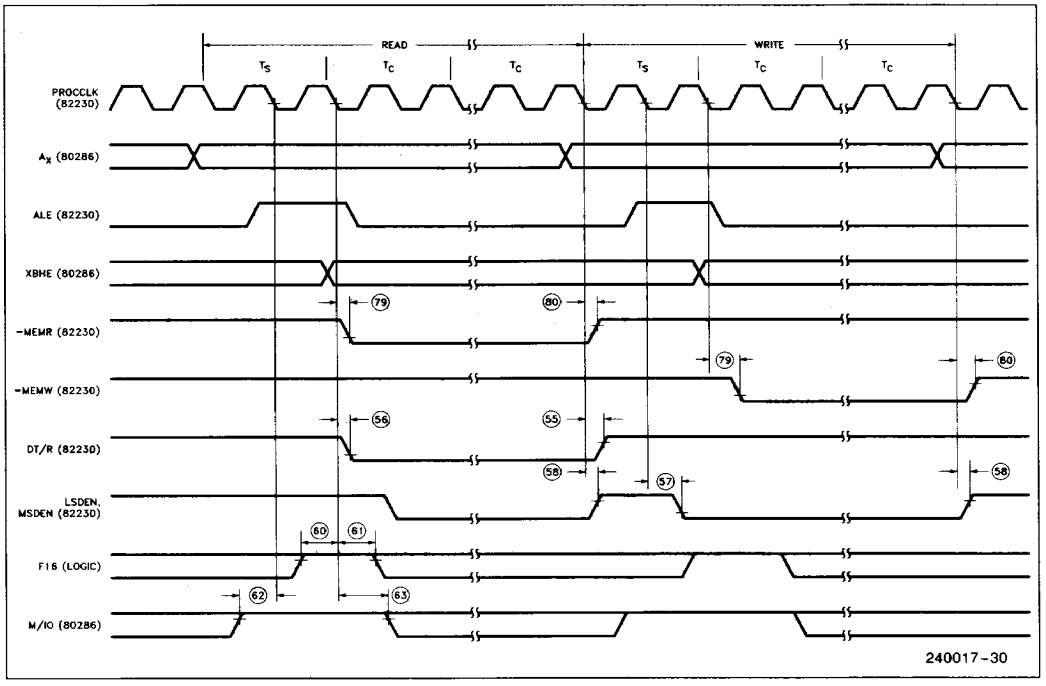


Figure 16. Memory Read/Write Cycles

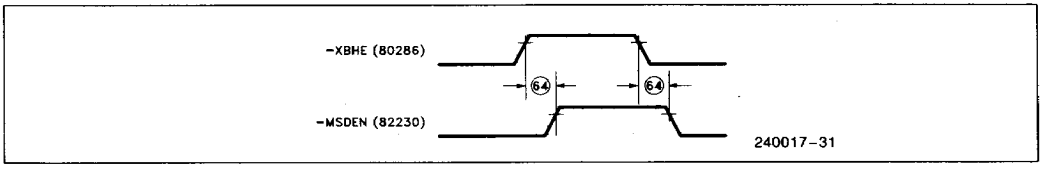


Figure 17. 82230 XHBE Timing

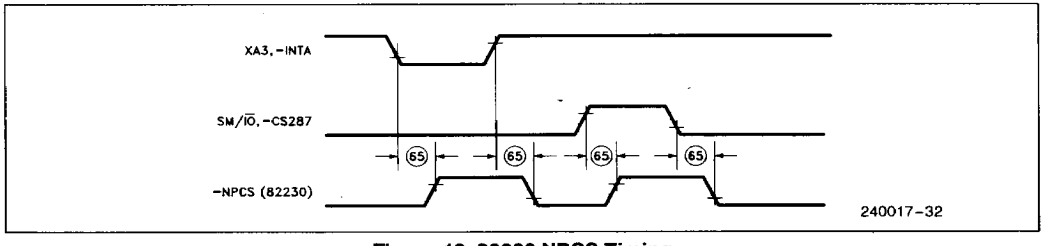


Figure 18. 82230 NPCS Timing

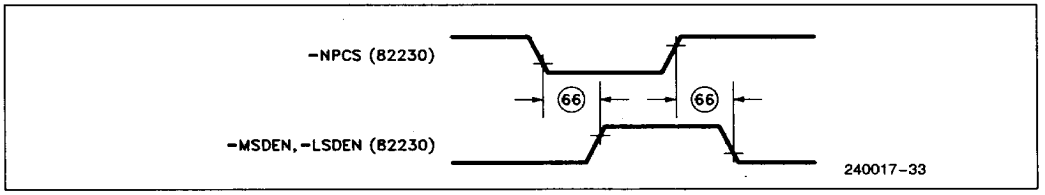


Figure 19. 82230 MSDEN, LSDEN Timing

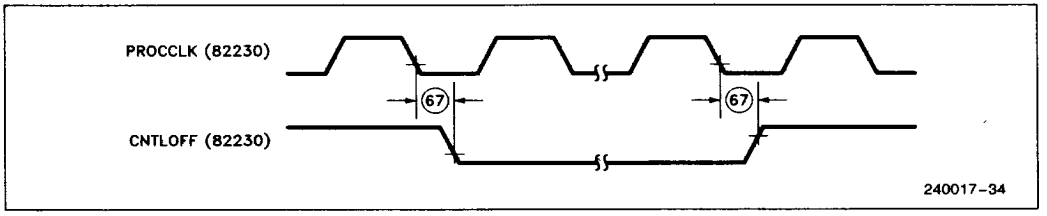


Figure 20. CNTLOFF Timing

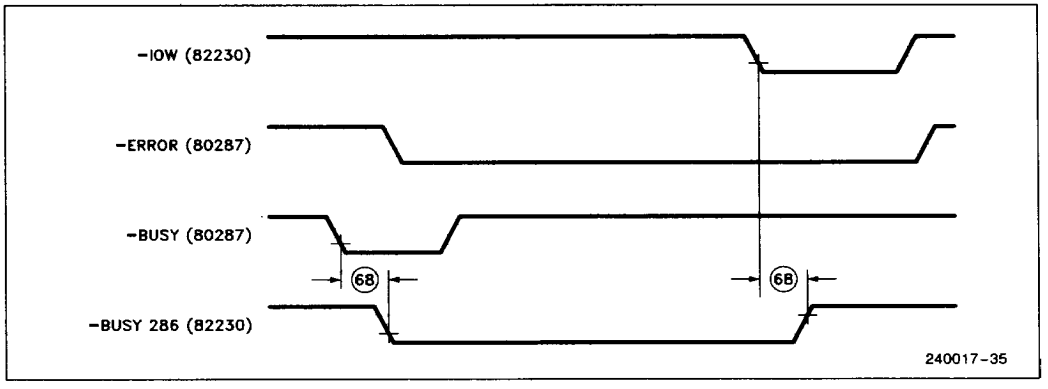


Figure 21. −BUSY286 Timing

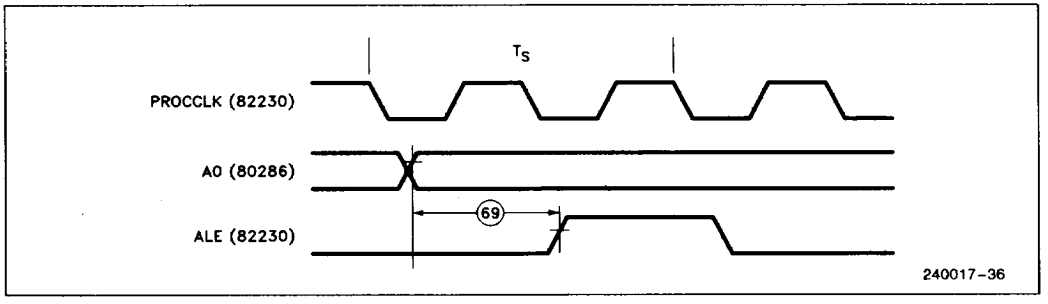


Figure 22. 82230 A0 Timing

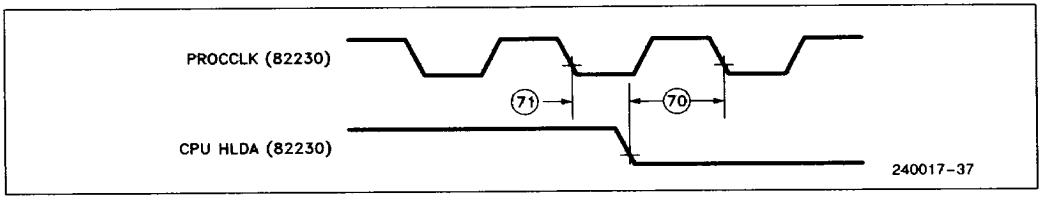


Figure 23. 82230 CPU HLDA Timing

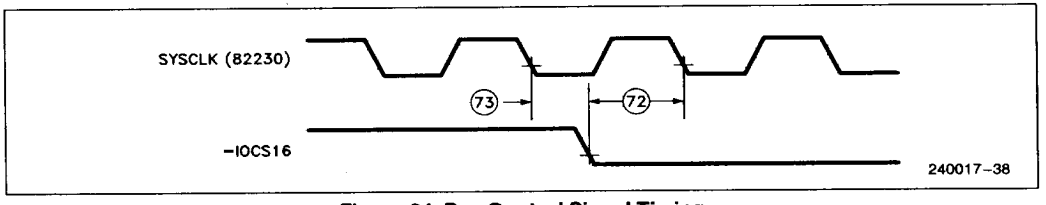


Figure 24. Bus Control Signal Timing

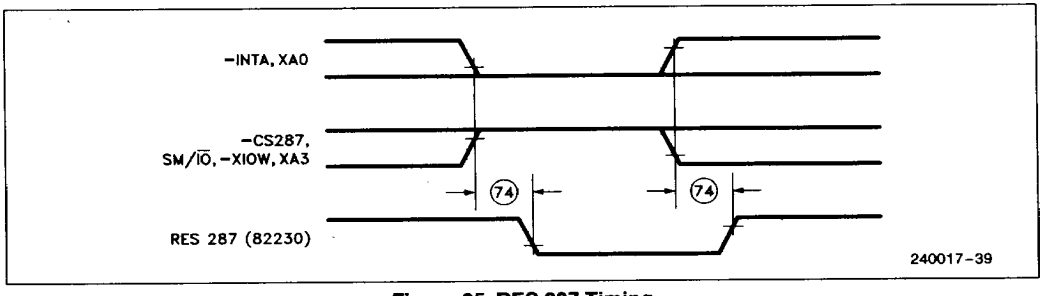


Figure 25. RES 287 Timing

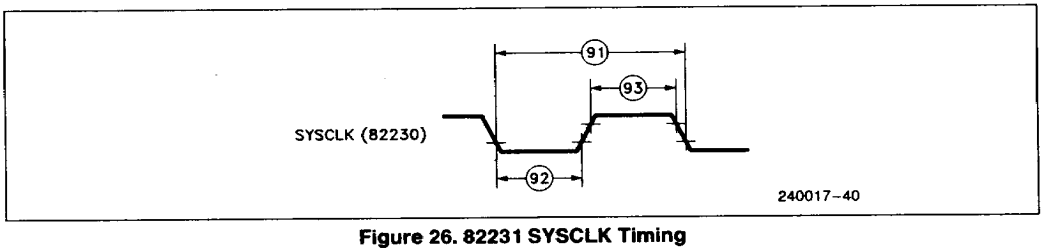


Figure 26. 82231 SYSCLK Timing

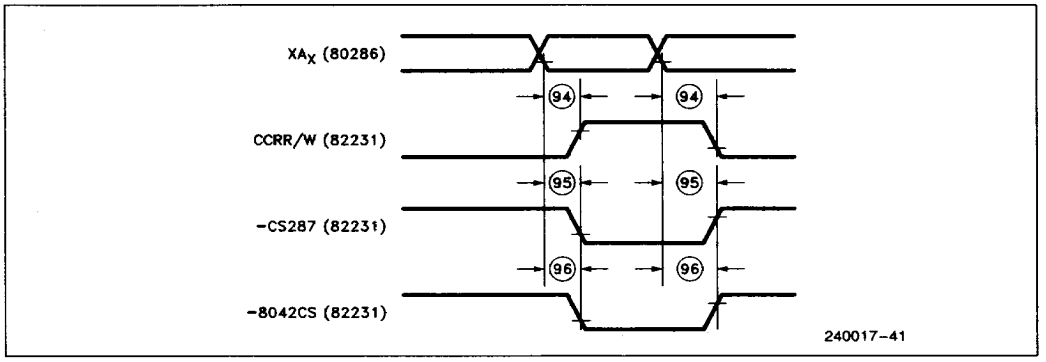


Figure 27. 82231 CCRR/W and CS287 Timing

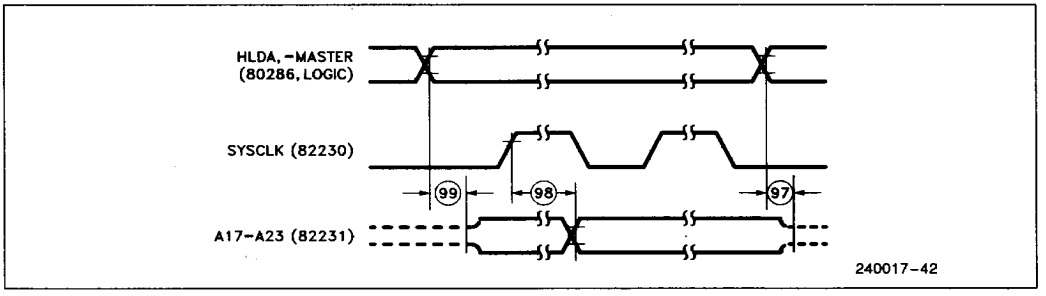


Figure 28. 82231 A17 to A23 Timing

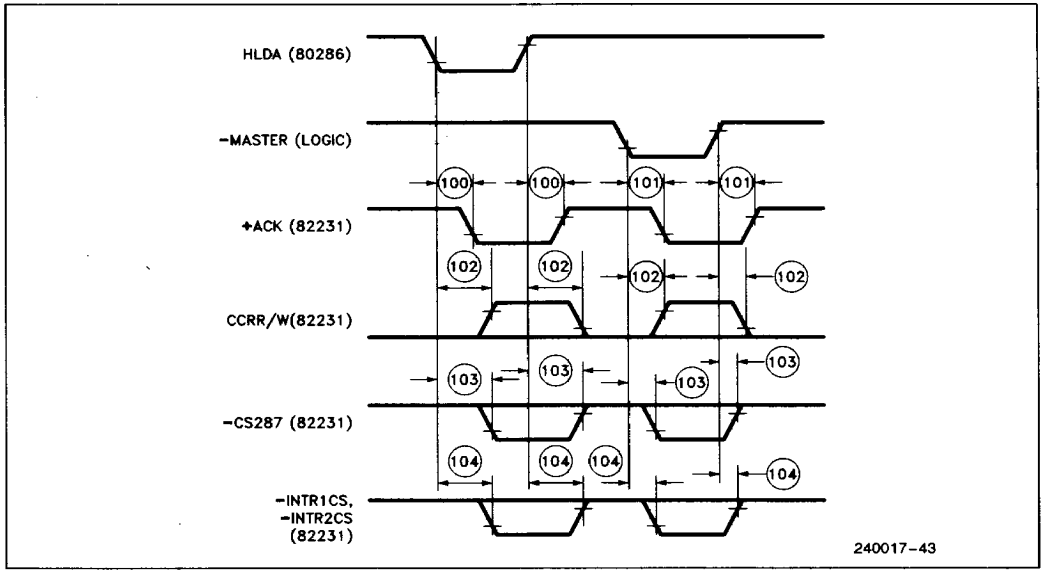


Figure 29. 82231 HLDA & −MASTER Timing

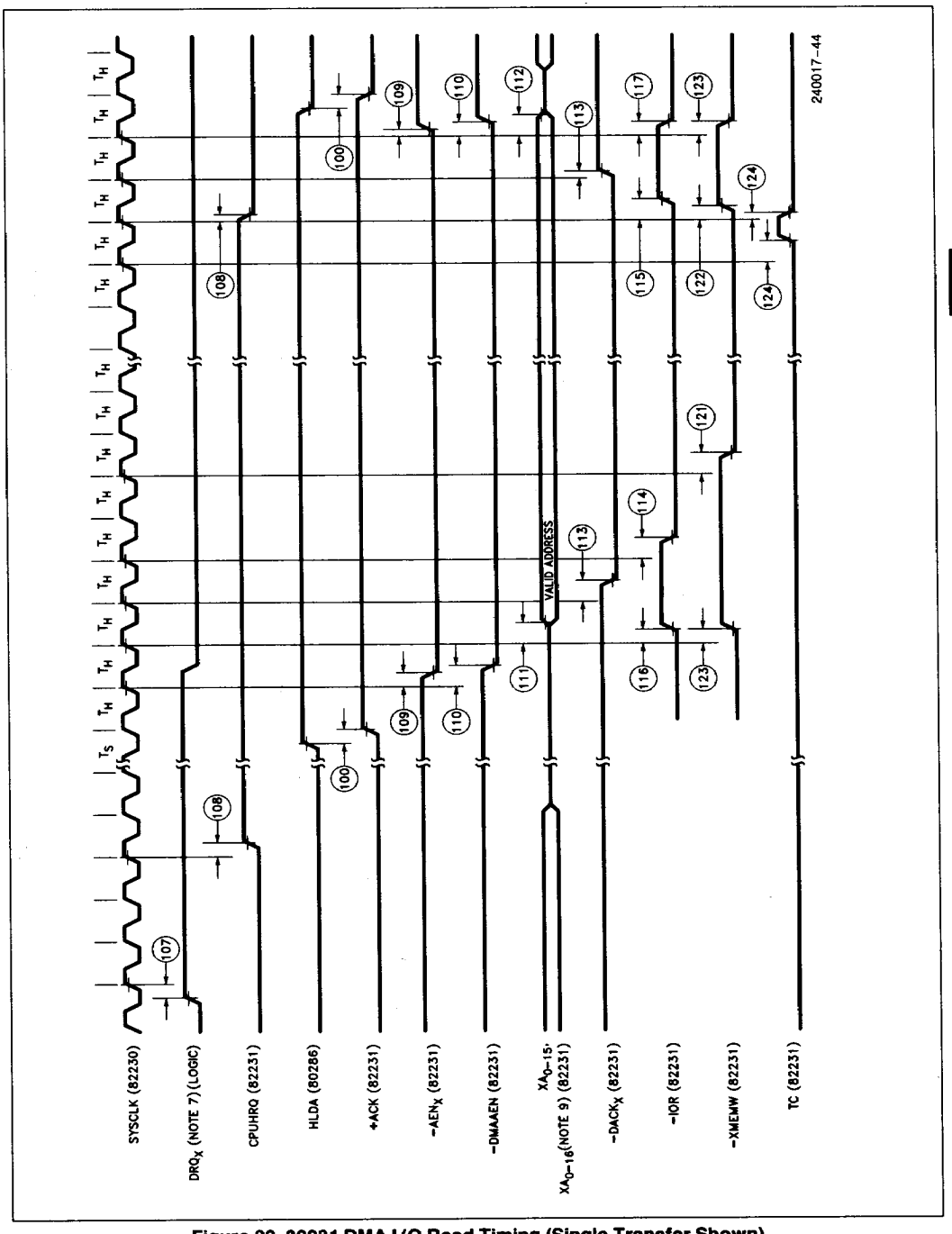


Figure 30. 82231 DMA I/O Read Timing (Single Transfer Shown)

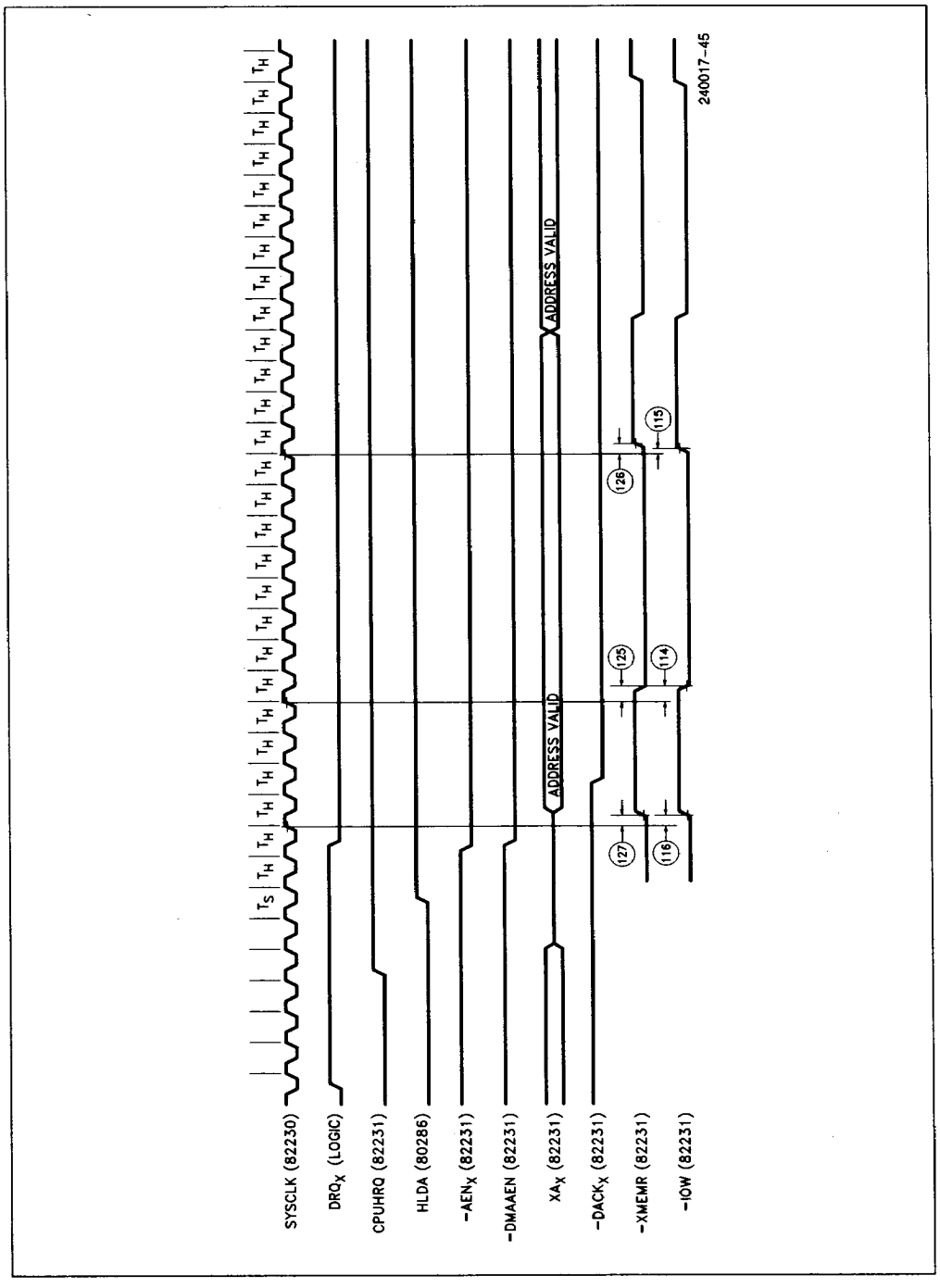


Figure 31. 82231 DMA I/O Write Timing (Block Transfer Shown)

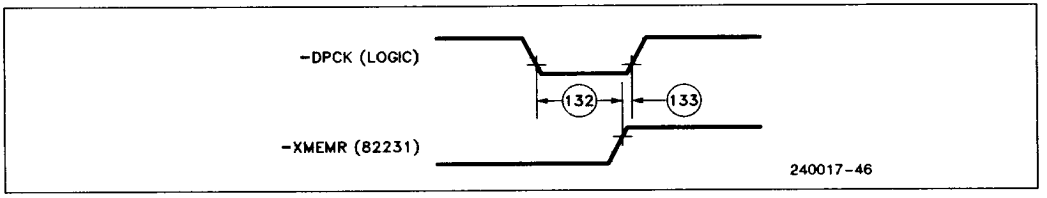


Figure 32. 82231 DPCK Timing

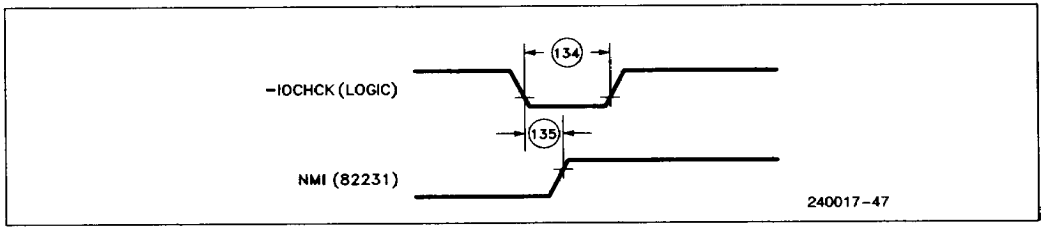


Figure 33. 82231 IOCHCK and NMI Timing

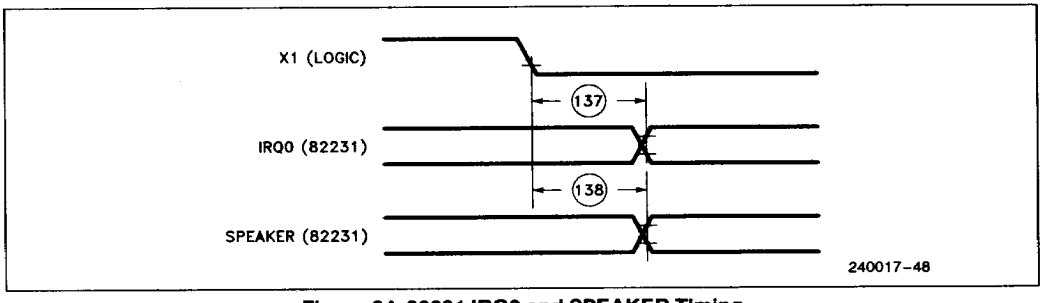


Figure 34. 82231 IRQ0 and SPEAKER Timing

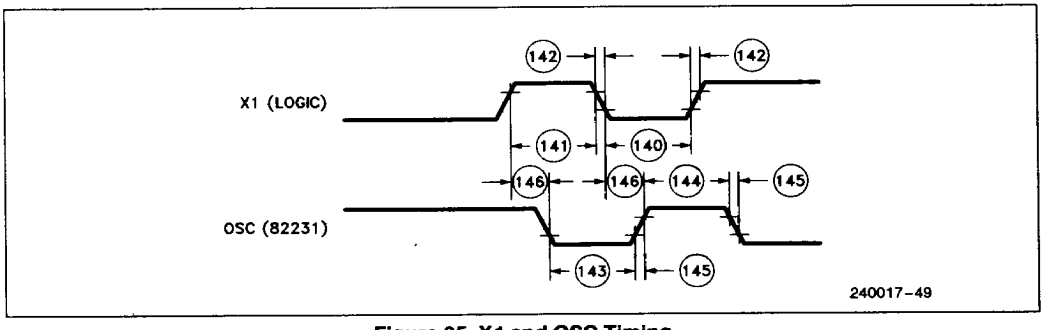


Figure 35. X1 and OSC Timing

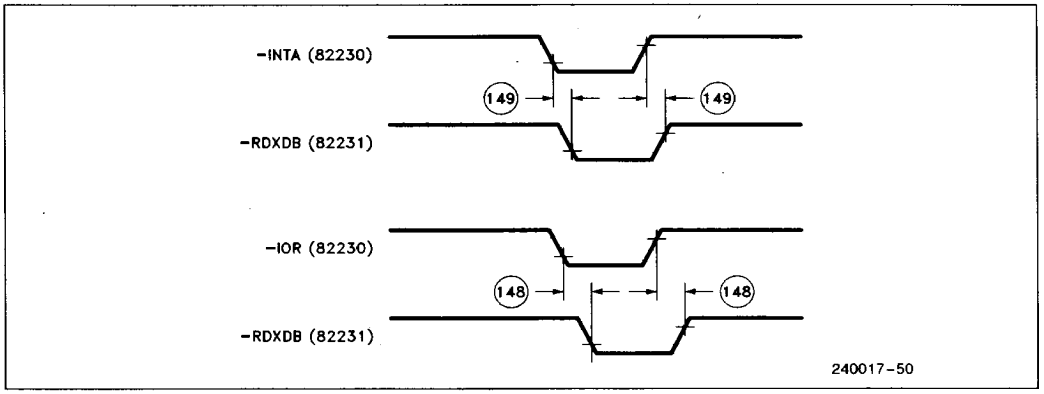


Figure 36. 82231 RDXDB Timing

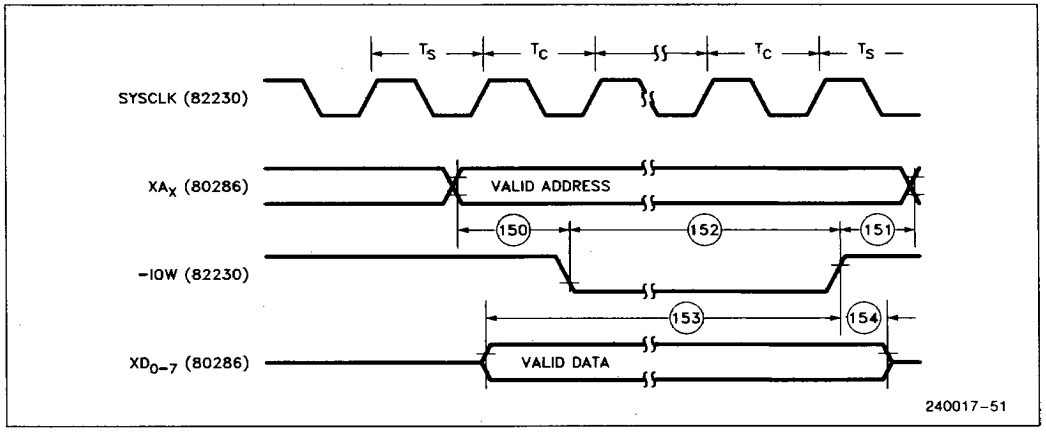


Figure 37. 82231 CPU Write Timing

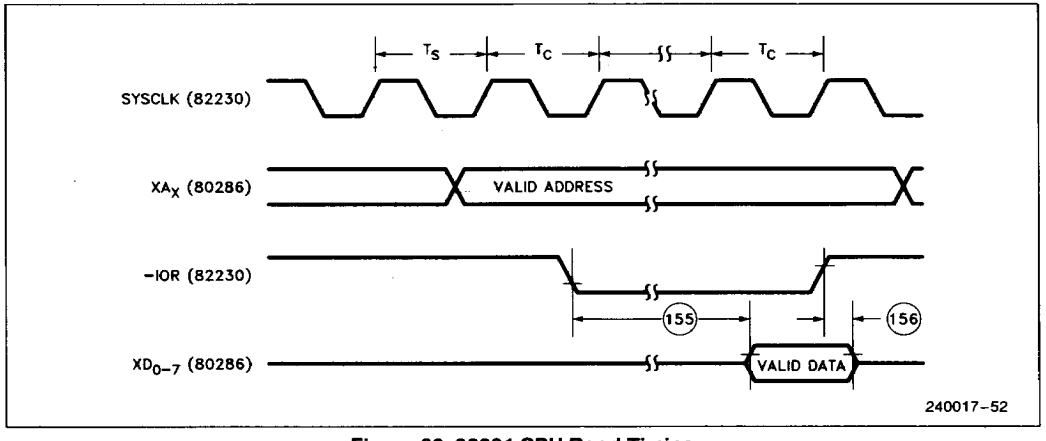


Figure 38. 82231 CPU Read Timing

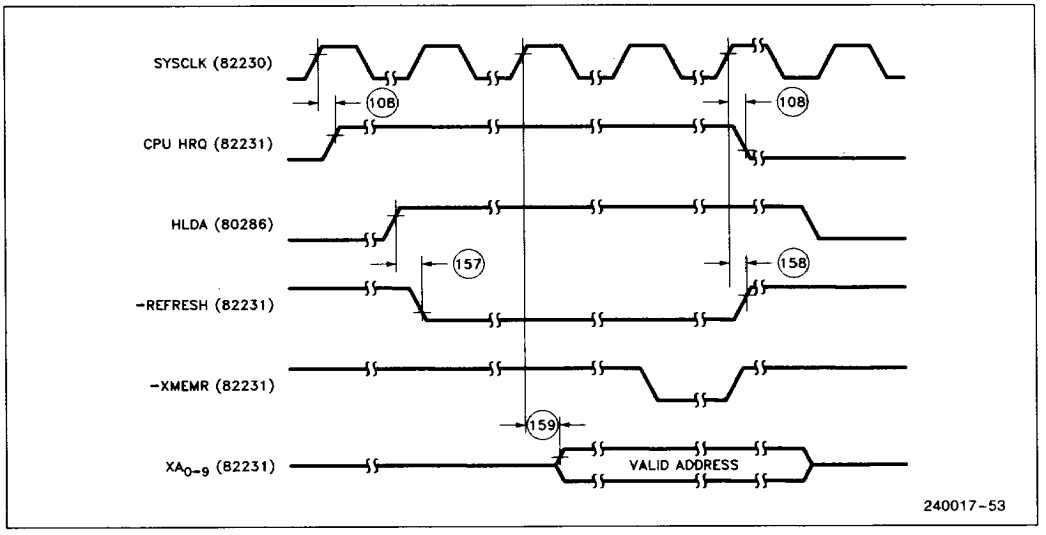
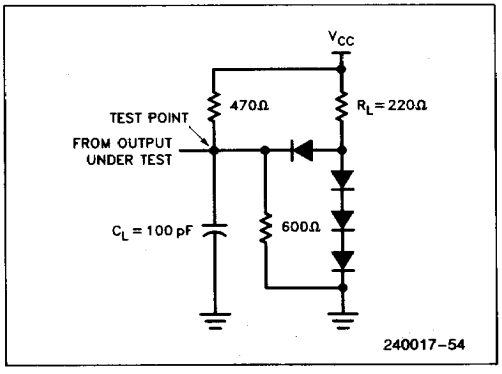


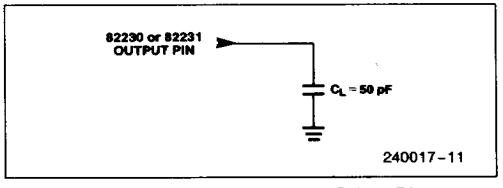
Figure 39. 82231 REFRESH Timing

TEST LOADS

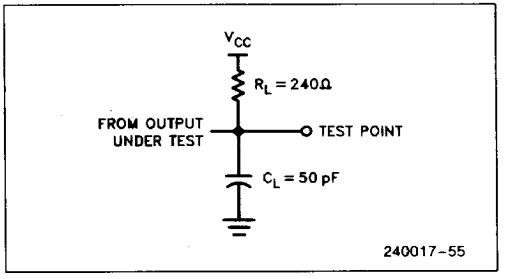


Output Load Circuit

For 82230 pins	SYSCLK
– IOR	– MEMR
– IOW	– MEMW
SA0	
82231 pins – IOR	OSC
– IOW	



Output Load Circuit for All Other Pins



Load Circuit for Open-Collector Output

REVISION HISTORY

The following list represents the differences between this and the -003 version of the data sheet.

1. The 82231 DMA I/O Read Timing diagram was corrected.