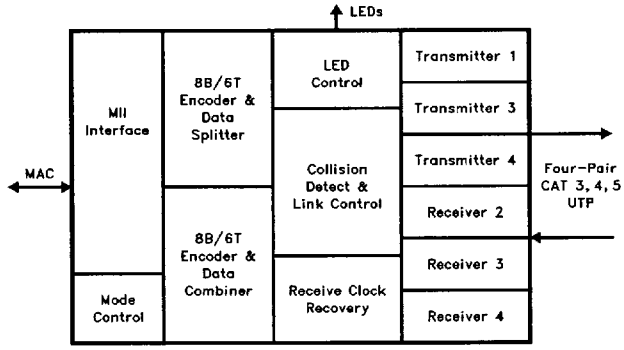
82553
10 Mbps/100 Mbps LAN PHYSICAL LAYER INTERFACE

NOTE:
This datasheet covers two steppings of the 82553 component. All normal text in this document covers both the B and C step parts. Text that is shaded with a gray background pertains only to the C step part.

For example, this text is shaded and pertains only to the C step part.

- **Optimal Integration for Lowest Cost Solution**
  - **— 100Base-T4 IEEE 802.3u Compliance**
  - **— Direct Interface To Single Magnetics Module for 100Base-T4/10Base-T**
  - **— 10Base-T IEEE 802.3 Compliance**
  - **— Full Media Independent Interface (MII) Support**
  - **— Glueless Interface To Intel 10 Mbps/ 100 Mbps Ethernet* Controllers**
  - **— Support for Serial and MII 10 Mbps Modes**
- **High Performance Networking Functions**
  - **— Automatic 100Base-T and 10Base-T Link Detection (Parallel Detection)**
  - **— Autonegotiation Support for Multi-Functional Local Area Networks**
  - **— Digital Adaptive Channel Equalizers Provides Superior S/N Ratio over UTP Media to 125 Meters**
  - **— Built in MII and Line Level Repeater Functions (Class I and II)**
  - **— 10 Mbps Full Duplex Support**
  - **— Power Saving Capability**
  - **— Pin Configurable MII Address in Line Level Repeater Mode**
  - **— Pin Configurable MII Address in Line Level Repeater Mode and MII Repeater Mode**
  - **— SQE support in 10 Mbps Mode**
- **Ease of Use**
  - **— Diagnostic Loopback**
  - **— User Test Modes for Improved Manufacturing Flow**
  - **— Auto Polarity Correction On All Three Receive Pairs**
  - **— Configurable Link, Speed, Activity LED Indicators**



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Note to Hub vendors: Intel and its technology partner, Broadcom Corporation, have an agreement pertaining to the 82553 component. This agreement does not allow Intel to sell the 82553 to hub vendors. Hub vendors should contact Broadcom Corporation directly at (714) 450-8700.

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April 1996 **Order Number: 290547-002**

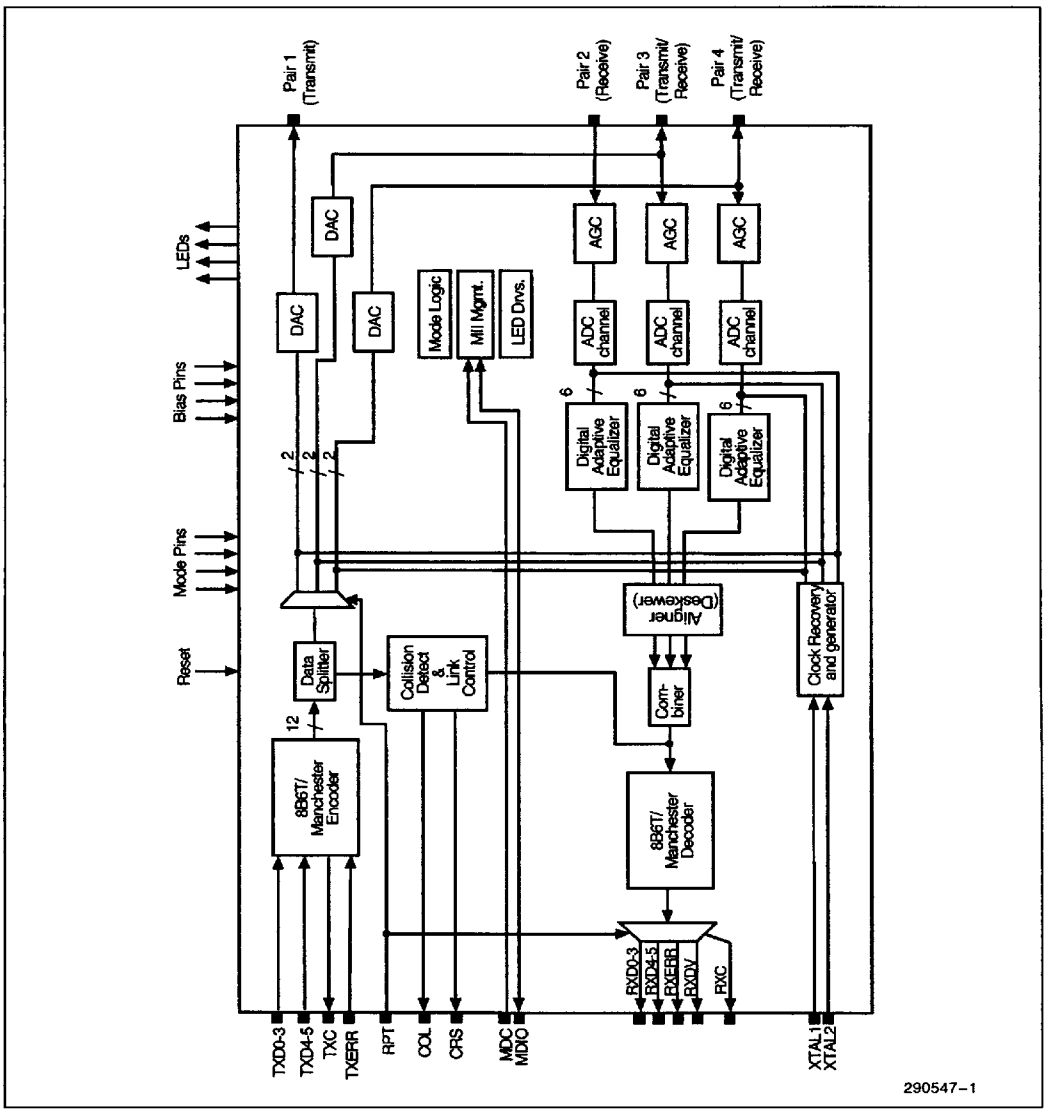

Figure 1. Intel 82553 General Block Diagram

82553
10 Mbps/100 Mbps LAN PHYSICAL LAYER INTERFACE

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TABLES

1.0 82553 INTRODUCTION

The 82553 is a highly integrated, physical layer interface solution designed for 100 Mbps or 10 Mbps Ethernet systems based on the 100Base-T4 and 10Base-T specifications. 100Base-T is the name of the work being done towards 100 Mbps Fast Ethernet by the IEEE 802.3u workgroup. 100Base-T4 is an IEEE 802.3 100 Mbps physical layer specification for use over four pairs of Category 3, 4, or 5 unshielded twisted-pair cable. 100Base-T4 defines a signaling scheme not only for 100 Mbps, but also provides CSMA/CD compatibility with the existing 10 Mbps IEEE 802.3 10Base-T signaling standard.

1.1 82553 Functional Overview

When configured to Adapter Mode, the 82553 incorporates all the active circuitry required to interface 10 Mbps/100 Mbps Ethernet controllers and CSMA/CD MAC components to 100Base-T4 100 Mbps and 10Base-T 10 Mbps networks. In this and other documents the 82553 may be referred to as the PMD, DTE, AFE, or PLM depending on the reference. It supports a direct glueless interface to Intel components such as the 82557 Fast Ethernet controller. The 82553 also supports the Media Independent Interface (MII) signals as a subset of its Controller/MAC interface. The following figure shows how the 82553 fits into a 10 Mbps/100 Mbps Ethernet adapter design.

When configured to MII or Line Level Repeater Mode, the 82553 incorporates several features which allow it to function as a line-level repeater. Section 6.0 describes the 82553 in a repeater type of application.

The 82553 incorporates advanced Digital Signal Processing (DSP) circuits and techniques as well as high-speed Analog circuitry. The 82553 DSP contains advanced circuitry such as digital adaptive equalizers, decision-feedback equalizers and feed-forward equalizers. The 82553 analog subsection contains high speed analog circuitry such as A/D and D/A converters, programmable-gain amplifiers and phase/delay-locked-loop timing recovery. This type of design not only allows the 82553 to meet the IEEE 802.3u 100Base-T4 Physical Layer specification, but also provides additional functionality for cable lengths to 125 meters and noisy cable environments.

The power save feature places the 82553 in a low-power state when there is no transmit activity from the D/A converters.

1.2 82553 Compliance to Industry Standards

When operating in 100 Mbps mode, the 82553 complies with the IEEE 802.3u 100Base-T4 specification. When operating in the 10 Mbps mode, the 82553 complies with the IEEE 802.3 10Base-T specification. The 82553 MAC interface is a superset of the IEEE 802.3u Media Independent Interface (MII) standard.

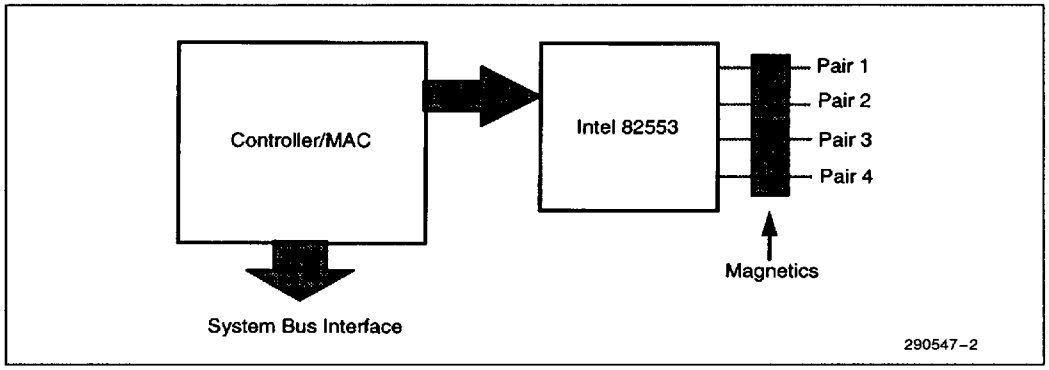

Figure 2. Intel 82553 in a 10 Mbps/100 Mbps Ethernet Solution

2.0 82553 PIN DEFINITIONS

All active digital pins are defined to have TTL voltage levels except the X1 and X2 crystal inputs. These have a separate, specific electrical definition pertaining to the type of crystal or oscillator used (defined by the CLKTYPE pin). The TD and RD pins are specified as analog outputs and inputs.

Figure 3 shows the pin locations on the 82553 component. Sections 2.1 through 2.8 describe pin functions.

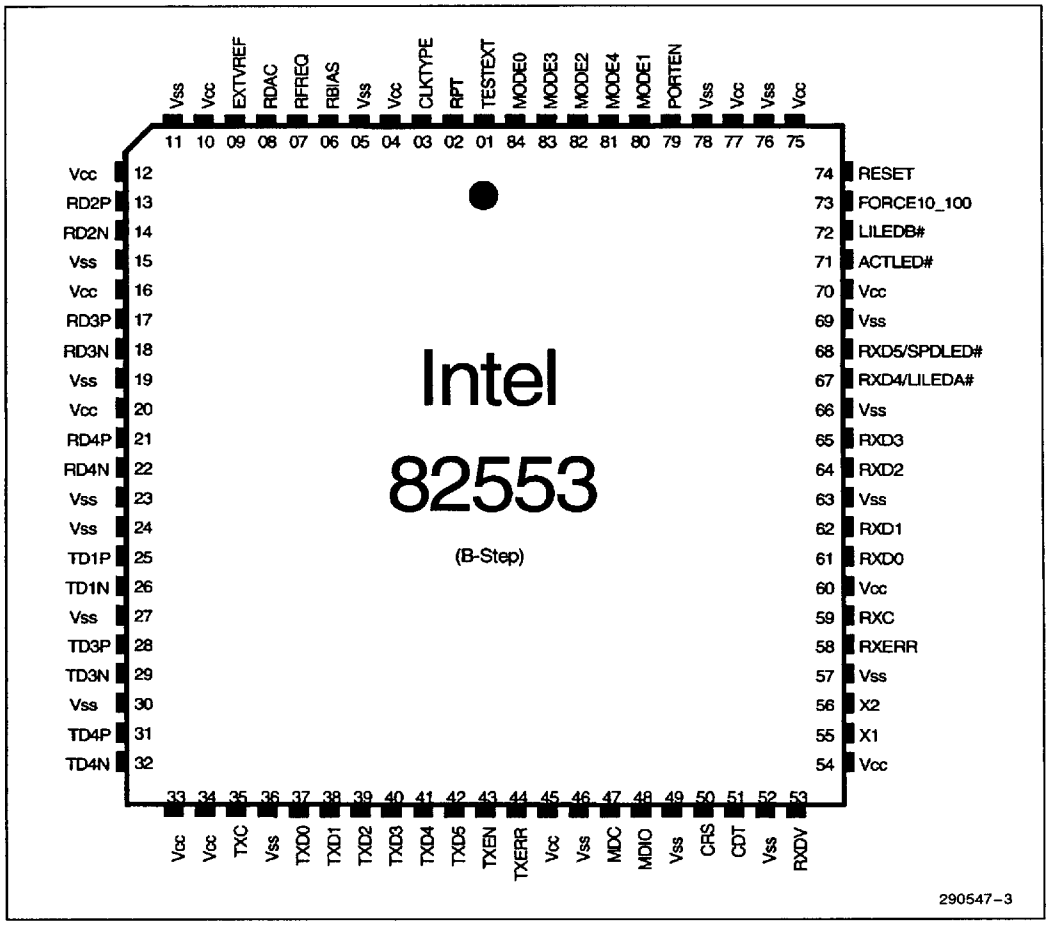

Figure 3. Intel 82553 Pin Numbers and Labels

Note: C-Step Pin Function Changes:
67 = RXD4/LILED#
72 = FDXLED#

2.1 Pin Types

Pin Type	Description
P	Power (V_{CC}) or Ground (V_{SS}) Pin
I	Input Pin to 82553
O	Output Pin from 82553
I/O	Input/Output Pin
B	Bias Pin (Connected to AGND Via a Resistor, or an External Voltage Reference)

2.2 Clock Pins

Symbol	Type	Pin No.	Name and Function
X1	I	55	**CRYSTAL INPUT ONE.** When CLKTYPE = 0, X1 and X2 can be driven by an external 20 MHz crystal. When CLKTYPE = 1, this pin can be driven by an external MOS level 50 MHz oscillator if X2 is floating.
X2	O	56	**CRYSTAL OUTPUT TWO.** When CLKTYPE = 0, X1 and X2 can be driven by an external 20 MHz crystal. When CLKTYPE = 1, the X1 pin can be driven by an external MOS level 50 MHz oscillator if this pin is floating.
CLKTYPE	I	3	**CLOCK TYPE.** Selects 20 MHz crystal or 50 MHz oscillator. When asserted "0", a 20 MHz crystal is connected to pin X1. When asserted "1", a 50 MHz oscillator is connected to pin X1. This pin enables the use of two external clock inputs, 20 MHz or 50 MHz.

2.3 TPE Pins

All TPE pins directly interface with a 100Base-T4 magnetics module.

Symbol	Type	Pin No.	Name and Function
TD1P TD1N	O‡	25 26	Transmit Pair 1
RD2P RD2N	I	13 14	Receive Pair 2
TD3P TD3N	O‡	28 29	Transmit Pair 3
RD3P RD3N	I	17 18	Receive Pair 3
TD4P TD4N	O‡	31 32	Transmit Pair 4
RD4P RD4N	I	21 22	Receive Pair 4

NOTE:
‡ = These analog signals are "open drain" drivers.

2.4 MAC/MII Interface Pins

Symbol	Type	Pin No.	Name and Function
RXD0 RXD1 RXD2 RXD3	O	61 62 64 65	**RECEIVE DATA OUTPUTS.** In 100 Mbps mode, data is transferred across all four lines, a nibble at a time. In 10 Mbps mode, data is transferred on RXD0 only when PAR__SER (MODE3) = 0, and on RXD0–3 nibble wide when PAR__SER (MODE3) = 1.
RXD4 RXD5	O†	67 68	**REPEATER RECEIVE DATA OUTPUTS.** In Line Level Repeater mode, data is transferred across RXD4–5 with RXD0–3.
RXC	O	59	**RECEIVE CLOCK.** 25/10/2.5 MHz output. This clock is recovered directly from the incoming data. In 100 Mbps mode, RXC is 25 MHz. In 10 Mbps mode, RXC is 10 MHz when PAR__SER (MODE3) is asserted low, and 2.5 MHz when PAR__SER (MODE3) is asserted high. RXC is a continuous clock into the Controller/MAC. It must be resynchronized at the start of each incoming packet.
RXDV	O	53	**RECEIVE DATA VALID.** Qualifies incoming data on the RXD pins. Synchronized to RXC.
RXERR	O	58	**RECEIVE ERROR.** Indicates that an error has occurred during a received frame.
PORTEN	I†	79	**PORT ENABLE.** In Line Level Repeater mode (RPT = 1) this input tri-states RXC, RXD0-5, RXDV and RXER when PORTEN = 0.
TXD0 TXD1 TXD2 TXD3	I	37 38 39 40	**TRANSMIT DATA INPUT.** In 100 Mbps mode, data is transmitted across all four lines, a nibble at a time. In 10 Mbps mode, data is transferred to 82553 on TXD0 only when PAR__SER (MODE3) = 0 and on TXD0–3 nibble wide when PAR__SER (MODE3) = 1.
TXD4 TXD5	I	41 42	**REPEATER TRANSMIT DATA INPUT.** In Line Level Repeater mode, data is transferred across TXD4–5 with TXD0–3. Note that TXD4 is also used to enable Repeater Mode. See Section 6.0.
TXC	O	35	**TRANSMIT CLOCK.** 25/10/2.5 MHz output. In 100 Mbps mode, TXC is 25 MHz. In 10 Mbps mode, TXC is 10 MHz when PAR__SER (MODE3) is asserted low, and 2.5 MHz when PAR__SER (MODE3) is asserted high. TXC is continuously driven to the Controller/MAC and is generated directly from CLK.
TXEN	I	43	**TRANSMIT ENABLE.** Indicates that data is valid on TXD0–3.
TXERR	I	44	**TRANSMIT ERROR.** Indicates there has been an error during a transmit frame.
CRS	O	50	**CARRIER SENSE.** Indicates activity on the wire. CRS is an asynchronous output signal to the controller.
CDT	O	51	**COLLISION DETECT.** In half-duplex mode, CDT indicates a collision has occurred on the link. CDT is an asynchronous output signal to the controller.
MDIO	I/O	48	**MANAGEMENT DATA I/O.** Bi-directional data pin for the Management Data Interface.
MDC	I	47	**MANAGEMENT DATA CLOCK.** Clock reference for MDIO. MDC frequency should be less than 2.5 MHz.

NOTE:
† = Denotes a bias pin. Must be connected to a voltage source or resistor.

2.5 Mode Pins

Symbol	Type	Pin No.	Name and Function		
RPT	I	2	**REPEATER ENABLE/DISABLE.** Puts 82553 into Line Level Repeater mode which enables RXD4-5 and TXD4-5 and bypasses the 8B6T decoder. RPT (low) is also used along with TXD4 (high) to enable MII Repeater mode.		
TESTEXT	I	1	**EXTERNAL TEST INPUT CONTROL.** When asserted 1, enables one of several test modes. These modes are controlled by the test address input pins TESTA0–4 (MODE0–4).		
FORCE100_10	I	73	**FORCE 100 OR 10 MBPS MODE.** This mode input is effective when AUTOSPSEL = 0, i.e., 82553 is in manual speed select. When asserted 1, 82553 is manually forced to be at 100 Mbps. When asserted 0, 82553 is selected to be at 10 Mbps mode.		
MODE4 (AUTOSPSEL/ PHYA4/ TESTA4)	I	81	**If RPT =**	**If TESTEXT =**	**Then MODE4 Function is:**
			0	0	**Automatic Speed Select.** When asserted "1" 82553 is at automatic speed detection mode. When asserted "0", 82553 is at manual speed detection mode.
			1	0	**PHY Address Input 4.** In multiple PHY configuration, the address of a specific PHY chip is determined by PHYA0–4 pins. PHYA4 is bit number 4.
			X	1	**Test Address Mode Pin 4 Input.** When TESTEXT is asserted "1", TESTA4 is bit 4 of the test mode address input.
MODE3 (PARSER/ PHYA3/ TESTA3)	I	83	If RPT =	If TESTEXT =	**Then MODE3 Function is:**
			0	0	**Parallel Serial Mode.** This mode affects to 10 Mbps mode only. When asserted "1", the 82553 processes nibble wide data (MII mode) on TXD0–3 inputs and outputs data on RXD0–3. When asserted "0", 82553 processes data serially (serial mode), on TXD0 and RXD0.
			1	0	**PHY Address Input 3.**
			X	1	**Test Address Mode Pin 3 Input.** TESTA3 is bit 3 of the test mode address input.

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2.5 Mode Pins (Continued)

Symbol	Type	Pin No.	Name and Function		
MODE2 (TRISTT/ PHYA2 TESTA2)	I	82	If RPT =	If TESTEXT =	**Then MODE2 Function is:**
			0	0	**82553 Tri-State.** If TRISTT = "1", the 82553 Tri-states all 82553 active outputs and puts inputs into a predefined state. Used for board debug. This pin also functions as an I_{DD}.
					Quiescent Mode. IDDQ is used for low current power—on-chip screening test. When IDDQ is high, all current sources are disabled. When IDDQ is low, current sources will be in normal operation.
			1	0	**PHY Address Input 2.**
			X	1	**Test Address Mode Pin 2 Input.** TESTA2 is bit 2 of test mode address input.
MODE1 (LPBK/ PHYA1/ TESTA1)	I	80	If RPT =	If TESTEXT =	**Then MODE1 Function is:**
			0	0	**Loopback Enable.** When LPBK = 1, 82553 is in Digital Loopback mode. When LPBK = 0, 82553 is in normal operation.
			1	0	**PHY Address Input 1.**
			X	1	**Test Address Mode Pin 1 Input.** TESTA1 is bit 1 of test mode address input.
MODE0 (PHYA0/ TESTA0)	I	84	If RPT =	If TESTEXT =	**Then MODE0 Function is:**
			X	0	**PHY Address Input 0.**
			X	1	**Test Address Mode Pin 0 Input.** When TESTEXT is asserted "1", TESTA0 is bit 0 of test mode address input.
RESET	I	74	**RESET.** Active high resets the 82553. Reset pulse width minimum of 600 ns should be used.		

2.6 External Bias Pins (Internal Use Only)

Symbol	Type	Pin No.	Name and Function
EXTVREF	B†	9	**EXTERNAL VOLTAGE REFERENCE.** This pin is connected to a 2.7V ± 5% external voltage reference diode.
RBIAS	B	6	**BIAS REFERENCE RESISTOR.** A resistor of 20 KΩ should be connected from RBIAS pin to AGND.
RDAC	B	8	**DAC BIAS RESISTOR.** Adjusts the current level of the TX DAC. A resistor of 22.1 KΩ should be connected from RDAC to AGND.
RFREQ	B	7	**CENTER FREQUENCY RESISTOR.** The center frequency of the clock generator is controlled by connecting a resistor of 20 KΩ between this pin to AGND.

NOTE:
† = Denotes a bias pin. Must be connected to a voltage source or resistor.

2.7 LED Pins (B1 Stepping Only)

Symbol	Type	Pin No.	Name and Function
ACTLED#	O	71	**ACTIVITY LED.** This LED indicates either transmit or receive activity. When there is activity, ACTLED is on (low). When there is no activity, ACTLED is off (high). When configured to MII or Line-Level Repeater mode, indicates receive activity only.
SPDLED#	O	68	**SPEED LED.** In MII or Adapter mode, this LED indicates the link speed. In 100 Mbps mode, the SPDLED is on (low). In 10 Mbps mode, this LED is off (high).
LILEDA#	O	67	**LINK INTEGRITY LED.** In MII or adapter mode, this LED indicates link beat integrity (valid link for either 10Base-T or 100Base-T4). When there is no link integrity, LILEDA# is off (high). When there is a valid link, this LED is on (low).
LILEDB#	O	72	**LINK INTEGRITY LED.** In Line-Level Repeater mode and 10Base-T mode, this LED indicates link beat integrity. When there is no link integrity, LILEDB is off (high). When there is a valid link, this LED is on (low). In 100 Mbps mode, LILEDB# blinks on and off during a valid link. LILEDB# is off when there is no link.

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2.8 LED Pins (C Stepping Only)

Symbol	Type	Pin No.	Name and Function
ACTLED#	O	71	**ACTIVITY LED** Adapter Mode: blinks on transmit and receive. MII Rept. Mode: blinks on receive. LL Rept. Mode: blinks on receive.
SPDLED#	O	68	**SPEED LED** Adapter Mode: on (low) = 100 Mbps; off (high) = 10 Mbps. MII Rept. Mode: on (low) = 100 Mbps; off (high) = 10 Mbps. LL Rept. Mode: not available; used as RXD5.
FDXLED#	O	72	**FULL DUPLEX LED** Adapter Mode: with TXD5 low Full Duplex on (low) = FDX true Full Duplex on (high) = FDX false with TXD high FDX blinks with a valid link and is off without a valid link. MII Rept. Mode: indicates link beat integrity. On = valid link; off = no valid link. LL Rept. Mode: on (low) = link pass; off (high) = link fail.
LILED#	O	67	**LINK INTEGRITY LED** Adapter Mode: on (low) = link pass; off (high) = link fail MII Rept. Mode: on (low) = link pass; off (high) = link fail LL Rept. Mode: not available; used as RXD5

2.9 Power Pins

Symbol	Type	Pin No.	Name and Function
V_{CC}	P	10, 12, 16, 20, 33, 77, 4, 34, 45, 75, 54, 60, 70	**Analog and digital power.** +5.0V ± 5%.
V_{SS}	P	11, 15, 19, 23, 24, 27, 30, 78, 5, 36, 46, 76, 49, 52, 57, 63, 66, 69	**Analog and digital ground.** 0V.

3.0 82553 ARCHITECTURE OVERVIEW

The internal architecture of the 82553 is a combination of advanced DSP, analog, and other functional blocks. Figure 1, at the beginning of this document, shows a general block diagram of the 82553 component.

In 100Base-T4 mode, the analog subsection of the 82553 performs three functions:

1. It takes receive analog data from pairs 2, 3 and 4, converts it to 6-bit digital representation, and passes it to the digital subsection.
2. It recovers receive timing from the three receive pairs, applies programmable gain, and forwards it to the digital subsection.
3. It takes transmit data in 2-bit digital form, translates it into an analog waveform, and transmits it on pairs 1, 3 and 4.

In 100Base-T4 mode, the 82553 digital subsection performs all necessary signal processing of the digital version of the transmit and receive data. This includes 8B/6T encoding and decoding, carrier sense, collision detection, link detection and providing an MII interface to the MAC. The 82553 supports the defined MII as its MAC interface. The 82553 expects that the controller will provide the MDIO and MDC signals.

The 82553 operation in 10Base-T mode is similar. Instead of receiving data on three pairs, only one is used, Manchester encoding and decoding are used in place of 8B/6T, and the TXC/RXC provides 2.5 MHz or 10 MHz instead of 25 MHz. Otherwise, 10Base-T data travel through the same internal 82553 paths as 100Base-T4 data.

The 82553 will interface with Intel components such as the 82557 Fast Ethernet Controller as well as any MII compatible MAC or controller. Figure 4 shows a schematic-level diagram of the 82557 Fast Ethernet controller implementation.

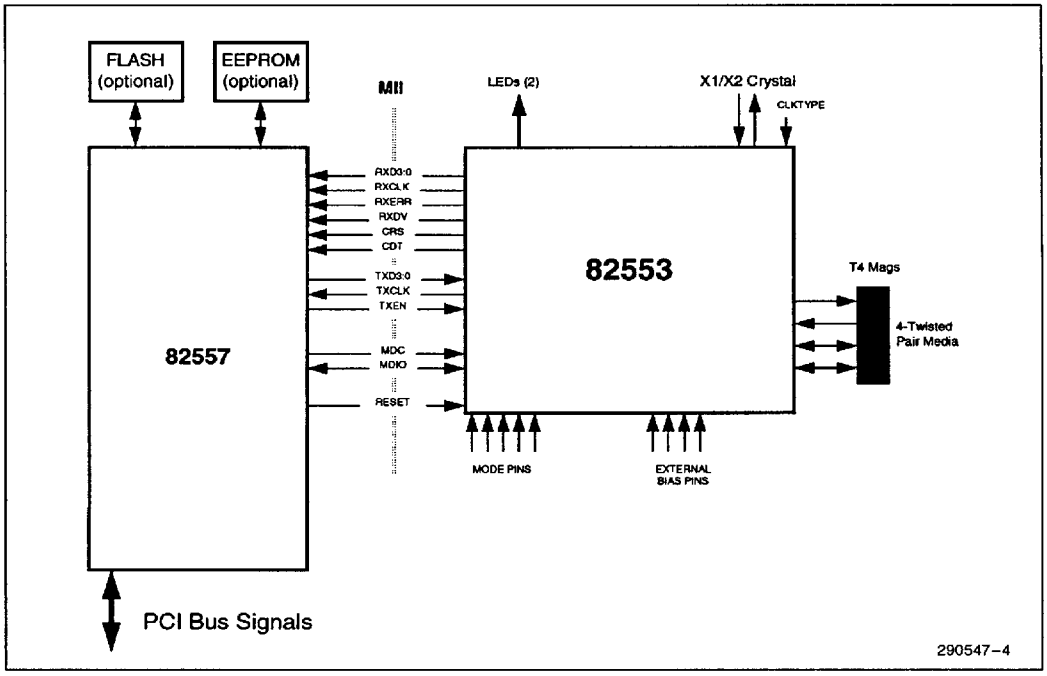

Figure 4. Simplified 82557 Fast Ethernet Controller and 82553 Design Diagram

Table 1. MII Interface

Signal Name	Description	Direction	Clock Reference	MII Signal Supported by 82553
TXC	Transmit Clock	From 82553	—	Yes
TXD0–3	Transmit Data	From MAC	TXC	Yes
TXEN	Transmit Enable	From MAC	TXC	Yes
COL	Collision	From 82553	Asynchronous	Yes
CRS	Carrier Sense	From 82553	Asynchronous	Yes
RXC	Receive Clock	From 82553	—	Yes
RXD0–3	Receive Data	From 82553	RXC	Yes
RXDV	Receive Data Valid	From 82553	RXC	Yes
RXERR	Receive Error	From 82553	RXC	Yes
MDIO	Management Data In/Out	From Manager	MDC	Yes
MDC	Management Data Clock	From Manager	—	Yes
TXERR	Transmit Error	From MAC	TXC	Yes

3.1 82553 MII Interface Support

The 82553 also supports the Media Independent Interface (MII) as its primary interface to the MAC. It also supports a superset of the MII where 10 Mbps data is transferred to the MAC serially at 10 MHz instead of nibble-wide at 2.5 MHz. The MII Interface is summarized in Table 1.

4.0 82553 ADAPTER MODE OPERATION

4.1 82553 Clock Generation

A 20 MHz parallel resonant crystal or 50 MHz oscillator (depending on the level of CLKTYPE) is used to drive the 82553 X1/X2 pins. In 100 Mbps mode, the 82553 derives its internal 25 MHz and 50 MHz digital clock based upon this crystal input. The 82553 will also drive TXC and RXC based on a derivative of this clock. The accuracy of the external crystal or oscillator generally must be ± 0.01%.

4.2 82553 Transmit Blocks

The transmit subsection of the 82553 accepts nibble-wide data on the TXD0–3 inputs when TXEN is active (high). The transmit subsection will pass data unconditionally to the 8B/6T encoder as long as TXEN is active. The transmit interface of the 82553 is compatible with Intel's 82557 controller. Figure 5 shows the 82553 transmit subsection.

The 8B6T Encoder accepts nibble-wide data from the MAC and compiles it into bytes. It then encodes the 8-bit binary data into 12-bit form, which is actually a representation of the 6-bit ternary (6T) code. In 12-bit form, each ternary bit is represented by two binary bits (+1 = 01, 0 = 00, −1 = 10). This 12-bit form is then sent serially to the Multimode DACs where the three-level 6T analog wave is created and transmitted.

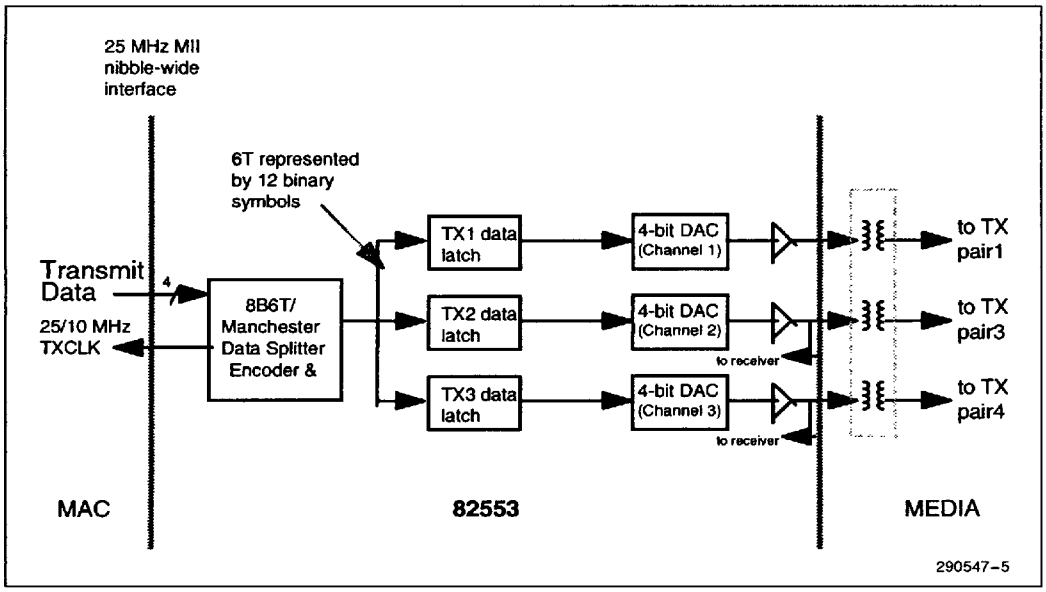

Figure 5. 82553 Transmitter Block Diagram

4.2.1 82553 8B/6T ENCODER AND DATA SPLITTER

The 8B/6T encoder complies with the IEEE 802.3u 100Base-T4 standard. Four bits at a time are accepted at the MII interface and a byte is encoded according to the T4 8B/6T lookup table. The lookup table matches a 6-bit ternary (6T) code to each binary byte. The data is then distributed by the Data Splitter to one of three transmission pairs (pairs 1, 3, or 4). The first data code is always transmitted on pair one, and sequentially after that (1, 3, 4, 1, 3, 4, . . .). Figure 6 shows an example of how the data is presented from the MAC via the MII, encoded, and sent to the TPE cable drivers.

4.2.2 82553 DC BALANCE AND THE INVERSION RULE

DC balance is maintained by the 82553 through the use of the inversion rule. The inversion rule is based on the fact that all 6T codes in the T4 scheme have weights of either 0 or +1. For example, the 6T representation of "40" is "0-00++", which has a weight of +1. The inversion rule states that on a given pair, if a 6T code of weight +1 is transmitted, then the next code of weight +1 to be transmitted on that pair will be inverted, giving it a weight of −1. This guarantees DC balance on any given pair throughout transmission. For instance, in Figure 6, Byte 4 has been inverted on the wire. Since the 6T code for Byte 4 has a weight of +1 and the previous 6T code (for Byte 1) on that pair also had a weight of +1, the inversion rule applies.

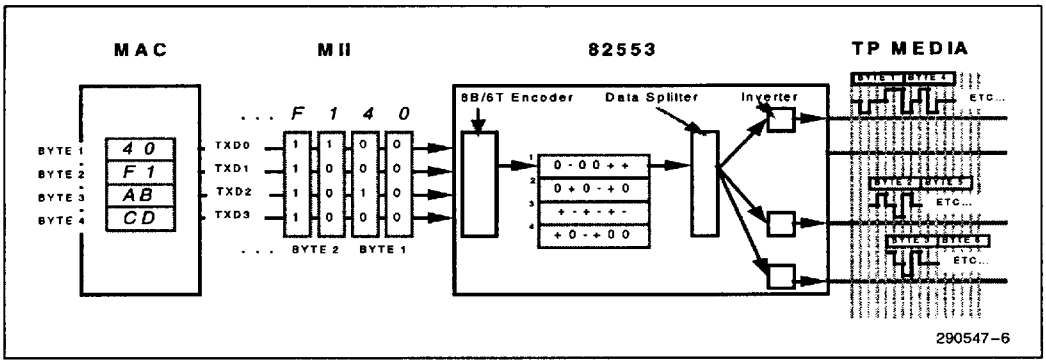

Figure 6. Example T4 8B/6T Frame

4.2.3 82553 TRANSMIT FRAMING

A T4 frame must be transmitted on pairs 1, 3 and 4 according to a certain framing protocol. As in 10Base-T, 100Base-T4 specifies a preamble, a start-frame delimiter, an Ethernet header and data, a 4 byte CRC, and an EOS delimiter. T4 also specifies a DC rebalance pattern that is necessary because of the special T4 EOS delimiter. Figure 7 shows a typical T4 frame.

During 100 Mbps transmission, when TXEN is active, the 82553 simply accepts the data on the MII TXD0–3 lines, encodes it, and sends it out on the wire. The 82553 is responsible for encoding the data into 6T representation, applying the inversion rule, and framing the data on the three transmit pairs, staggering each pair by 2 TXCs (80 ns). The 82553 is also responsible for determining what values to transmit for the EOS delimiters (E1, E2 and E3). The EOS delimiters are defined as the end-of-sequence indicators and have a value of all "−" or all "+". E1 will always fall on the same pair as CRC2 because of the rotational nature of the three transmit pairs. The values of E1, E2 and E3 are determined as follows:

Weight of Last Non-Zero 6T Code On Any Given Pair	E1	E2	E3
+1	− − − − − −	− − − −	− −
−1	+ + + + + +	+ + + +	+ +

E1, E2 and E3 are different lengths to allow for simultaneous end-of-transmission on all three transmit pairs. The 82553 is responsible for re-balancing the DC level of each pair after transmitting E1, E2 or E3. This is accomplished by transmitting the opposite of the EOS delimiter immediately. For instance, if E2 is transmitted as "+ + + +", then the 82553 should immediately transmit "− − − −" to re-balance the line.

If there is an error in the transfer of a packet to the 82553, the MAC may assert its TXERR. The 82553 will respond by sending out the jam pattern instead of the rest of the packet.

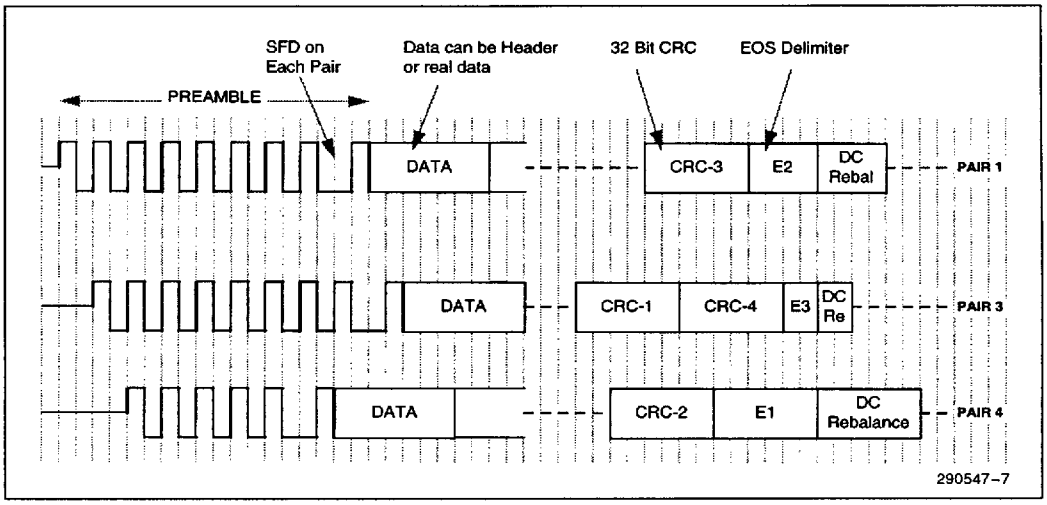

Figure 7. T4 Transmit Data Framing

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4.2.4 100BASE-T4 TRANSMIT ERROR DETECTION AND REPORTING

The 82553 provides a dedicated pin (TXERR) to allow the MAC to alert the PHY that a transmit error has occured. When TX__ER is asserted for one or more TXCs (while TXEN is asserted) the 82553 will transmit non-valid data somewhere in the frame being transmitted. Assertion of TXERR does not affect the transmission of data when the 82553 is operating at 10 Mbps, or when TXEN is de-asserted.

4.2.5 82553 TRANSMIT MULTIMODE DAC AND EXTERNAL MAGNETICS

The twisted pair line drivers (TD pairs) are implemented with a multimode DAC. The DAC begins transmitting the 6T ternary bit stream approximately three bit times after TXEN is first asserted. The 82553 DAC will either sink, float or drive the TD output pins with 70 mA of current depending on whether the ternary signal is −1, 0, or +1 respectively. The magnetics external to the 82553 convert this current source to voltage levels of ± 3.5 V_{PP} as required by the T4 specification. The same magnetics that are used for 100Base-T4 mode also work in 10Base-T mode. The following is a list of current magnetics modules which are available from several vendors:

Vendor	Model/Type	100Base-T4	10Base-T
Pulse	Tortuga 1.0	Yes	Yes
Filmag	7829022SM	Yes	Yes
Valor		Yes	Yes

NOTE:
These magnetics along with the 82553 are designed to pass FCC Class B testing.

The multimode DAC also performs signal wave shaping with an internal FIR filter in order to simplify the complexity of the external magnetics module.

4.3 82553 Receive Blocks

The receive subsection of the 82553 accepts 100Base-T4 ternary data on three RD twisted pairs (2, 3, and 4). Due to the advanced DSP design techniques employed, the 82553 will accurately receive valid data from Category 3 twisted pair wiring of length in excess of 100 meters. Figure 8 shows the 82553 receive subsection.

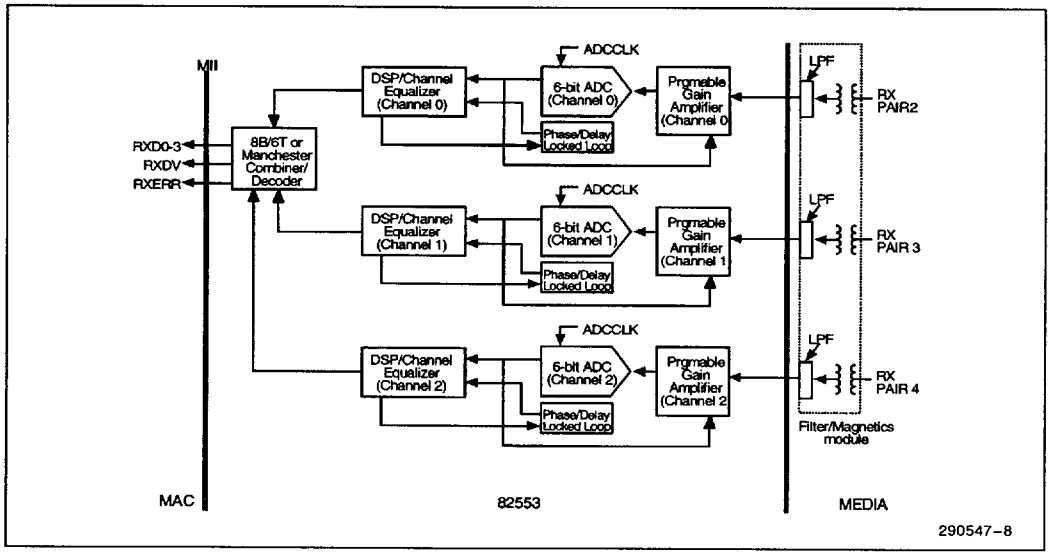

Figure 8. 82553 Receiver Block Diagram

4.3.1 PROGRAMMABLE GAIN AMPLIFIER AND CONTROL

Based on the feedback from the DSP Unit, the 82553 adjusts programmable gain to each of the three incoming analog signals in order to compensate for amplitude loss during transmission. This further enhances the recovery of data and timing from the incoming bit stream. The DSP Unit is able to detect bit patterns in the ranges specified by the T4 specification and, in some cases, even when the voltage levels vary from those ranges.

4.3.2 RECEIVE ADCs

After amplification by the Programmable Gain Amplifiers, the raw voltages on the various receive pairs are captured by the high-speed 50 MHz ADCs and converted to 6-bit digital form. This 6-bit digital version of the incoming data is sent to the Channel Equalizers where it is analyzed by the DSP Unit.

4.3.3 CHANNEL EQUALIZERS

The Channel Equalizers use advanced DSP technology to compensate for various signal degradation causes. They compensate for channel length, channel noise and removes intersymbol interference caused by the channel media. The Channel Equalizers achieve an optimum signal-to-noise ratio and employ a memory of the media characteristics. That is, the Channel Equalizers remember the appropriate gain from the last received signal.

4.3.4 100BASE-T4 CLOCK RECOVERY

The 82553 performs the necessary 8B/6T decoding and recovers timing from incoming data on all three receive pairs (pairs 2, 3, and 4). The 82553 employs three separate DLLs and phase controllers to recover RXC timing from the Receive Data independently on each receive pair. Once the receive timing is obtained, the three recovered clocks are synchronized to the RXC output to the MII and the RXDV signal is asserted to the MII, telling it that receive data is now valid.

4.3.5 100BASE-T4 RECEIVE FRAMING

A T4 frame must be received on pairs 1, 3 and 4 according to a certain framing protocol. As in 10Base-T, T4 specifies a preamble, a start-frame delimiter, an Ethernet header and data, a 4 byte CRC, and an EOS delimiter. T4 also specifies a DC rebalance pattern that is necessary because of the special T4 EOS delimiter. Figure 7 shows a typical T4 frame.

During 100 Mbps reception, the 82553 differentiates between the idle condition (no carrier) and the preamble or SFD. When the 82553 detects a valid preamble, it immediately asserts CRS and waits to see if the SFD appears on all three pairs. After the SFD is recognized, the 82553 Channel Equalizers start passing valid 6T data on to the combiner and 8B/6T Decoder. The 82553 then provides the data on the MII RXD0–3 lines synchronized to RXC, asserting RXDV. The 82553 is also responsible for determining if the 6T data was inverted. The 82553 must recognize the EOS delimiters (E1, E2 and E3) and discard them, deasserting RXDV immediately.

4.3.6 100BASE-T4 8B/6T DECODER

The 6T data recovered from the three Channel Equalizers is converted to bytes, combined into a single 6T data stream, and fed through the 8B/6T decoder where coding errors and the inversion rule are checked. The resulting bytes are combined to form a single nibble-wide Receive Data stream that is fed to the MII via the RXD0-RXD3 pins, synchronized to RXC. CRS is asynchronously asserted to the MAC as soon as valid activity is detected on receive pair 2 and will precede RXDV by several clocks.

4.3.7 100BASE-T4 RECEIVE ERROR DETECTION AND REPORTING

In 100Base-T4 mode, the 82553 can detect errors in the receive data in a number of ways. Any of the following conditions is considered an error:

- A validation of DC Balance Rule as described in the 100Base-T4 specification.
- A violation of the 100Base-T4 group table.
- Packet to Packet Skew (change on any of the three channels is greater than 40 ns).
- Pair to Pair Skew (more than 60 ns)
- Bad code received (per 100Base-T4 specification)
- EOP errors received (per 100Base-T4 specification)

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When any of the above error conditions occurs, the 82553 will immediately assert its RXERR pin to the MAC. The RXERR pin will be held active as long as a receive error condition persists on one of the receive pairs.

4.4 100Base-T4 Collision Detection

100Base-T4 Collisions are detected much the same as they are in 10Base-T: by simultaneous transmission and reception. When transmitting T4, pair 2 is idle (listening for reception). If a carrier (preamble) is sensed on pair 2 when a frame is being transmitted on the other three pairs, then a jam pattern is sent out on pair 1 and idle on pairs 3 and 4 until the end-of-carrier is received on pair 2. This mechanism is very similar to 10Base-T and is discussed in detail in the IEEE 802.3u 100Base-T4 specification.

4.5 100Base-T4 Link Integrity (Parallel Detection)

100 Mbps link integrity pulses for 100Base-T4 are defined as shown in Figure 9. Note the difference between 10Base-T and T4 link integrity pulses. The 82553 will detect whether the adapter is operating at 100 Mbps or 10 Mbps based the spacing of the link beat pulses it receives. The frequency of 100Base-T4 link pulses is greater than 10Base-T pulses. 100Base-T4 link pulses come much more quickly than 10Base-T link pulses. After reset, the 82553 will send T4 link pulses on pair 1 and listen on pair 2. If the adapter receives T4 pulses on pair 2, it will go into 100Base-T4 link pass state and be ready for transmission and reception. If 10Base-T pulses are received on pair 2, the 82553 will switch to sending 10Base-T link pulses on pair 1 and attempt to reach 10Base-T link pass. If neither link is detected, possibly due to a detached cable, the 82553 defaults to T4. This process is also called Parallel Detection and is used to select the appropriate link speed.

The 82553 has an advanced, built-in auto speed selection mechanism based upon link status. Section 9.4 describes this mechanism.

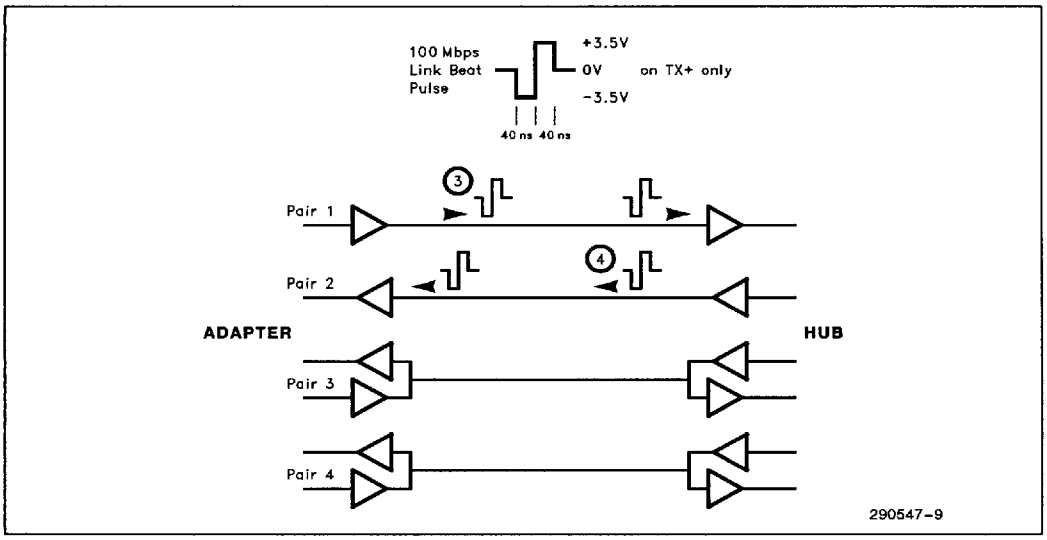

Figure 9. 82553 T4 Link Beat Protocol

4.6 Auto 10 Mbps/100 Mbps Selection

The MAC may either allow the 82553 to determine what speed to operate at, or force the 82553 into 10 Mbps or 100 Mbps mode. If AUTOSPSEL (MODE4 pin when RPT and TESTEXT = 0) is high, then the 82553 will ignore the FORCE10__100 input. If AUTOSPSEL is low, the 82553 is forced into 10 Mbps or 100 Mbps operation depending on the level of FORCE10__100 (1 = 100 Mbps mode). The 82553 can also be put into auto-speed-select mode through the MDI interface, however the AUTOSPSEL pin carries a higher priority than the using the MDI interface to enable auto-speed select.

The 82553 determines the operation speed of the media, based on the link integrity pulses it receives (Parallel Detection). If no link integrity pulses are detected, the 82553 will default to 10 Mbps operation. In Repeater mode (RPT = 1), the 82553 is always in 100 Mbps mode. If the 82553 detects a speed change, it will dynamically change its TXC and RXC frequencies to the appropriate value. This change takes a maximum of 5 ms.

5.0 ADAPTER MODE 10BASE-T OPERATION

5.1 10Base-T Clock Generation

A 50 MHz oscillator or 20 MHz oscillator/crystal is used to drive the external 82553 X1/X2 pin. In 10 Mbps mode, the 82553 derives the 20 MHz ± 0.01% serial clock (for use in Manchester decoding) from this crystal input. The 82553 should, in turn, provide the 10 MHz TXC and RXC to the MAC. The accuracy of the external crystal oscillator depends on the PC board characteristics.

5.2 10Base-T Transmit Blocks

5.2.1 10BASE-T MANCHESTER ENCODER

The 10 MHz RXC is used to Manchester-Encode the serial data arriving on the TXD0 input. 10Base-T Manchester encoding is NRZ. Please refer to the *Intel 82503 Data Sheet* for a complete description of Manchester encoding.

5.2.2 10BASE-T TPE CABLE DRIVER

In 10 Mbps mode, the 82553 should begin transmitting the serial Manchester bit stream within 3-bit times (300 ns) after TXEN is asserted by the MAC. In 10 Mbps mode, the current line drivers use a predistortion algorithm to improve jitter tolerance. The line drivers reduce their drive level during the second half of "wide" (100 ns) Manchester pulses and maintain a full drive level during all "narrow" (50 ns) pulses and the first half of the wide pulses. This reduces line overcharging during wide pulses, a major source of jitter. The following figure shows the serial data, its Manchester representation, and the signal at the RJ45 connector after predistortion.

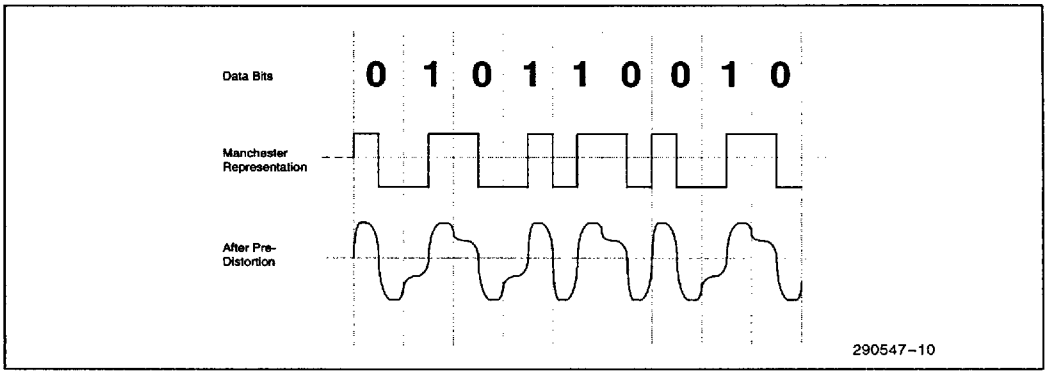

Figure 10. 82553 Pre-Distortion (10 Mbps Mode Only)

5.3 10Base-T Receive Blocks

5.3.1 10BASE-T MANCHESTER DECODER

The 82553 will perform Manchester decoding and timing recovery when in the 10 Mbps mode. The Manchester-encoded data stream is decoded from twisted-pair 2 to separate Receive Clock (RXC) and the Receive Data (RXD0) from the differential signal. This data will be transferred to the controller on the RD0 line at 10 MHz. The 10 Mbps clock and data recovery is insensitive to variations in operation conditions much like the 82503 high resolution phase reference. For instance, jitter tolerances are at least ±3.5 ns. For more information on the 82503, refer to the *Intel 82503 Data Sheet*.

5.3.2 10BASE-T TPE RECEIVE BUFFER

In 10 Mbps mode, data is expected to be received on differential pair 2 (RD2 and RD2#). The signal received on the differential pair is assumed to have already passed through isolation transformers and EMI filters which perform the line coupling necessary to comply with the 10Base-T specification. The input differential voltage range for the TPE receiver is greater than 500 mV and less than 3.1V differential. The TPE receive buffer distinguishes valid receive data, link test pulses, and the idle condition according to the requirements of the 10Base-T standard. The following line activity is determined to be inactive and is rejected:

- Differential pulses of peak magnitude less than 300 mV.
- Continuous sinusoids with a differential amplitude less than 6.2 V_{PP} and a frequency less than 2 MHz.
- Sine waves of a single cycle duration starting with phase 0 degrees or 180 degrees that have a differential amplitude less than 6.2 V_{PP} and a frequency of at least 2 MHz and not more than 16 MHz. These single cycle sine waves are discarded only if they are preceded by 4-bit times (400 ns) of silence.

All other activity is determined to be either receive data, link test pulses, or idle condition (silence, differential signals less than 300 mV). If activity is detected, then the CRS signal should be asserted to the MAC.

5.3.3 10BASE-T ERROR DETECTION AND REPORTING

In 10 Mbps mode, the 82553 can detect errors in the receive data. The following condition is considered an error:

- The receive pair's voltage level drops to the idle state during reception before the End-of-Frame delimiter is seen.

5.4 10Base-T Collision Detection

Collision detection in 10 Mbps mode is indicated by simultaneous transmission on pair 1 and reception on pair 2. (Note that in 10 Mbps Full Duplex mode, collisions are not detected—see Section 5.7.) If the 82553 detects this condition, then the CDT signal is asserted. The CDT signal should be held active until receive data is no longer sensed on pair 2. Upon detecting a collision, the MAC will replace transmit data with the jam pattern. The 82553 should forward this jam pattern as if it were regular transmit data. The MAC will continue to send the jam pattern for a specified amount of time.

5.5 10Base-T Link Integrity

The link integrity pulses for 10 Mbps are slightly different than 100 Mbps so the 82553 can autosense whether the network is 100Base-T4 or 10Base-T. Figure 11 shows the 10 Mbps Link Integrity pulse. The Link Beat pulse also determines if the receive pair polarity is reversed.

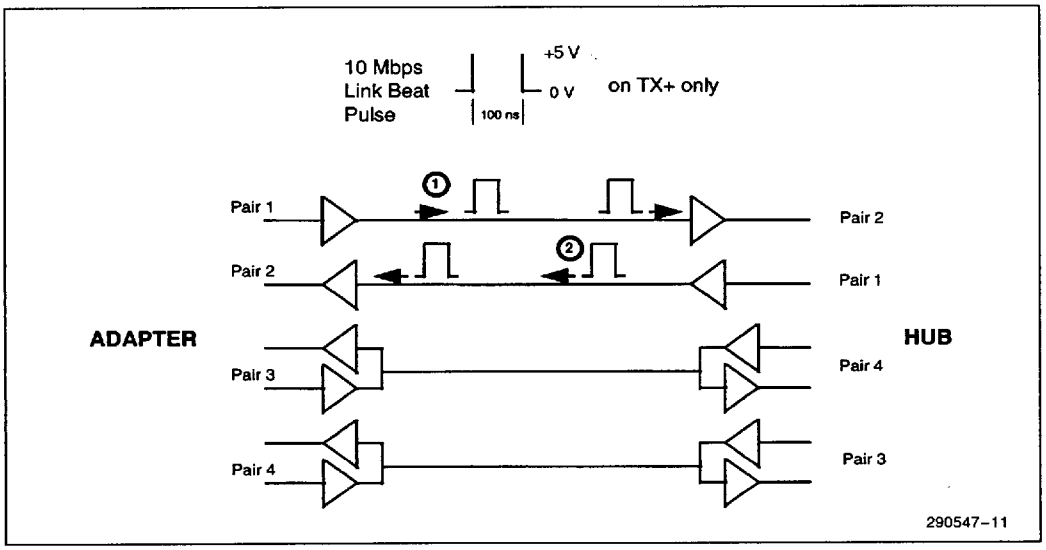

Figure 11. 82553 10Base-T Link Beat Protocol

5.6 10Base-T Jabber

The 82553 contains a jabber control function which, when enabled, will inhibit transmission after a specified time window. In 10 Mbps mode, the jabber timer is set to a value between 26.2 ms and 39.0 ms. If the 82553 detects continuous transmission for longer than this time, it will prevent further transmissions from going out in the wire until it detects that the MAC RTS signal has been inactive for at least 314 ms. See the IEEE 802.3 10Base-T specification for more details.

5.7 10Base-T Full-Duplex

The 82553 supports 10 Mbps full-duplex by disabling the CRS and CDT functions. This allows the 82553 to transmit and receive simultaneously, achieving up to 20 Mbit/s of network bandwidth. Otherwise, all functions and pins of the 82553 perform identically to normal 10Base-T mode.

The 82553 can be set to Manual Full Duplex operation by setting the appropriate MDI Register using the MDI interface (Register 0, bit 8). See Section 7.1.1 for details. The 82553 can also be set to automatic Full Duplex (through Auto-Negotiation). See Section 8 for details.

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6.0 100BASE-T4 REPEATER MODE

The 82553 can be programmed to operate in one of two different repeater modes: Line Level (Class II) or MII (Class I). The following table lists the various settings for enabling the two modes.

Table 2. MII/Line Level Repeater Mode Settings

TXD4	Repeater Mode (RPT)	Internal Mode Indication
0	0	Adapter (Normal) Mode (DTE)
1	0	MII (Class I) Mode
X	1	Line-Level (Class II) Mode

6.1 Line Level Repeater Mode

The 82553 contains many internal features that allow it to perform as a 100 Mbps line-level repeater physical layer component. In Line Level Repeater mode, the 82553 provides incoming 6T data (ternary symbols) in its original form that other 82553s can use without adding extra delays. Several 82553s to be wired ("ored") together to form the core of a line level repeater. This mode is enabled by setting the RPT pin to a "1" (TESTEXT = 0). When this mode is enabled, the 82553 will route the 2-bit output of the three receive aligners to RXD0–5. In this fashion, other 82553s can accept this 2-bit representation of 6T codes on their TXD0–5 pins. For instance, at any given instance, a receive pair can have a value of −1, 0 or +1. This will map into a 10, 00, or 01 respectively and be provided on either RXD4–5 (pair 4) RXD2–3 (pair 3) or RXD0–1 (pair 2). The 82553 8B6T decoder will be bypassed when in Repeater Mode.

This Repeater Mode feature enables low-cost 100Base-T4 line level repeaters to be manufactured with multiple 82553 components.

Figure 12 shows the 82553 in this configuration.

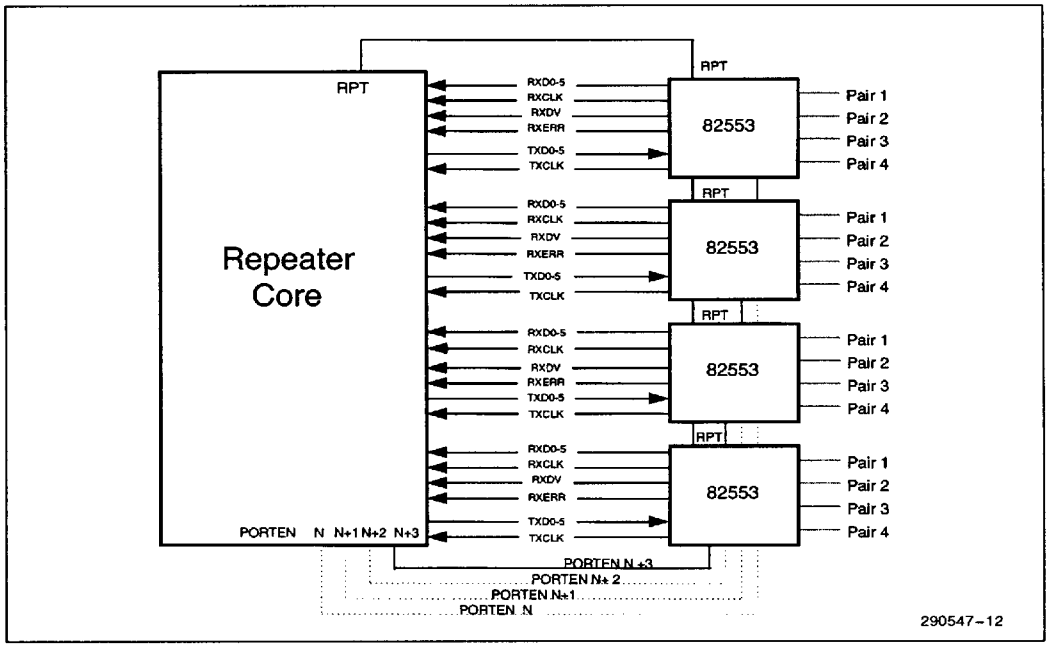

Figure 12. Repeater Core Sample Diagram

6.2 MII Repeater Mode

MII Repeater Mode allows the several 82553 components to form the core of an MII Repeater. The 6T data is sent from the 82553 through the MII interface and to the receiving 82553, and vice versa. MII Repeater Mode differs from Line Level Repeater Mode in that MII Repeater Mode uses the 8B6T decoder to pass receive data from the 82553 through the MII interface, to the repeater core.

While in MII Repeater Mode, the 82553 does not return CRS during transmission. Figure 13 shows a sample MII repeater mode diagram.

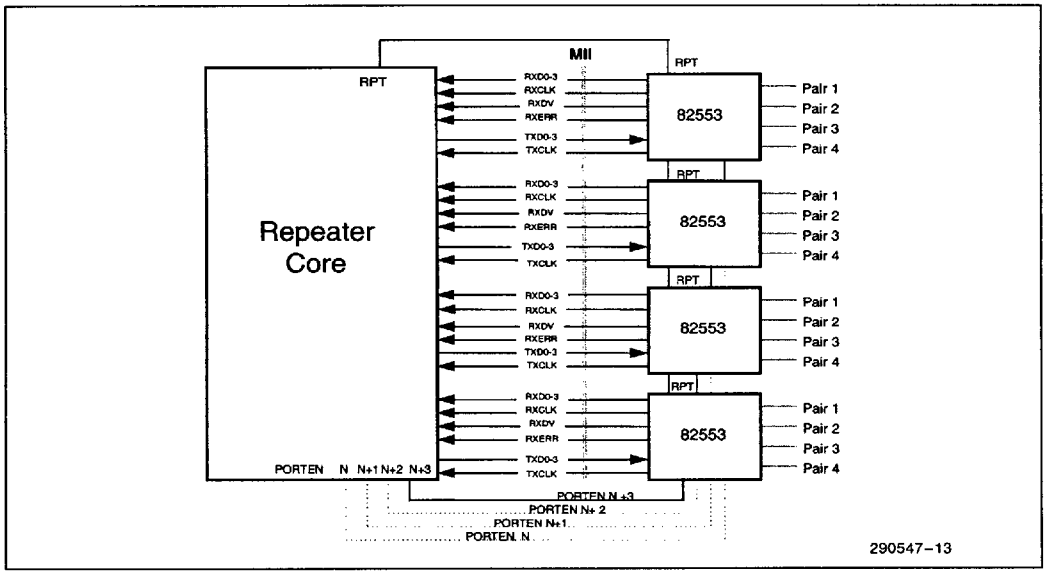

Figure 13. MII Repeater Sample Diagram

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7.0 MANAGEMENT DATA INTERFACE

The 82553 provides status and accepts management information via the Management Data Interface (MDI). This is accomplished via read and write operations to various registers according to the IEEE 802.3μ MII specification. A read or write of a particular register is called a management frame, which is sent serially over the MDIO pin synchronous to MDC. Read and Write cycles are from the perspective of the controller. Therefore, the controller would always drive the Start, Opcode, PHY Address and Register Address on to the MDIO pin. For a write, the controller would also drive the transition bits and the data. For a read, the 82553 drives the transition bits and data onto the MDIO pin. The controller should drive address and data on the rising edge of MDC and the 82553 latches that data on the rising edge of MDC. In a non-repeater application, the 82553 uses a default PHY Address of 00001. In a repeater application, the 82553 can be configured for 32 different addresses (by pin selection). The management frame structure is as follows:

	Start	Op Code	PHY Addr	Reg Addr	Transition	Data
READ:	<01>	<10>	<AAAAA>	<RRRRR>	<Z0>	16 Bits
WRITE:	<01>	<01>	<AAAAA>	<RRRRR>	<10>	16 Bits

Preamble: At the beginning of each transaction, the MAC will send a sequence of 32 continguous logic one bits on the MDIO pin with the corresponding cycles on the MDC pin for synchronization by the 82553.

ST: A start of frame pattern of "01".

OP Code: An Operation Code that identifies an MDI Read or MDI Write.

PHY Addr: A 5-bit address of the 82553. Provides support for up to 32 unique PHY addresses (31 other PHY addresses).

Reg Addr: A 5-bit address of the specific register within the 82553.

TA: A two-bit turnaround time during which no device actively drives the MDIO signal on a Read cycle. During a Read transaction the 82553 will not drive MDIO in the first bit time and will drive a 0 in the second bit time. During a Write transaction the MAC will drive a "10" pattern to fill this time.

DATA: 16 bits of data driven by the 82553 on Read transactions or by the MAC for Write transactions. This data is either control or status parameters passed between the MAC and the 82553.

IDLE: The IDLE condition on MDIO is a high impedance state. The 82553 should pull-up the MDIO line to a logic one.

This structure allows a controller, or other management hardware, to query the 82553 for the status of the link or configure the 82553 to one of many modes.

7.1 MDI Register Set

Table 3 shows the MDI register set.

Table 3. The 82553 MDI Register Set

Register Address	Register Name and Function
00000	Control Register (MDI Standard Register)
00001	Status Register (MDI Standard Register)
00010	PHY Identification Register (Word 1)
00011	PHY Identification Register (Word 2)
00100	Auto-Negotiation Advertisement
00101	Auto-Negotiation Link Partner Ability
00110	Auto-Negotiation Expansion
00111–01111	Not Used
10000	Extended Register 0 (82553-Specific Modes)
10001	Reserved
10010	Reserved
10011	Reserved
10100	Extended Register 1 (82553-Specific Error Indications)
10101	Extended Register 2
10101–1111	Not Used

The individual registers are defined in Sections 7.1.1 through 7.1.8.

7.1.1 CONTROL REGISTER

The Control Register (Address 00000) consists of a single 16-bit register.

Table 4. Control Register

Bit	Name	R/W	Description	Default
15	Reset	R/W (SC)	1 = PHY Reset 0 = Normal Operation	0
14	Loopback	R/W	1 = Loopback Mode 0 = Normal Operation	0
13	10/100	R/W	0 = 10 Mbit/s 1 = 100 Mbit/s	1
12	Auto Negotiation Enable	R/W	1 = Enable Auto Negotiation 0 = Disable Auto Negotiation	1
11	Power Down	R/W	1 = Power Down 0 = Normal Operation	0
10	Isolate	R/W	1 = Electrically Isolate PHY from MII 0 = Normal Operation	0
9	Restart Auto Configuration	R/W	1 = Restart the Auto Negotiation	0
8	Full/Half	R/W	1 = Full Duplex 0 = Half Duplex	0
7	Collision Test Enable	R/W	1 = Enable the Collision CDT Test during Loopback	0
0-6	Reserved	R/W	Written as 0, Don't Care on Read	0

NOTE:
The 82553 can also be placed in Isolate mode by changing the PHY address to 00000.

7.1.1.1 Control Register Management Functions

Reset: The reset function is used to reset the 82553. All MII status and control registers are set to default states. Subsequent writes to the control register should not be completed before 500 ms after the RESET bit is set.

Loopback: The loopback function is used to isolate the 82553 from the link. Data from the MII transmit path is sent to the MII receive path upon assertion of TX_EN. The delay from TX_EN to RX_DV is not more than 512 bit times.

Speed Selection: The speed function is used to manually configure the 82553. Auto-Negotiation Enable bit must be set to 0 (disabled) in order to use the Sped Selection bit. Note this bit is a read or write (bit can be set to a one or zero by the result of Auto-Negotiation).

Auto-Negotiation Enable: This function activates the Auto-Negotiate process which will determine link configuration. If the 82553 cannot perform Auto-Negotiation, this bit will be set to a zero. Any attempt to write to this bit will be ignored.

Power Down: This bit places the 82553 in low power state. The 82553 will still respond to management transactions.

Isolate: The Isolate function is used to electrically isolate the 82553 data paths from the MII. When the PHY is isolated from the MII it will not respond to the TXD0-3, TX_EN and TX_E inputs, and will present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RXD0-3, COL, and CRS outputs. However, when in Isolate Mode, the 82553 will respond to Management transactions.

Restart Auto-Negotiation (Renegotiate): Used to restart the Auto-Negotiation process. Any attempt to write to this bit upon an unsuccessful Auto_Negotiate process is ignored.

Duplex Mode: Used to manually configure the 82553 to full-duplex operation. If Auto-Negotiation is enabled, this bit can be read or written but has no effect on the link configuration. If loopback is enabled, this bit can be read or written but has no effect on the link configuration.

Collision Test: This bit, when enabled, will cause the 82553 to assert CDT within 512-bit times after TX_EN is assserted. When TX_EN is subsquently de-asserted, the 82553 will deassert CDT within four bit times.

7.1.2 STATUS REGISTER

The Status Register (Address 00001) consists of a single 16-bit register.

7.1.2.1 Status Register Management Functions

Bits 6–15: refer to Table 7.

Auto-Negotiation Complete: This bit indicates that Auto-Negotiation has completed. If set to a one, MII registers 4, 5, 6, and 7 are valid. If this bit is set to a zero, the Auto-Negotiation process has not yet been completed and the contents of registers 4, 5, 6, and 7 are void.

Table 5. Status Register

Bit	Name	R/W	Description	Default
15	T4 Capable	RO	1 = T4 Capable 0 = not T4 Capable	1
14	TX Full Duplex Capable	RO	1 = TX Full Duplex Capable 0 = not TX Full Duplex Capable	0
13	TX Half Duplex Capable	RO	1 = TX Half Duplex Capable 0 = not TX Half Duplex Capable	0
12	10Base-T full Duplex Capable	RO	1 = 10BaseT full Duplex Capable 0 = not 10BaseT full Duplex Capable	1
11	10Base-T Half Duplex Capable	RO	1 = 10BaseT Half Duplex Capable 0 = not 10BaseT Half Duplex Capable	1
6–10	Reserved	RO	Written as 0, Don't Care on Read	0
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation Complete 0 = not Complete	0
4	Remote Fault Detect	RO	1 = Remote Fault Detect 0 = not Detect	0
3	Auto Negotiate Capable	RO	1 = Auto Negotiate Capable 0 = Auto Negotiate not Capable	0
2	Link Status (LINKFLT)	RO	1 = Link is up 0 = Link is down	Sticky Bit
1	Jabber Detect (JABFLT)	RO	1 = Jabber Condition Detected 0 = no Jabber Condition Detected	Sticky Bit
0	Extended Cap	RO	1 = Extended Register Capabilities 0 = Basic Register Set Capabilities only	1

Remote Fault: This bit, when set to a one, indicates that the 82553 has detected a remote fault condition. An MII reset only will clear this bit.

Auto-Negotiate Ability: This bit is used to indicate whether or not the 82553 can perform Auto-Negotiation.

Link Status: This bit, when set to a one, indicates that the 82553 has determined link is valid (Link-Pass state). When set to a one, indicates that the 82553 had determined link is not valid (Link-Fail state).

Jabber Detect: This bit, when set to a one, indicates a jabber condition has been detected by the 82553. A jabber condition is one in which transmission continues beyond the limits specified. The 82553 will inhibit further transmission and assert CDT. The limits for jabber transmission are 20 ms to 150 ms, and the inhibit period will extend until the 82553 detects sufficient idle time (between 250 ms and 750 ns) on the TX_EN signal. Jabber Detect is only valid when the 82553 is configured for 10 Mbit mode.

Extended Capability: This bit, when set to a one, indicates that the 82553 provides an additional set of functions which may be accessed through the extended register set. When set to a zero, indicates that the 82553 provides only the basic register set.

7.1.3 82553 IDENTIFICATION REGISTER

The 82553 Identification Register consists of a register of 32 bits at MDI offset 00010 and 00011. The 82553 Identification Register values differ in the B step and C step parts.

In the B step part, the identification register is:
ID Low = 03E0 h and 0000 h ID High.

In the C step part, the identification register is:
ID Low = 02A8 h and 0353 h ID High.

7.1.4 82553 AUTO-NEGOTIATION ADVERTISEMENT REGISTER

This register contains the Advertisement Ability of the 82553. This register is used by software to determine the highest common denominator technology once Auto-Negotiation has completed. Any change of this register prior to Auto-Negotiation must be followed by setting the Renegotiate bit in the Command register.

Table 6. Auto-Negotiation Advertisement Register (Register 4)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	Not Supported (Reserved).	0
14	Reserved	RO	This bit position in the transmitted code word is used to indicate Acknowledge. It is set only by the Auto-Negotiation logic, after receiving three consecutive and matching code words from the link partner.	0
13	Remote Fault	R/W	Indicates Remote Fault in local station. May be set by management to indicate the remote fault condition of the partner.	0
5–12	Technology Ability Field(1)	R/W	Contains information indicating supported technologies specific to the selector field value (see Table 9).	00010011
0–4	Selector Field	R/W	Used to identify the protocol supported. IEEE 802.3 is indicated by Selector value 00001.	00001

NOTE:
1. For normal operation, the software driver (management agent) does not need to change this register value. When not advertising a certain ability, the respective bit in the Technology Ability field must be cleared. A bit must NOT be set within this field that is not supported by the device. Otherwise, the Auto-Negotiation protocol will be violated.

7.1.5 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER

This register holds the link code word captured from the Link Partner's PHY (device at the other end of the link segment). Its value is valid only when the Auto-Negotiation Complete bit is set in the Status register.

Table 7. Auto-Negotiation Link Partner Ability Register (Register 5)

Bit	Name	R/W	Description	Default
15	Next Page	RO	Not Supported (Reserved).	0
14	Acknowledge	RO	Indicates that a device has successfully received its Link Partner's Link Code Word.	0
13	Remote Fault	RO	Remote Fault bit set in received code word.	0
5–12	Technology Ability Field	RO	Technology Ability received from link partner.	00000000
0–4	Selector Field	RO	Selector field from link partner.	00000

7.1.6 AUTO-NEGOTIATION EXPANSION REGISTER

This register holds supplemental information used by the Auto-Negotiation process.

Table 8. Auto-Negotiation Expansion Register (Register 6)

Bit	Name	R/W	Description	Default
5–15	Reserved	RO	Reserved	0
4	Parallel Detection Fault	RO	1 = More than one of the 10Base-T, 100Base-TX, or 100Base-T4 PMAs detects a valid link 0 = Not more than one of the 10Base-T, 100Base-TX, or 100Base-T4 PMAs detects a valid link	0
3	Link Partner Next Page Able	RO	1 = Link Partner is Next Page Able 0 = Link Partner is not Next Page Able	0
2	Next Page Able	RO	1 = Local Device is Next Page Able 0 = Local Device is not Next Page Able	0
1	Page Received	RO	1 = 3 Identical and Consecutive Link Code Words have been Received 0 = 3 Identical and Consecutive Link Code Words have not been Received	0
0	Link Partner Auto-Negotation Able	RO	1 = Link Partner is Auto-Negotiation Able 0 = Link Partner is not Auto-Negotiation Able	0

7.1.7 EXTENDED REGISTER 0

The 82553 implements additional functions in the Extended Registers of its MDI Register set. The Extended Registers are implementation-specific registers that are not available in non-Intel PHY components. Extended Register 0 exists at MDI Address 10000. It provides configuration and status information of additional 82553 features and is defined below.

Table 9. Extended Register 0

Bit	Name	R/W	Description	Default
15	JABDIS	R/W	1 = Jabber Function Disabled in PHY 0 = Jabber Function Enabled in PHY	0
14	LINKDIS	R/W	1 = Link Integrity Test Disabled in PHY 0 = Link Integrity Test is Enabled in PHY 0	0
9–13	TEST(0–4)	R/W		00000
8	FORCE100	RO	1 = 100 Mbps Mode of Chip Operation Speed 0 = 10 Mbps Mode of Chip Operation Speed	0
5–7	82553 Part Revision	RO	000 = B-Step 011 = C-Step	—
3–4	HSQ (4) LSQ (3)	R/W		00
2	Wake Up*	R/W	1 = Wake Up DACs 0 = Shut Down DAC	0
1	Speed Indication	RO	1 = 100 Mbit/s Mode 0 = 10 Mbit/s Mode	0
0	Full Duplex Indication	RO	1 = Full Duplex Mode 0 = Half Full Duplex Mode	0

NOTE:
*This bit is used to disable the 82553 power-saving feature. The 82553 will automatically power-down part of the DACs when not transmitting unless this bit is set to a 1.

7.1.8 EXTENDED REGISTER 1

The 82553 implements additional functions in the Extended Registers of its MDI Register set. The Extended Registers are implementation-specific registers that are not available in non-Intel PHY components. Extended Register 1, also known as the Error Indication Register, exists at MDI Address 10100 and is defined below.

Table 10. Error Indication Register (Extended Register 1)

Bit	Name	R/W	Description	Default
15	PAIR_SKEW_ERR	RO	1 = Pair Skew Error 0 = No Pair Skew Error	Sticky Bit
14	DC_BALANCE_ERR	RO	1 = DC Balance Error 0 = Not DC Balance Error	Sticky Bit
13	INVALID_CODE_ERR	RO	1 = Invalid Code Error 0 = Not Invalid Code Error	Sticky Bit
12	BAD_CODE_ERR	RO	1 = Bad Code Error 0 = Not Bad Code Error	Sticky Bit
11	EOP_ERR	RO	1 = EOP Error 0 = Not EOP Error	Sticky Bit
10	MANCHESTER_CODE_ERR	RO	1 = Manchester Code Error 0 = No Error	Sticky Bit
9	CH2_EOF_ERR	RO	1 = Channel 2 EOF Detection Error 0 = No Error	Sticky Bit
8	DTE_MODE_SEL	RO	1 = External DTE mode	DTE Mode from External Select
7	LINE_RPTR_MODE_SEL	RO	1 = MII Repeater Mode	Line Repeater Mode Select
6	EXT_TEST_MODE_SEL	RO	1 = Line Level Repeater Mode	External Test Mode Select
5	MII_RPTR_MODE_SEL	RO	1 = MII Repeater Mode	MII Repeater Mode Select
4	CH2_POLARITY_ERR	RO	1 = Channel 2 Polarity Error	0
3	CH3_POLARITY_ERR	RO	1 = Channel 3 Polarity Error	0
2	CH4_POLARITY_ERR	RO	1 = Channel 4 Polarity Error	0
1	CH2_SFD_DETECT_ERR	RO	1 = Channel 2 SFD Not Found	Sticky Bit
0	Reserved			0

NOTE:
R/W = Read/Write, RO = Read only, SC = Self Clear

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7.1.9 EXTENDED REGISTER 2 (C STEP ONLY)

The 82553 implements additional functions in the Extended Registers of its MDI Register set. The Extended Registers are implementation-specific registers that are not available in non-Intel PHY components. Extended Register 2, exists at MDI Address 10101 and is defined below.

Table 11. Extended Register 2

Bit	Name	R/W	Description	Default
15	Auto_Negotiation_Select	RO		0
14	CH3_SFD_ERROR	RO		0
13	CH4_SFD_ERROR	RO		0
12	Reserved	RO		0

7.2 Support for Multiple PHY Addresses

7.2.1 B STEP PART ONLY

When in Adapter and MII mode, the 82553 can be configured for two addresses: 00000 and 00001. When in Line Level Repeater mode, the 82553 for all 32 addresses from 00000 to 11111.

7.2.2 C STEP PART ONLY

When in Adapter mode, the 82553 can be configured for two addresses: 00000 and 00001. When in Line Level Repeater mode or MII mode, the 82553 for all 32 addresses from 00000 to 11111.

7.2.3 INFORMATION FOR ALL PARTS

In an application where only one PHY is present (RPT = 0), the 82553 uses a default PHY Address of 00001. This can optionally be changed to 00000 by deasserting the MODE0 pin during RESET. In Line level repeater mode (RPT = 1), the 82553 will assume its PHY Address from the state of the following pins.

PHY Address Bit	Value Read in at RESET Calculated from:
4	MODE4
3	MODE3
2	MODE2
1	MODE1
0	MODE0

8.0 AUTO-NEGOTIATION FUNCTIONALITY

8.1 Overview

The 82553 (C-step) supports Auto-Negotiation. Auto-Negotiation is a scheme of auto-configuration designed to manage interoperability in multi-functional LAN environments. It allows two stations with "N" different modes of communication to establish a common mode of operation. At power-up, Auto-Negotiation automatically establishes a link that takes advantage of an Auto-Negotiation capable device. An Auto-Negotiation-capable hub can detect and automatically configure its ports to take maximum advantage of common modes of operation without user intervention or prior knowledge by either station. The possible common modes of operation are: 100Base-T4, 100Base-TX, 100Base-TX Full Duplex, 10Base-T, 10Base-T Full Duplex.

8.2 Description

Auto-Negotiation selects the fast operating mode (Highest Common Denominator) available to hardware at both ends of the cable. A PHY's capability is encoded by bursts of link pulses called Fast Link Pulses (FLPs). Connection is established by FLP exchange and handshake during initialization time. Once the link is established by this handshake, the native link pulse scheme resumes (i.e., 10Base-T or 100Base-T4 link pulses, etc.). A reset or management renegotiate command (through the MDI interface) will restart the process. To enable Auto-Negotiation, bit 12 of the MII Control Register must be set. If the 82553 cannot perform Auto-Negotiation, it will set this bit to a 0 and determine the speed using Parallel Detection (see Section 4.5).

The 82553 supports three technologies: 100Base-T4, 10Base-T, and 10Base-T Full Duplex. Since only one technology can be used at a time (after every re-negotiate command), a priorization scheme must be used to ensure that the highest common denominator ability is chosen. Table 12 lists the technology ability field bit assignments. Each bit in this table is set according to what the PHY is capable of supporting. In the case of the 82553, bits 0, 1, and 4 are set. Table 13 lists the priority of each of the technologies.

Table 12. FLP Technology Ability Field Bit Assignments

Bit Setting	Technology
0	10Base-T
1	10Base-T Full Duplex
2	100Base-TX
3	100Base-TX Full Duplex
4	100Base-T4
5	Reserved
6	Reserved
7	Reserved

Table 13. Technology Priority List

Priority	Technology
1	10Base-TX Full Duplex
2	10Base-T4
3	100Base-TX
4	100Base-T Full Duplex
5	100Base-T

To detect the correct technology, the two 2 register fields should be ANDed together to obtain the Highest Common Denominator. This value should then be used to map into a Priority Resolution Table used by the MAC driver to use the appropriate technology.

The following is a summary outline of the Auto-Negotiation process:

- Receive 3 consecutive, matching code words.
- Set Acknowledge bit in transmit code word.
- Receive 3 consecutive, matching code words with Acknowledge bit set.
- Transmit 6-8 more code words with Acknowledge bit set.
- Use the Priority table to determine operating mode
- FLP received from link partner is recorded in MII register.

8.3 Parallel Detect (B1-Stepping Only)

The 82553 automatically determines the speed of the link either by using Parallel Detect. Upon RESET, MII forced speed change, link status fail, or Negotiate/Renegotiate command, it will insert a long delay during which no link pulses are transmitted. This period, known as Force_Fail, insures that the 82553 link partner has gone into a Link Fail state before Parallel Detection begins. Thus, both sides (82553 and 82553 link partner) will perform Parallel Detection with no data packets being transmitted. Connection is then established by Parallel Detection. The 82553 will look for link integrity pulses. Figure 14 illustrates this process. Note that the B1 stepping does not support Auto-Negotiation as shown in the diagram.

8.4 Parallel Detect and Auto-Negotiation (C-Stepping Only)

The 82553 automatically determines the speed of the link either by using Parallel Detect or Auto-Negotiation. Upon RESET, MII forced speed change, link status fail, or Negotiate/Renegotiate command, it will insert a long delay during which no link pulses are transmitted. This period, known as Force_Fail, insures that the 82553 link partner has gone into a Link Fail state before Negotiation or Parallel Detection begins. Thus, both sides (82553 and 82553 link partner) will perform Auto-Negotiation or Parallel Detection with no data packets being transmitted. Connection is then established either by FLP exchange or Parallel Detection. The 82553 will look for both FLPs and link integrity pulses. Figure 14 illustrates this process.

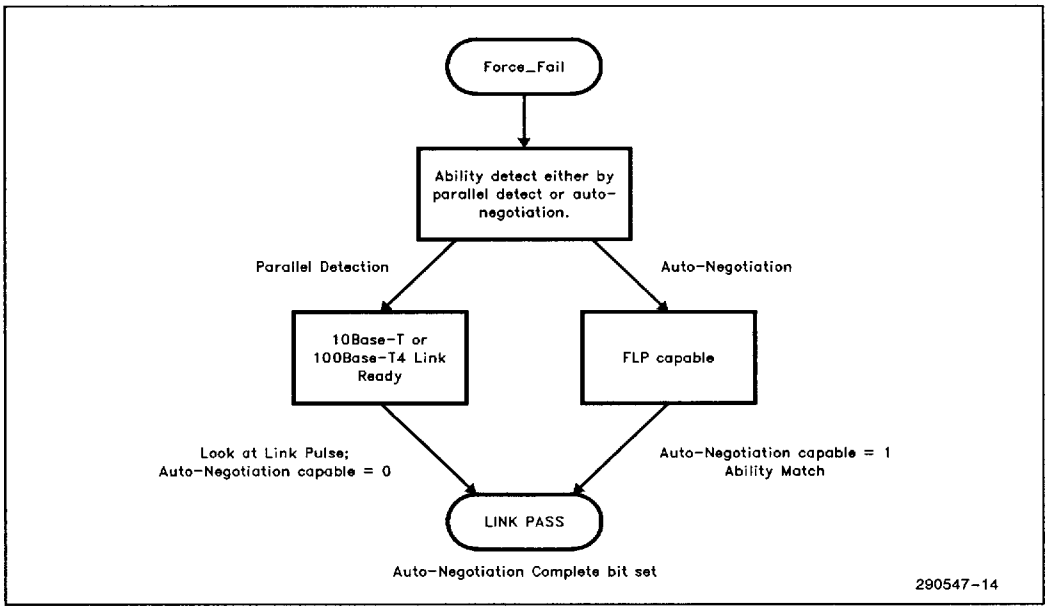

Figure 14. Auto-Negotiation and Parallel Detect

9.0 LED DESCRIPTIONS

9.1 B1-Stepping Descriptions Only

The 82553 supports four LED pins to indicate link activity, speed and full duplex mode. Each pin is capable of directly driving an LED. The LEDs are defined as follows:

ACTLED#	**ACTIVITY LED.** This LED indicates either transmit or receive activity. When there is activity, ACTLED is on (low). When there is no activity, ACTLED is off (high). When configured to MII or Line-Level Repeater mode, indicates receive activity only.
SPDLED#	**SPEED LED.** In MII Repeater or Adapter mode, this LED indicates the link speed. In 100 Mbps mode, the SPDLED is on (low). In 10 Mbps mode, this LED is off (high).
LILEDA#	**LINK INTEGRITY LED.** In MII Repeater or adapter mode, this LED indicates link beat integrity (valid link for either 10Base-T or 100Base-T4). When there is no link integrity, LILEDA# is off (high). When there is a valid link, this LED is on (low).
LILEDB#	**LINK INTEGRITY LED.** In Line-Level Repeater mode and 10Base-T mode, this LED indicates link beat integrity. When there is no link integrity, LILEDB is off (high). When there is a valid link, this LED is on (low). In 100 Mbps Adapter or MII Repeater mode, LILEDB# blinks on and off during a valid link. LILEDB# is off when there is no link.

9.2 C-Stepping Descriptions Only

The 82553 supports four LED pins to indicate link activity, speed and full duplex mode. Each pin is capable of directly driving an LED. The LEDs are defined as follows:

ACTLED#	**ACTIVITY LED.** This LED indicates either transmit or receive activity. When there is activity, ACTLED is on (low). When there is no activity, ACTLED is off (high). When configured to either Repeater mode, indicates receive activity only.
SPDLED#	**SPEED LED.** This LED indicates the link speed. In 100 Mbps mode, the SPDLED is on (low). In 10 Mbps mode, this LED is off (high). In line level repeater mode, this pin is used as RXD5 instead of an LED pin.
FDXLED#	**FULL DUPLEX LED.** In Adapter mode (and TXD5 = low) this LED indicates the duplex capability of the 82553. In Half-Duplex, this LED is off (high). In Full-Duplex, this LED is on (low). In adapter mode with TXD5 = high or in MII mode, this pin functions the same as LILEDB# (pin 72) in the B Step part. In Line Level Repeater mode, this LED is on (low) when there is a valid link. When there is no valid link, FDXLED# is off (high).
LILED#	**LINK INTEGRITY LED.** This LED indicates link beat integrity (valid link for either 10Base-T or 100Base-T4). When there is no link integrity, LILED is off (high). When there is a valid link, this LED is on (low). In the Line-Level Repeater Mode, this pin becomes RXD4 (Receive Data line) and is not used as an LED pin.

10.0 RESET AND TEST MODES

10.1 Reset

When the 82553 RESET signal is asserted (active high), all internal circuits are reset. The default state for the 82553 will be 100 Mbps Adapter mode. TXC should run continuously even though Reset is active. The Reset pulse is expected to be a minimum of 600 ns. The 82553 has an internal reset filter which will allow it to directly accept resets from PCI, EISA, VL, or ISA bus resets. In Intel implementations, the 82557 will provide the Reset pulse. The 82553 may also be reset via the Reset bit in the MDI Register set.

NOTE:
In the event that a RESET is issued to the 82553, sufficient delay must be allowed to ensure the 82553 will complete the Auto-Negotiation or Parallel Detection process. (A RESET is NOT required during initialization time.)

10.2 Digital Loopback Mode

The 82553 employs a Digital Loopback function for testing purposes. When Digital Loopback is enabled, the 82553 routes the internal 12-bit representation of the 6T (or Manchester) transmit code back to the receive 8B/6T (or Manchester) decoder. In both 10 Mbps and 100 Mbps operation, Loopback mode is enabled with the LPBK pin (MODE1 when RPT and TESTEXT = 0). All control signals such as RXDV and TXEN must act accordingly when in Loopback mode.

Figure 15 shows the Digital Loopback path.

10.3 Tri-State Mode

The Tri-State pin, when active (high), will tri-state all 82553 output pins. This state lasts as long as the 3STT pin is active. After assertion of the 3STT pin, the 82553 will require a reset to revert to normal functionality.

10.3.1 DRIVER CONSIDERATIONS

If Auto-Speed Select is used, about 500 ms of delay must be added to after RESET before reading the status of the auto speed selection. The Link Status (bit 2 of the MDI Status Register) should be read first to determine if a link is present. Note that the Link Status bit is a sticky bit (latched low), which implies that the register MUST be read TWICE before the bit can be considered valid. If Link Status is set to a 1, the next step is to read bit 1 in Extended Register 0 for determining the correct line speed.

10.4 User Test Modes

The 82553 User Test Modes:

- Improve the control and ability to observe internal blocks.
- Reduce production cost by shortening test times.
- Reduce burn-in test cost.

10.5 Autopolarity

The 82553 monitors the link beat pulses and determines if the polarity of one or more of its receive pairs (2, 3 and 4) is reversed. If the SFDs (either 10 Mbps or 100 Mbps) are received with reversed polarity on any given pair, the 82553 will automatically switch the differential pair internally. The 82553 will default to no reversed polarity on any receive pair.

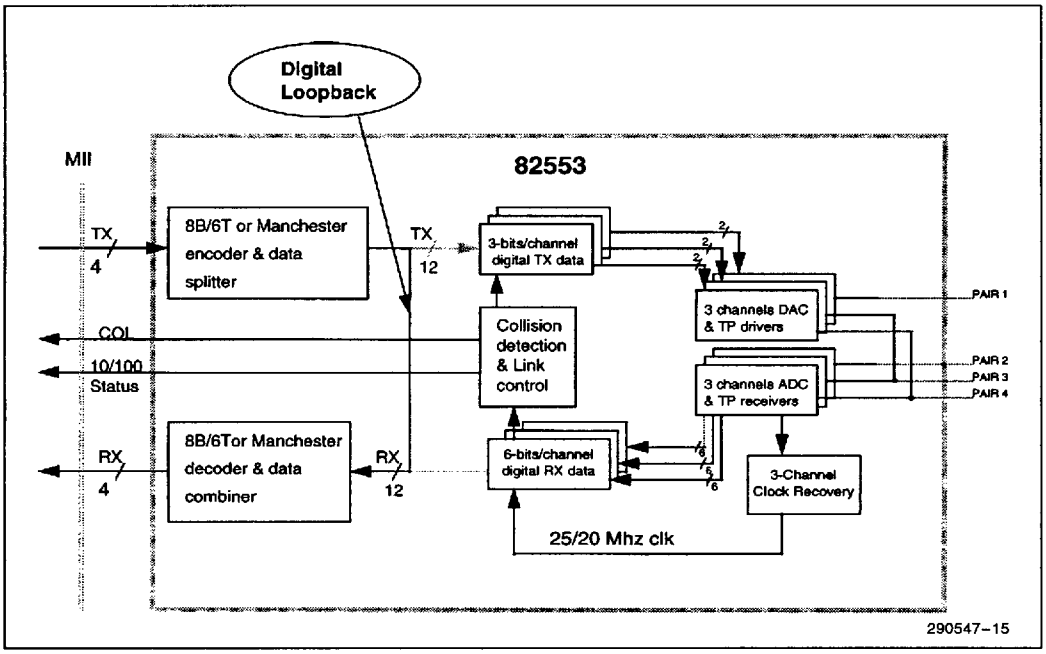

Figure 15. 82553 Analog and Digital Loopback Paths

The following test modes are suggested for the 82553 based on the values of the TEST2, TEST1 and TEST0 pins.

Table 14. User Test Modes

TEST2	TEST1	TEST0	Test Name	Test Function
0	0	0	Disabled	No test mode is enabled.
0	0	1	Reserved	
0	1	0	V_{IL}/V_{IH}	This mode enable testing all inputs for V_{IL}/V_{IH}. If this test passes, a dedicated pin will go to high state.
0	1	1	V_{OL}/V_{OH}	This mode enable testing all outputs for V_{OL}/V_{OH}. If this test passes, a dedicated pin will go to high state.
1	0	0	Nand Tree	The Nand Tree internally NAND combines all 82553 pins and produces an output.
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

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11.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

11.1 Absolute Maximum Ratings

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Case Temperature under Bias	0°C to +85°C
Storage Temperature	−65°C to +140°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to 6.0V

For more information on the quality and reliability of the 82557, refer to the *Components Quality and Reliability Handbook,* order number 210997.

When the 82553 is actively transmitting and receiving in 100Base-T4 mode, it will consume an average of 300 mA at 5V. The 82553 also has a special power saving mode which allows this value to be dropped to 200 mA at 5V whenever there is no transmit activity (the power savings mode is enabled automatically). When idle, the 82553 consumes approximately 80 mA.

11.2 DC Characteristics (V_{CC} = 5V ± 5%, T_C = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3	V	
V_{IH}(X1)	X1 Input High Voltage	3.7	V_{CC}+0.3	V	X1
V_{IL}(X1)	X1 Input Low Voltage	−0.3	0.8	V	X1
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −4 mA
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 4 mA
V_{OH}(LED)	Output High Voltage	3.9		V	I_{OH} = −500 μA
V_{OL}(LED)	Output Low Voltage		0.45	V	I_{OL} = 10 mA
I_{OZ}	Offstate Output Current with High/Low Level Voltage Applied		±15	μA	0 ≤ V_{OUT} ≤ V_{CC}
I_{LI}	Input Leakage Current		±15	μA	0 ≤ V_{IN} ≤ V_{CC}
I_{CC}	Power Supply Current		300	mA	@ f_{RCLK} = 25 MHz
I_{CCPD}	Power Down Supply Current		5	mA	
C_{IN}	Digital Input Buffer Cap		8	pF	@ f = 1 MHz
C_{OUT}	Digital Output Buffer Cap		8	pF	@ f = 1 MHz
C_{X1}	X1 Input Cap		15	pF	@ f = 1 MHz
R_{DIFF}	Input Differential Resistance	9		KΩ	
V_{IDF}	Input Differential Accept Input Differential Reject		2.9 2.7	V_p V_p	
Rs	Output Source Resistance	1		MΩ	
V_{ODF}	Output Differential Voltage	±1.15	±8.85	V	

11.3 AC Timing Characteristics and Measurement Conditions

NOTES:
1. T_C = 0°C to +85°C, V_{CC} = 5V ±5%
2. AC Load
   a. MOS = 20 pF total capacitance to ground.
   b. TPE = 20 pF total capacitance to ground.

11.4 Clock Timing (f = 20 MHz)

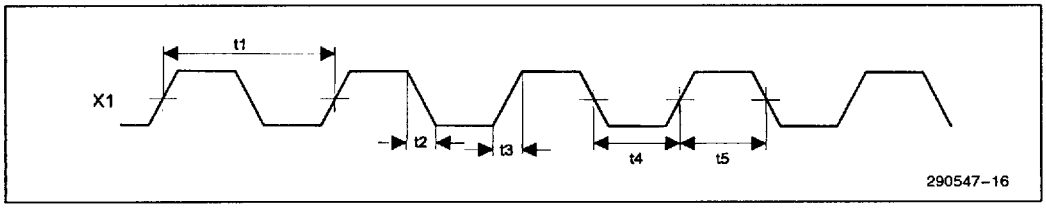

Figure 16. Clock Timing at 20 MHz

Symbol	Parameter	Min	Typ	Max	Units
t1	X1 Cycle Time	49.995	50	50.005	ns
t2	X1 Fall Time			4	ns
t3	X1 Rise Time			4	ns
t4	X1 Low Time	17.5		22.5	ns
t5	X1 High Time	17.5		22.5	ns

11.5 Clock Timing (f = 50 MHz)

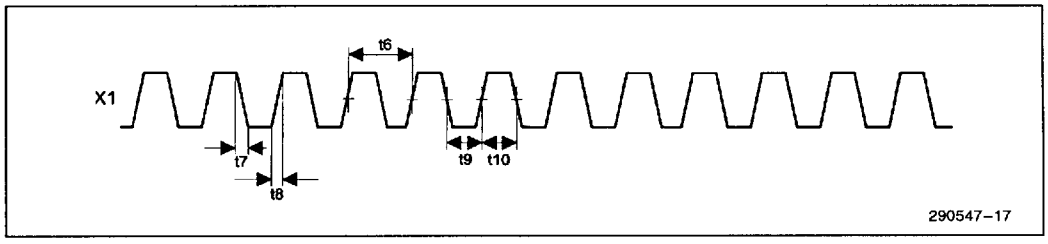

Figure 17. Clock Timing at 50 MHz

Symbol	Parameter	Min	Typ	Max	Units
t6	X1 Cycle Time	19.998	20	20.002	ns
t7	X1 Fall Time			4	ns
t8	X1 Rise Time			4	ns
t9	X1 Low Time	9		11	ns
t10	X1 High Time	9		11	ns

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11.6 Controller Interface Timings (100 Mbit Mode, 10 Mbit MII Mode, 10 Mbit Serial Mode)

11.6.1 TRANSMIT TIMINGS (Controller Interface)

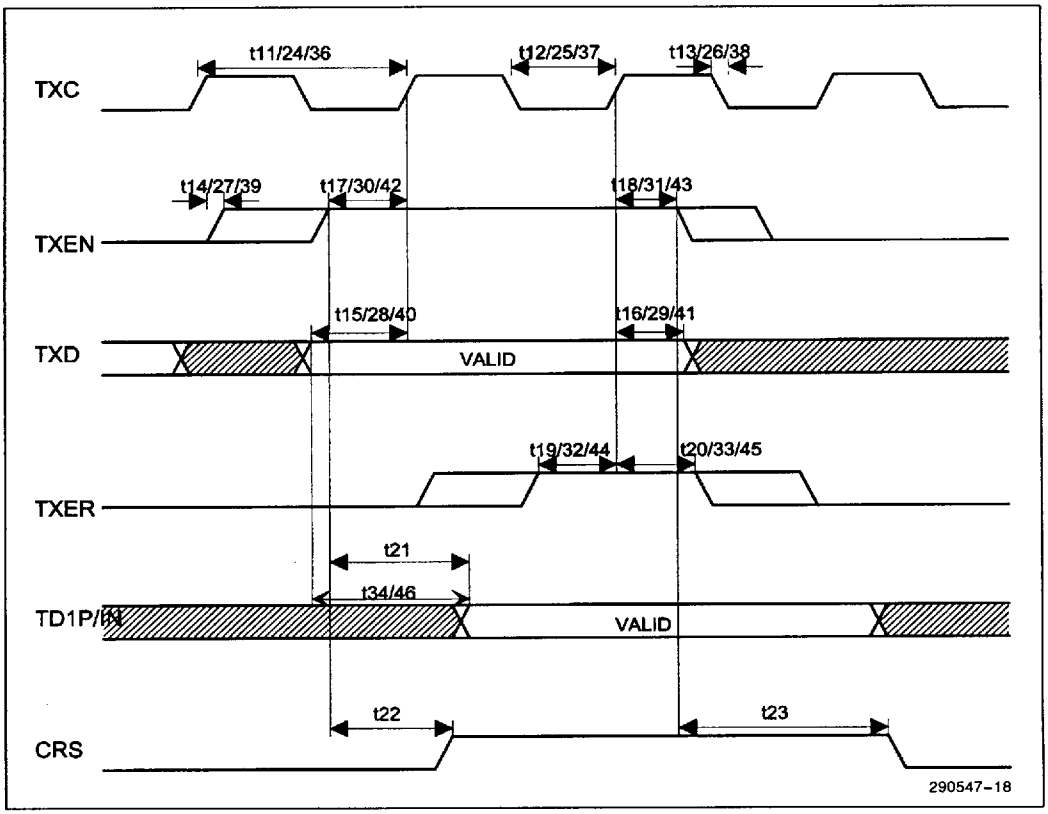

Figure 18. Transmit Timings at 100 Mbps

100 Mbit Mode

Symbol	Parameter	Min	Typ	Max	Unit
t11	TXC Cycle Time	39.996	40	40.004	ns
t12	TXC High/Low Time	14	20	26	ns
t13	TXC Rise/Fall Time	1.3		1.7	ns
t14	TXD and TXEN Rise/Fall Time	1.3		1.7	ns
t15	TXD0–5 Setup Time to TXC ↑	10			ns
t16	TXD0–5 Hold Time from TXC ↑	0			ns
t17	TXEN Setup Time to TXC ↑	10			ns
t18	TXEN Hold Time from TXC ↑	0			ns
t19	TX_ER Setup Time to TXC	10			ns
t20	TX_ER Hold Time to TXC	0			ns
t21	PMA_OUT + TEN_OUT (TXEN to TD1P Delay)	25		130	ns
t22	TXEN_CRS(TXEN to CRS Delay)	0	40		ns
t23	NOT_TXEN_CRS (TXEN Inactive to CRS Inactive Delay)	0	40		ns

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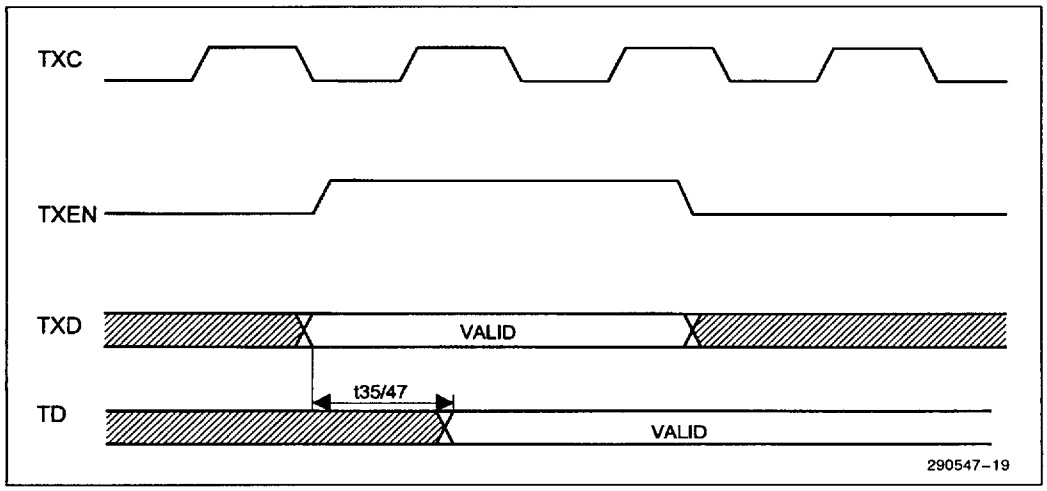

Figure 19. Transmit Timings at 10 Mbps

10 Mbit MII Mode

Symbol	Parameter	Min	Typ	Max	Unit
t24	TXC Cycle Time	399.96	400	400.04	ns
t25	TXC High/Low Time	140	200	260	ns
t26	TXC Rise/Fall Time	1.3		1.7	ns
t27	TXD and TXEN Rise/Fall Time	1.3		1.7	ns
t28	TXD0–5 Setup Time to TXC ↑	20			ns
t29	TXD0–5 Hold Time from TXC ↑	0			ns
t30	TXEN Setup Time to TXC ↑	20			ns
t31	TXEN Hold Time from TXC ↑	0			ns
t32	TX__ER Setup Time to TXC	20			ns
t33	TX__ER Hold Time to TXC	0			ns
t34	TXD to TD Steady State Propagation Delay			400	ns
t35	TXD to TD1P Startup Delay			400	ns

10 Mbit Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
t36	TXC Cycle Time	99.99	100	100.01	ns
t37	TXC High/Low Time	45	50	55	ns
t38	TXC Rise/Fall Time	1.3		1.7	ns
t39	TXD and TXEN Rise/Fall Time	1.3		1.7	ns
t40	TXD0–5 Setup Time to TXC ↑	20			ns
t41	TXD0–5 Hold Time from TXC ↑	0			ns
t42	TXEN Setup Time to TXC ↑	20			ns
t43	TXEN Hold Time from TXC ↑	0			ns
t44	TX__ER Setup Time to TXC	20			ns
t45	TX__ER Hold Time to TXC	0			ns
t46	TXD to TD Steady State Propagation Delay			400	ns
t47	TXD to TD Startup Delay			400	ns

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11.6.2 RECEIVE TIMINGS (Controller Interface)

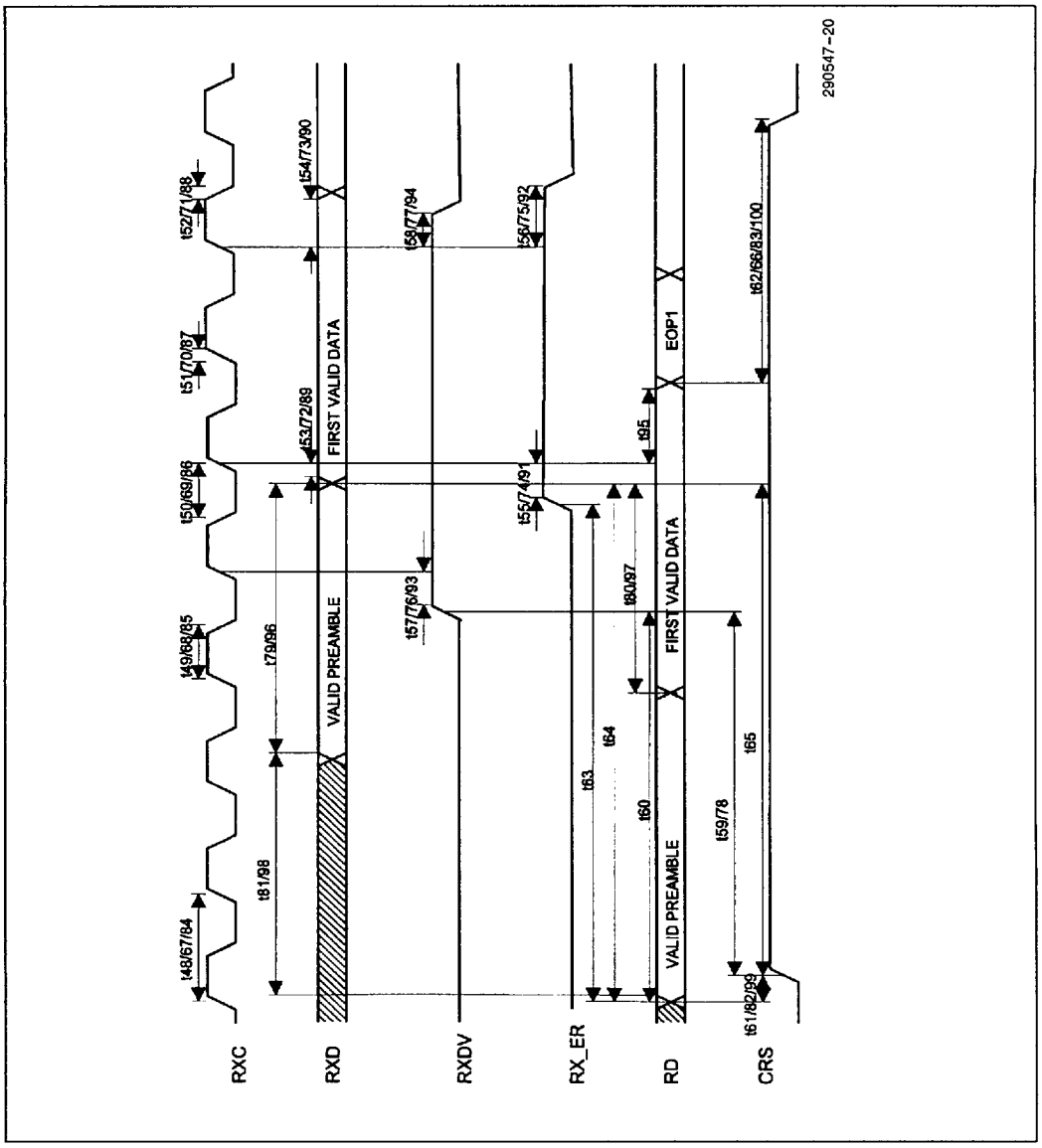

Figure 20. Receive Timings

100 Mbit MODE

Symbol	Parameter	Min	Typ	Max	Unit
t48	RXC Cycle Time	39.996	40	40.004	ns
t49	RXC High Time	14	20	26	ns
t50	RXC Low Time	14	20	26	ns
t51	RXC Rise Time	1.3		1.7	ns
t52	RXC Fall Time	1.3		1.7	ns
t53	RXD0-5 Setup from RXC ↑	10			ns
t54	RXD0-5 Hold from RXC ↑	10			ns
t55	RX__ER Setup Time to RXC ↑	10			ns
t56	RX__ER Hold Time to RXC ↑	10			ns
t57	RXDV Setup Time to RXC ↑	10			ns
t58	RXDV Hold Time to RXC ↑	10			ns
t59	RS Assert to RXDV Assert Delay	530		1145	ns
t60	RD to RXDV Delay	765		1100	ns
t61	RX__CRS (CRS Assertion (RD active to CRS) Delay)	0		230	ns
t62	RS Deassertion Delay (RD off to CRS) Delay	0		470	ns
t63	RX__PMA__ERR (RD to RXERR)	625		1070	ns
t64	RX__PMA__DATA (RD to RXD)	625		860	ns
t65	RS__PMA__DATA (CRS to RXD)	0		785	ns
t66	EOP__CARRIER__STATUS	465		700	ns

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10 Mbit MII Mode

Symbol	Parameter	Min	Typ	Max	Unit
t67	RXC Cycle Time	399.6	400	400.4	ns
t68	RXC High Time	140	200	260	ns
t69	RXC Low Time	140	200	260	ns
t70	RXC Rise Time	1.3		1.7	ns
t71	RXC Fall Time	1.3		1.7	ns
t72	RXD0–5 Setup from RXC ↑	10			ns
t73	RXD0–5 Hold from RXC ↑	10			ns
t74	RX_ER Setup Time to RXC ↑	10			ns
t75	RX_ER Hold Time to RXC ↑	10			ns
t76	RXDV Setup from RXC ↑	10			ns
t77	RXDV Hold from RXC ↑	10			ns
t78	CRS Assert to RXDV Assert Delay			1500	ns
t79	RD2P to RXD Bit Loss at Start of Packet	4		16	Bits
t80	RD2P to RXD Steady State Propagation Delay			400	ns
t81	RD2P to RXD0–5 Startup Delay			2.0	μs
t82	CRS Assertion (RD active to CRS) Delay			700	ns
t83	CRS Deassertion Delay (RD off to CRS) Delay (Last Bit of SOI)			450	ns

10 Mbps Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
t84	RXC Cycle Time	99.99	100	100.01	ns
t85	RXC High Time	45	50	55	ns
t86	RXC Low Time	45	50	55	ns
t87	RXC Rise Time	1.3		1.7	ns
t88	RXC Fall Time	1.3		1.7	ns
t89	RXD0–5 Setup from RXC ↑	10			ns
t90	RXD0–5 Hold from RXC ↑	10			ns
t91	RX_ER Setup Time to RXC ↑	10			ns
t92	RX_ER Hold Time to RXC ↑	10			ns
t93	RXDV Setup from RXC ↑	10			ns
t94	RXDV Hold Time to RXC ↑	10			ns
t95	CRS Deassertion Hold Time from RXC High	10			ns
t96	RD2P to RXD Bit Loss at Start of Packet	4		16	Bits
t97	RD to RXD Steady State Propagation Delay			400	ns
t98	RD to RXD0–5 Startup Delay			2.0	μs
t99	CRS Assertion (RD active to CRS) Delay			700	ns
t100	CRS Deassertion Delay (RD off to CRS) Delay			450	ns

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11.7 Collision Timings

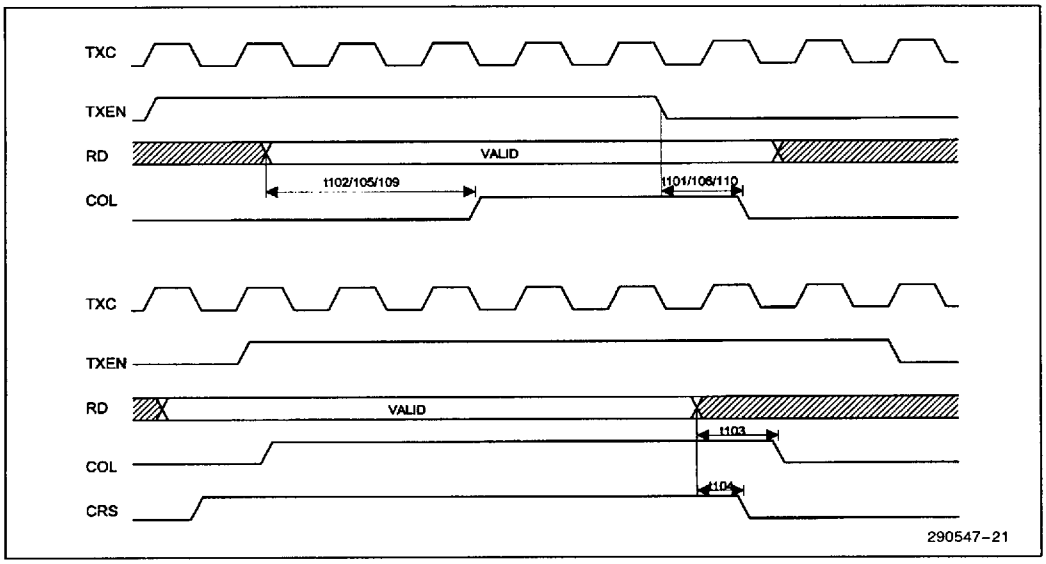

Figure 21. Collision Timings

100 Mbit Mode

Symbol	Parameter	Min	Typ	Max	Unit
t101	TX__NOT__COL (TXEN Inactive to COL Inactive Delay)	0	134	360	ns
t102	RX__COL (RD to COL Delay)	0	158	275	ns
t103	RX__NOT__ COL (RD Inactive to COL Inactive Delay)	0	176	515	ns
t104	EOC__CARRIER__STATUS	0		460	ns

10 Mbit MII Mode

Symbol	Parameter	Min	Typ	Max	Unit
t105	Onset of Collision (RD Pair and TXEN Active) to COL Assert			900	ns
t106	End of Collision (RD Pair or TXEN Inactive) to COL Deassert			900	ns

10 Mbit Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
t109	Onset of Collision (RD Pair and TXEN Active) to COL Assert			900	ns
t110	End of Collision (RD Pair or TXEN Inactive) to COL Deassert			900	ns

11.8 Link Integrity Timings

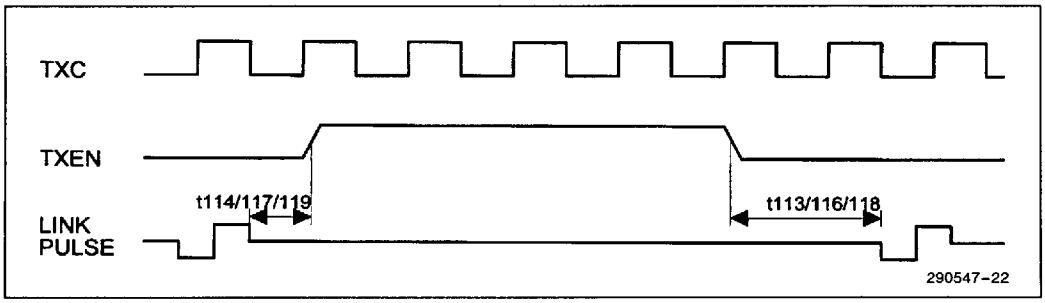

Figure 22. Link Integrity Timings

100 Mbit Mode

Symbol	Parameter	Min	Typ	Max	Unit
t113	Last Transmit Activity to Link Test Pulse	0.6		1.8	ms
t114	Link Test Pulse to Data Separation	40			ns

10 Mbit MII Mode

Symbol	Parameter	Min	Typ	Max	Unit
t116	Last Transmit Activity to Link Test Pulse	8		24	ms
t117	Link Test Pulse to Data Separation	100			ns

10 Mbit Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
t118	Last Transmit Activity to Link Test Pulse	8		24	ms
t119	Link Test Pulse to Data Separation	100			ns

11.9 Signal Quality Error Timings

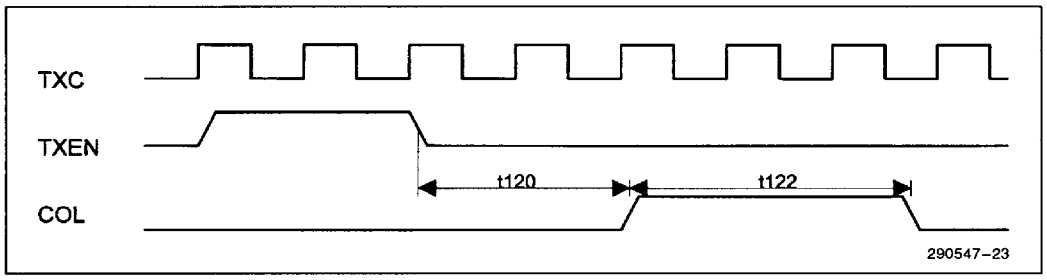

Figure 23. Signal Quality Error Timings

10 Mbit Serial and MII Mode

Symbol	Parameter	Min	Typ	Max	Unit
t120	TXEN Deassert to CDT	0.6	1	1.2	μs
t121	SQE Test Wait Time	0.6		1.6	μs
t122	SQE Test Duration	0.5		1.5	μs

11.10 Loopback Timings

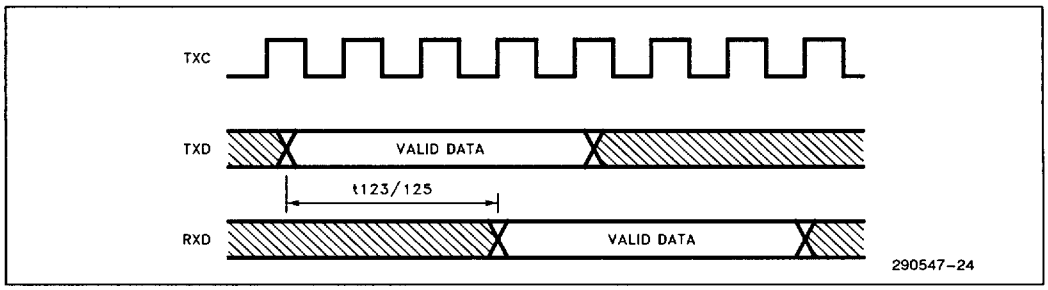

Figure 24. Loopback Timings

100 Mbit, 10 Mbit MII, and Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
t123	TXD to RXD Steady State Propagation Delay in 100 Mbit Mode			480	ns
t125	TXD to RXD Steady State Propagation Delay in 10 Mbit and Serial Mode			600	ns

11.11 Jabber Timings (10 Mbit/s Operation Only)

Symbol	Parameter	Min	Typ	Max	Unit
	Jabber Time Enable		40		ms
	Un-jabber Timer		367		ms

11.12 LED Timings

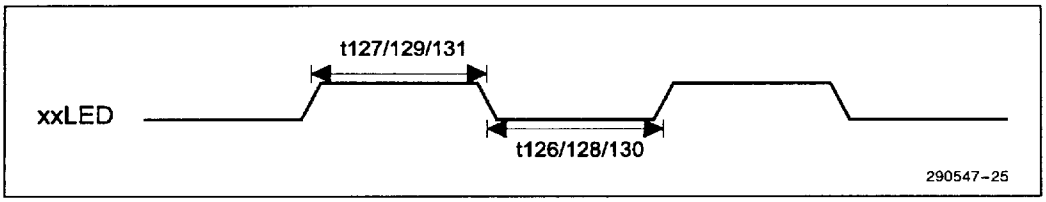

Figure 25. LED Timings

100 Mbit Mode

Symbol	Parameter	Min	Typ	Max	Unit
t126	LILED On Time	167			ms
t127	LILED Off Time	167			ms
t128	ACTLED On Time	167			ms
t129	ACTLED Off Time	167			ms

10 Mbit Mode

Symbol	Parameter	Min	Typ	Max	Unit
t130	ACTLED On Time	209			ms
t131	ACTLED Off Time	209			ms

11.13 Management Data Interface Timings

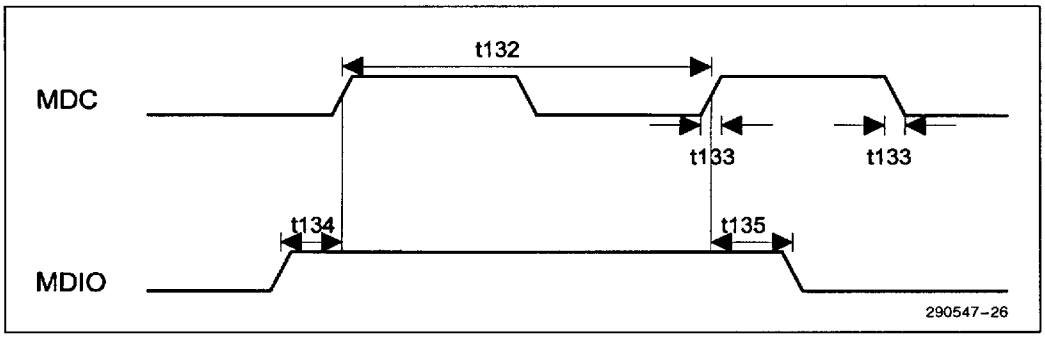

Figure 26. MDI Timings

Symbol	Parameter	Min	Typ	Max	Unit
t132	MDC Cycle Time	400			ns
t133	MDC Rise/Fall Time			5	ns
t134	MDI Setup Time to MDC ↑	10			ns
t135	MDI Hold Time from MDC ↑	10			ns

12.0 PHYSICAL ATTRIBUTES AND DIMENSIONS

This section provides the physical packaging information for the 82553. The 82553 is an 84-lead plastic leaded chip carrier (PLCC) device. Package attributes are provided in Table 15 and dimensions are shown in Figures 27–31. Table 16 shows the dimensions for the figures. For more information on Intel device packagaging, refer to the *Intel Packaging Handbook,* available from Intel Literature or your local sales office.

Table 15. Intel 82553 Package Attributes

Attribute	Value
Lead Count	84
Square or Rectangle?	Square
Pitch (in.)	0.050
Package Thickness (in.)	0.150
Weight (gm)	6.2
Shipping Media	Trays, Tubes, Tape and Reel
Desiccant Pack	Yes
Comments	All PLCCs are "J" Lead

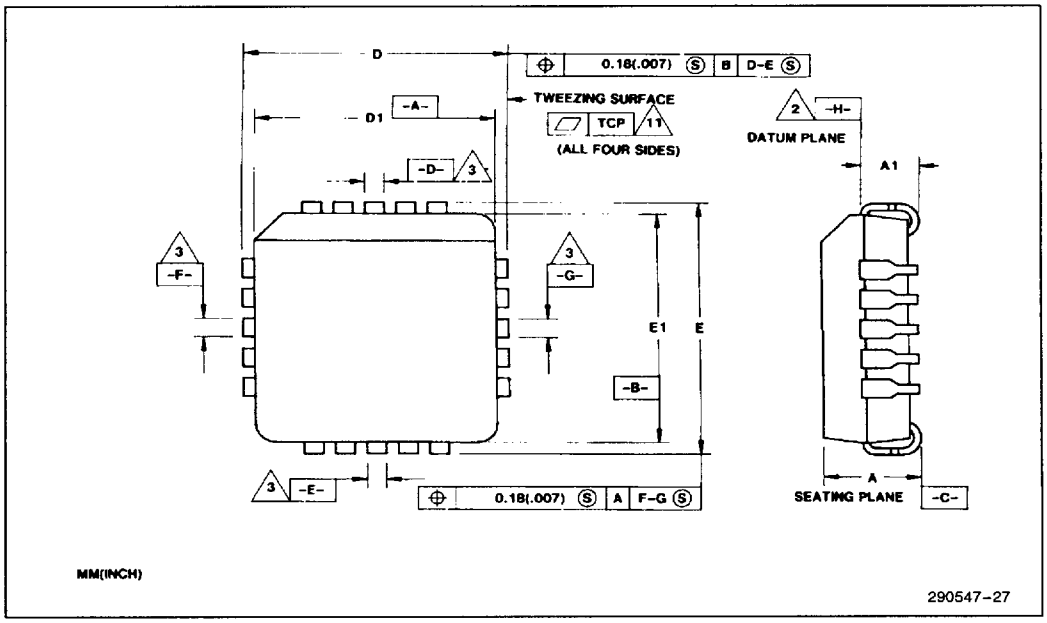

Figure 27. Principal Dimensions for 82553 Package

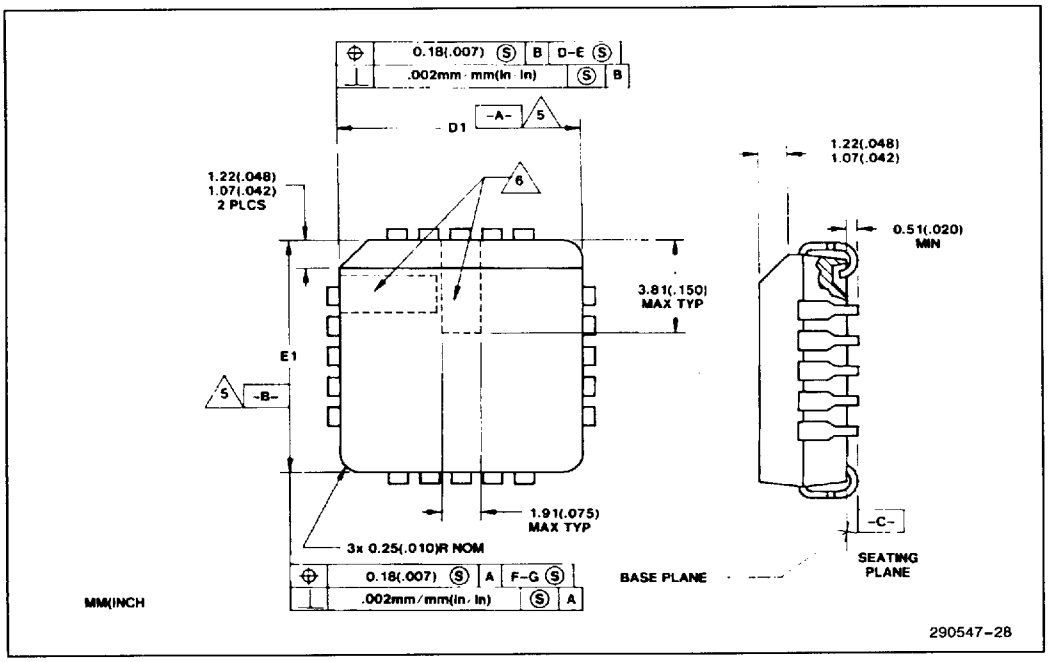

Figure 28. Molded Details

Table 16. Quad Flatpack Dimensions in Figures 27–31

Symbol	Minimum	Maximum
A	0.165	0.190
A1	0.090	0.120
D	1.185	1.195
D1	1.15	1.158
D2	1.090	1.130
E	1.185	1.195
E1	1.15	1.158
E2	1.090	1.130
N	84	
CP	0	0.004
TCP	0	0.004
LT	0.008	0.014
Dimensions are in inches		

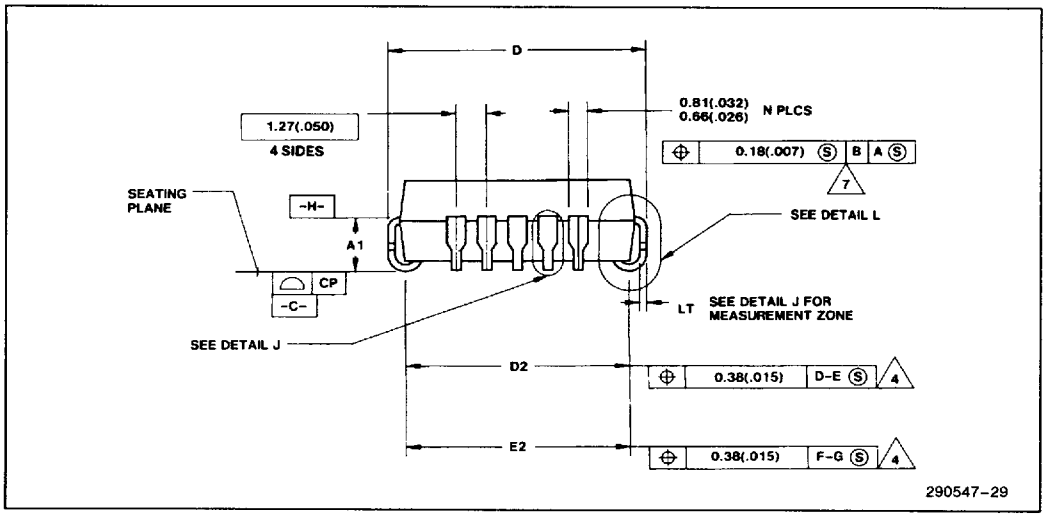

Figure 29. Terminal Details

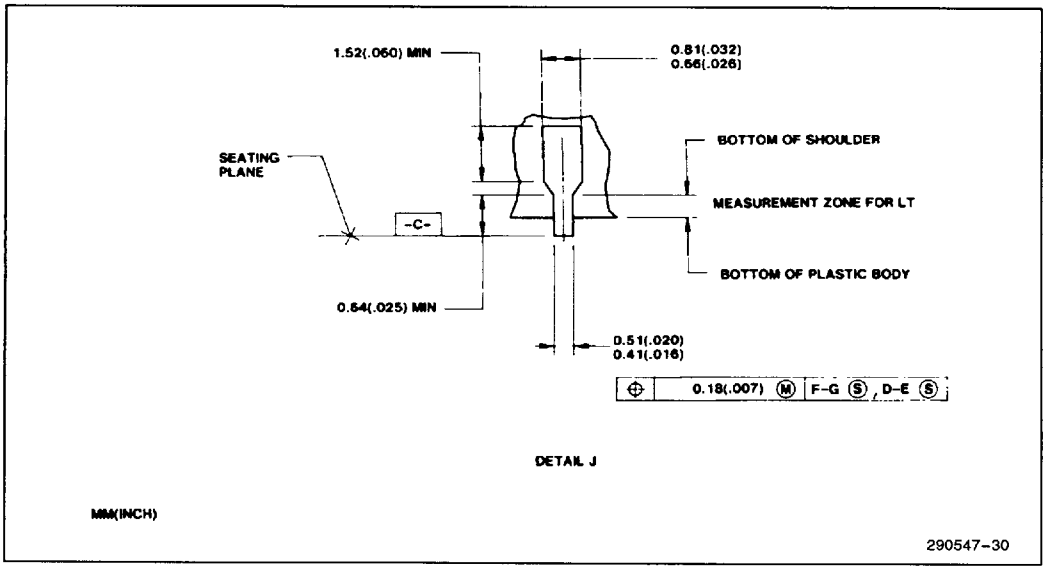

Figure 30. Terminal Details (Continued)—Detail J

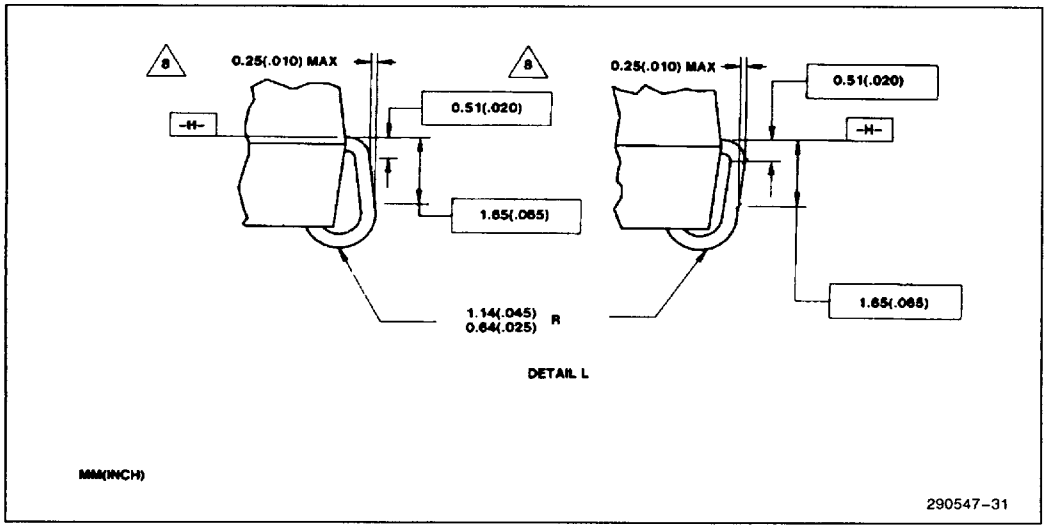

Figure 31. Terminal Details (Continued)—Detail L

NOTES SQUARE PACKAGE:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane —H— located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Datums D—E and F—G to be determined where center leads exit plastic body at datum plane —H—.
4. To be determined at seating plane —C—.
5. Dimensions D_1 and E_1 do not include protrusion.
6. Pin 1 identifier is located within one of the two defined zones.
7. Locations to datum —A— and —B— to be determined at plane —H—.
8. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
9. Controlling dimension, inch.
10. All dimensions and tolerances include lead trim offset and lead plating finish.
11. Tweezing surface planarity is defined as the furthest any lead on a side may be from the datum. The datum is established by touching the outermost lead on that side and parallel to D—E or F—G.

13.0 REVISION HISTORY

The following chart outlines important changes made to the data sheet.

Date of Change	Section Number	Description
12-95	2.4	Expanded desc. for TXD4
12-95	2.5	Deletion in TESTEXT
12-95	2.7, 2.8	Revised section for B1 stepping; new section for C stepping
12-95	6.0	Revised Table 2
12-95	8.3, 8.4	Revised text for B1 and C stepping clarification
12-95	9.1, 9.2	Revised text for B1 and C stepping clarification
12-95	Fig. 11, 12, 13	Revised artwork for readability
12-95	Various	Added shading to denote C stepping functionality
01-96	2	Revised Figure 3 for stepping differences
01-96	4.3	Revised Figure 8
01-96	5.2.2	Revised Figure 10
01-96	7.2	Added stepping differences, shading
01-96	—	Revised Figure 1
01-96	7.1.3	Added register values for part steppings
01-96	7.1.9	Added Extended Register 2 for C Step part

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