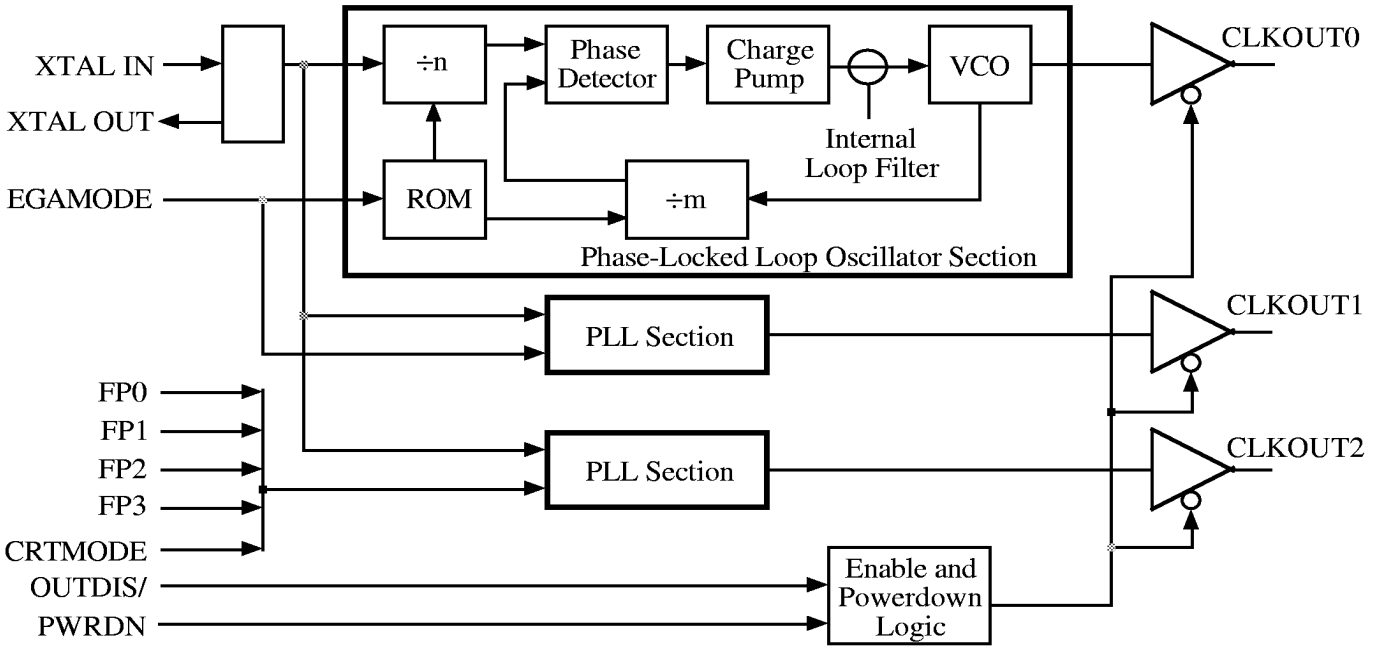
82C401A
Flat Panel/CRT
Clock Synthesizer

- 3 Independent Clock Outputs
- Supports all 82C455, 82C456, 82C457 and 82C451 Clock Frequency Requirements
- Supports DRAM Refresh in Powerdown mode
- Low Power Consumption
- Reduced Board Space Requirements
- 3-State Output Control Disables Outputs for Test Purposes
- 5-Volt Operation
- Internal Loop Filter Requires no External Components
- Frequency Selection Scheme Compatible with Chips BIOS and Extended Mode Drivers
- Frequencies Supported up to 40 MHz
- 16-pin DIP or SOIC Package
- Reference Frequency uses Standard 14.31818 MHz Crystal
- Low-Power, High Speed 1.25µ CMOS Technology



82C401A Functional Block Diagram

Revision History

Revision	Date	By	Comment
0.01	7/23	DR	Draft Copy
0.1	7/31	DR	Review Copy before formatting
0.2	8/1	DR	Added Table of Contents and List of Figures
0.3	1/91	DR	Output Freq. - line inserted in equation. DC Characteristics - first 4 lines of table changed.
0.4	5/91	DR/ST	Added 82C40x Clock Chip Layout and Pin List.

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Introduction

In applications requiring two or more TTL oscillators, board space, power consumption, and cost may be reduced by using a clock synthesis chip. In portable computer designs, these factors are extremely important.

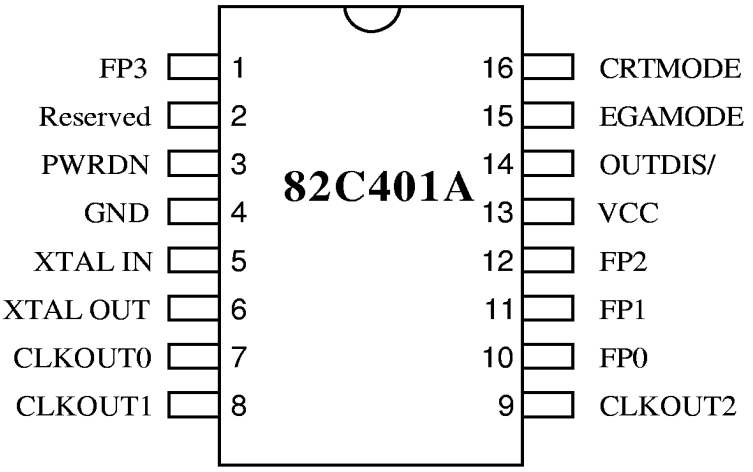
The 82C401A clock synthesis chip is designed specifically for interfacing to Chips and Technologies 82C455, 82C456, 82C457 and 82C451 VGA Controllers. The 82C401A features three independent clock outputs plus a powerdown mode compatible with the 82C455 and 82C456.

The 82C401A replaces both standard VGA TTL oscillators (25.175 and 28.322 MHz) plus the 40 MHz TTL oscillator which is used for both the master clock (MCLK) and the 800x600 video clock. In addition, the 82C401A provides a wide selection of frequencies compatible with most flat panels and CRTs.

The active power of the triple output 82C401A is typically less than the TTL oscillators which it replaces. When in powerdown mode, the power consumption of both the 82C401A and the VGA controller are reduced. The power consumption of the 82C401A is reduced because it disables all three of its internal VCO's. The 82C401A does keep the reference frequency running, dividing it by an integral value to generate an output frequency which will guarantee DRAM refresh by the 82C455/456/457. The resulting frequency fed to the 82C455/456/457 is much lower than the active input hence this feature reduces power consumption in the 82C455/456/457 as well.

The 82C401A requires no buffering into the VGA controller. The output drive of the 82C401A is matched to the input characteristics of an 82C45x clock pin. This reduces the overshoot and undershoot problems which are encountered when designing with fast TTL oscillators. As a result, high frequency noise within the clock circuit is reduced which facilitates compliance to FCC standards.

82C401A Pinouts



82C401A Pin List

Pin Name	Pin #
CLKOUT0	7
CLKOUT1	8
CLKOUT2	9
CRTMODE	16
EGAMODE	15
FP0	10

Pin Name	Pin #
FP1	11
FP2	12
FP3	1
GND	4
OUTDIS/	14

Pin Name	Pin #
PWRDN	3
RESERVED	2
XTAL IN	5
XTAL OUT	6
VCC	13

82C401A PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
1 12 11 10	FP3 FP2 FP1 FP0	In In In In	High High High High	Flat Panel Frequency Select. These pins select the frequency which is output on CLKOUT2 when CRTMODE = 0. There are 12 flat panel frequencies from which to select:

FP3	FP2	FP1	FP0	Frequency (MHz)
0	0	0	0	40.000
0	0	0	1	36.000
0	0	1	0	32.000
0	0	1	1	30.000
0	1	0	0	28.322
0	1	0	1	26.000
0	1	1	0	25.175
0	1	1	1	24.000
1	0	0	0	20.000
1	0	0	1	16.000
1	0	1	0	14.318
1	0	1	1	12.000

16	CRTMODE	In	Both	Selects between the CRT frequency set and the FLAT PANEL frequency set for output on CLKOUT2. 0 = FLAT PANEL (as selected by user) 1 = CRT (40.000/32.500 MHz)
15	EGAMODE	In	Both	Selects between VGA and EGA frequencies for output on CLKOUT0 and CLKOUT1:

EGAMODE	CLKOUT0	CLKOUT1
0	25.175	28.322
1	14.318	16.257

3	PWRDN	In	High	Compatible with the 82C455, 82C456, and 82C457 powerdown input pin. When active, the 82C401A switches into a power saving mode. It disables outputs on CLKOUT0, and CLKOUT1 (forces the outputs low) and lowers the CLKOUT2 frequency to approximately 795 KHz. This is the lowest frequency resulting from an integral division of the reference for which the 82C455/456/457 can maintain DRAM refresh. 0 = Normal Operation 1 = Powerdown mode

82C401A PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
14	OUTDIS/	In	Low	Output Disable. This disables all three of the clock outputs and puts those pins into a high-impedance mode. This is useful for automated board test or for multiplexing additional clocks into the VGA controller. This pin has an internal pull-up and may be left unconnected if not used. 0 = Clock outputs disabled 1 = Clock outputs enabled (default)
5	XTAL IN	In	Both	Reference frequency input (if using an external oscillator) or 14.31818 MHz crystal input.
6	XTAL OUT	Out	Both	Optional Oscillator output to a 14.31818 MHz (Series Resonant) crystal. All passive components required for series resonant operation are implemented internally to the 82C401A.
7	CLKOUT0	Out	Both	Clock Output 0. This should be connected directly to the CLK0 input on the VGA controller. It provides 25.175 MHz (EGAMODE = 0) or 14.318 MHz (EGAMODE = 1) clock frequencies. The output impedance has been matched for a standard layout and the input impedance of an 82C45x VGA controller.
8	CLKOUT1	Out	Both	Clock Output 1. This should be connected directly to the CLK1 input on the VGA controller. It provides 28.322 MHz (EGAMODE = 0) or 16.257 MHz (EGAMODE = 1) clock frequencies. The output impedance has been matched for a standard layout and the input impedance of an 82C45x VGA controller.
9	CLKOUT2	Out	Both	Clock Output 2. This pin should be connected to the CLK2 input on the VGA controller. It provides a 40 MHz clock for 800x600 CRT resolution as well as a selection of Flat Panel frequencies (see FP3:0 pin description).
2	RESERVED	NC		Reserved pin (do not connect).
13	VCC	Power		+5V Power Supply.
4	GND	Ground		Ground Pin.

Functional Description

Clock Oscillator Selection

The output frequency values of the dedicated CRT clock oscillators (CLKOUT0, and CLKOUT1) are selected by the EGAMODE, PWRDN, and OUTDIS/ pins as shown below:

OUTDIS/	PWRDN	EGAMODE	CLKOUT0 (MHz)
0	X	X	HIGH-Z
1	0	0	25.175
1	0	1	14.31818
1	1	X	LOW

CLKOUT0 Frequency Select

OUTDIS/	PWRDN	EGAMODE	CLKOUT1 (MHz)
0	X	X	HIGH-Z
1	0	0	28.322
1	0	1	16.257
1	1	X	LOW

CLKOUT1 Frequency Select

CLKOUT2 decodes the CRTMODE signal to select between the 40 MHz CRT mode and the selected Flat Panel frequency. The selection table for CLKOUT2, including the ROM decode options for the flat panel frequency, are shown below:

At any time during operation, the selection lines can be changed to choose a different frequency. The internal phase-lock loop will immediately begin to seek the newly selected frequency. During the transition period, the clock output may glitch. The intermediate frequency will not exceed the higher of the two transition frequencies.

3-State Output Operation

The OUTDIS/ signal, when pulled low, will 3-state all three of the clock output lines. This supports "wired-or" connections between external clock lines (e.g. the Feature Connector external clock) and allows for procedures such as automated testing, where the clock must be disabled. The OUTDIS/ signal contains an internal pull-up and may be left unconnected if it is not required.

Optional External Crystal

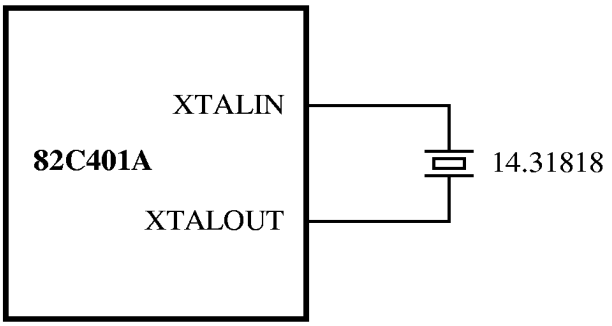
Normal operation requires a nominal 14.31818 MHz reference signal which is standard in all PC systems. If the 82C401A is used in a motherboard application then it can be used to generate the 14.31818 MHz clock (XTAL OUT) required for the system. If the 14.31818 MHz clock is generated elsewhere on the motherboard, it may be connected directly to the 82C401A (XTAL IN). In motherboard applications,

OUTDIS/	PWRDN	CRTMODE	EGAMODE	FP3	FP2	FP1	FP0	CLKOUT2 (MHz)
0	X	X	X	X	X	X	X	HIGH-Z
1	0	1	0	X	X	X	X	40.000
1	0	1	1	X	X	X	X	32.500
1	0	0	X	0	0	0	0	40.000
1	0	0	X	0	0	0	1	36.000
1	0	0	X	0	0	1	0	32.000
1	0	0	X	0	0	1	1	30.000
1	0	0	X	0	1	0	0	28.322
1	0	0	X	0	1	0	1	26.000
1	0	0	X	0	1	1	0	25.175
1	0	0	X	0	1	1	1	24.000
1	0	0	X	1	0	0	0	20.000
1	0	0	X	1	0	0	1	16.000
1	0	0	X	1	0	1	0	14.318
1	0	0	X	1	0	1	1	12.000
1	0	0	X	1	1	0	0	X
1	0	0	X	1	1	0	1	X
1	0	0	X	1	1	1	0	X
1	0	0	X	1	1	1	1	X
1	1	X	X	X	X	X	X	0.795

CLKOUT2 Frequency Select

control over the quality of the reference clock is guaranteed by the layout and design. When placing the 82C401A on a daughter card, the stability of the system bus 14.31818 MHz reference frequency is not assured. In the majority of PC designs, this signal is stable enough for use with the 82C401A.

For those cases where a stable noise-free system clock cannot be guaranteed, the 82C401A includes a built-in oscillator which can serve as the reference source. If this mode is desired, an external series-resonant 14.31818 MHz crystal should be connected between the XTAL IN and XTAL OUT pins. No additional resistors or capacitors are required. All components necessary to achieve series resonance are fabricated internal to the 82C401A.



82C401A Crystal Connection

No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the 82C401A. The phase-lock loops require no external capacitors or resistors.

Clock Synthesizer Description

Each of the three oscillator blocks is a classic phase-locked loop connected as shown in the block diagram on the first page. The external input frequency (XTAL IN) is 14.31818 Mhz and goes into a "divide-by-n" block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is essentially a feedback system which attempts to get two signals (the divided reference signal and the divided variable 'synthesized' signal) to arrive in phase. The system attempts to achieve zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower depending on what is required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately 'lock-on' to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal 'loop filter' provides stability and damping.

Output Frequency Accuracy

The accuracy of the output frequency depends upon the target output frequency. The tables within this document contain target frequencies which are different than the actual frequencies produced by the clock synthesizer. The output frequency of the 82C401A clock synthesizer is an integral fraction of the input (reference) frequency:

$$f_{Out} = \frac{2 f_{Ref} m}{n} \qquad m,n \text{ integer}$$

Only certain output frequencies are possible for a particular reference input. The 82C401A always produces an output frequency within 1% of the target. This is more than sufficient to meet standard display requirements.

Minimized Parasitic Problems

All of the 82C40x family of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins isolated as much as possible. Further, all the synthesis VCO's are separated from their digital logic. Finally, separate ground buses for the analog and digital circuitry are used internally. This eliminates the need to provide separate analog and digital VCC and GND to the chip.

The parts use center pins to deliver power and ground to the die instead of the more conventional corner pins. The package leadframes are optimized to have especially wide power and ground leads. This gives the lowest possible inductance from the supply pin on the package to the die within, and results in minimized supply noise problems such as ground-bounce and output crosstalk.

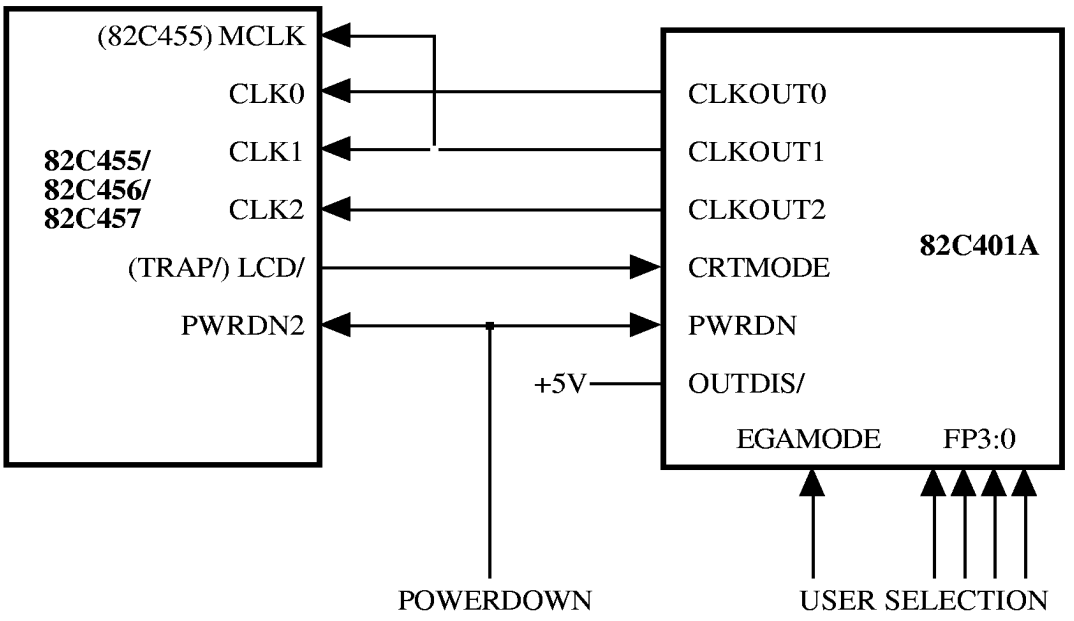
Stability and "Bit-Jitter"

The long–term frequency stability of the 82C40x phase-locked loop frequency synthesis components is guaranteed due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices are affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short–term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The 82C40x frequency synthesis parts have been designed with an emphasis on reduction of "bit-jitter". The primary cause of this phenomenon is the flutter of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize this "bit-jitter". The 82C40x family of frequency synthesis components are guaranteed to operate at a jitter rate low enough to be visually unnoticeable in the graphics display.

Temperature and Process Sensitivity

Because of its feedback circuitry, the 82C401A is inherently stable over temperature and manufacturing process variations. An advantage of incorporating the loop filter internal to the chip is that the loop filter will track the same process variations as does the VCO. This means no manufacturing tuning is required to filter components as is commonly required for external "de-coupled" filters.



82C401A Interface to an 82C455 / 82C456/82C457

82C40x Clock Chip Layout

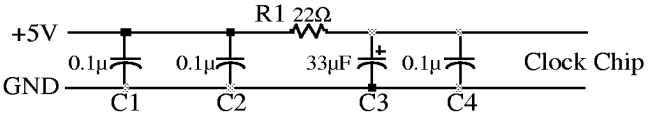
Clock synthesis chips are extremely sensitive to voltage supply noise. This is due in part to their use of VCO's to lock onto the desired frequency. The 82C40x family of clock chips all currently contain multiple Phase Lock Loops (PLLs). Each Phase Lock Loop employs a Voltage Controlled Oscillator (VCO). These VCO's have a very high df/dv so small changes in supply voltage can cause large shifts in output frequency. The stability of the VCO's in graphics applications is critical in order to avoid frequency fluctuations. Temporary phase shifts are seen on the display as jitter. To minimize supply line ripple, CHIPS has developed the following layout suggestions for filtering the power supply to the 82C40x clock chips.

When using the 82C401A, a full power and ground plane layout should be employed both under and around the IC package.

For two layer boards, bring a separate VCC trace from the bus connector up to the clock chip. This is also desirable but not absolutely necessary for multilayer layouts. Filter this trace at its source with a 0.1µF capacitor (C1) and again adjacent to the 22Ω resistor (C2) as shown. Multi layer boards tapping an inner power plane may omit the first 0.1µF capacitor (C1) but should include the second (C2). All designs must include R1, C3, and C4.

The 22Ω resistor acts to filter small fluctuations but also drops the supply voltage to the 82C40x chip by approximately 500mV. This value may be increased to as much as 33Ω in very noisy situations with careful attention given to the supply voltage level at the clock chip. If the supply (VCC) drops below 4.25V at the clock chip then the phase lock loop may lose lock. The 82C40x family of clock chips have been tuned to operate with a 22Ω resistor in series with the VCC input.

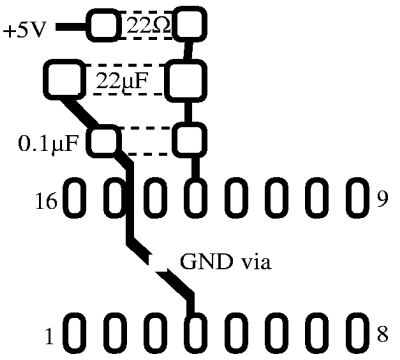
The isolated supply should be filtered by a bulk tantalum 22µF-47µF capacitor and immediately adjacent to the clock chip by another 0.1µF cap. Both capacitors should be placed within 0.15" of the power pin.It is extremely important that the power supply trace to the clock chip pass from the 22Ω resistor, connecting the bulk capacitor, then connecting the 0.1µF capacitor before reaching the power pin on the clock chip. There will be high frequency noise on the isolated supply trace between the bulk capacitor and the 0.1µF. It is important that the clock chip power pin not see any of this noise so do not route the trace from the bulk cap to the 0.1µF via the power pin. The 0.1µF cap will filter this high frequency noise which may otherwise cause visible jitter on the display. For through-hole designs, use ceramic disk capacitors rather than axial leaded capacitors. Minimizing inductance between the VCC and GND pins on the clock chip is very important. For two layer designs, a GND plane should be placed under the 82C40x and its immediate bypass components.



Clock Chip Power Supply Isolation

The designer should also avoid routing the clock output traces of the 82C401A in close parallel proximity for any great distance. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs and the duty cycle. The 82C401A has been optimized to have its clock output pins connected directly to the VGA controller.

When designing with this device, the best rule to follow is to locate the 82C401A as close to the 82C45x VGA controller as is possible. Do not route high frequency signals such as DRAM control lines near to the 82C401A or its clock outputs. A suggested layout is shown below for the isolated section of the supply.



Suggested Clock Chip Layout

82C401A Electrical Specifications

82C401A ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	175	mW
V_{CC}	Supply Voltage	-0.5	–	7.0	V
V_I	Input Voltage	-0.5	–	V_{CC}+0.5	V
T_{SOL}	Maximum Soldering Temperature (10 sec.)	–	–	260	°C
T_{OP}	Operating Temperature (Ambient)	-25	–	85	° C
T_{STG}	Storage Temperature	-40	–	125	° C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C401A NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
T_A	Ambient Temperature	0	–	70	° C

82C401A DC CHARACTERISTICS

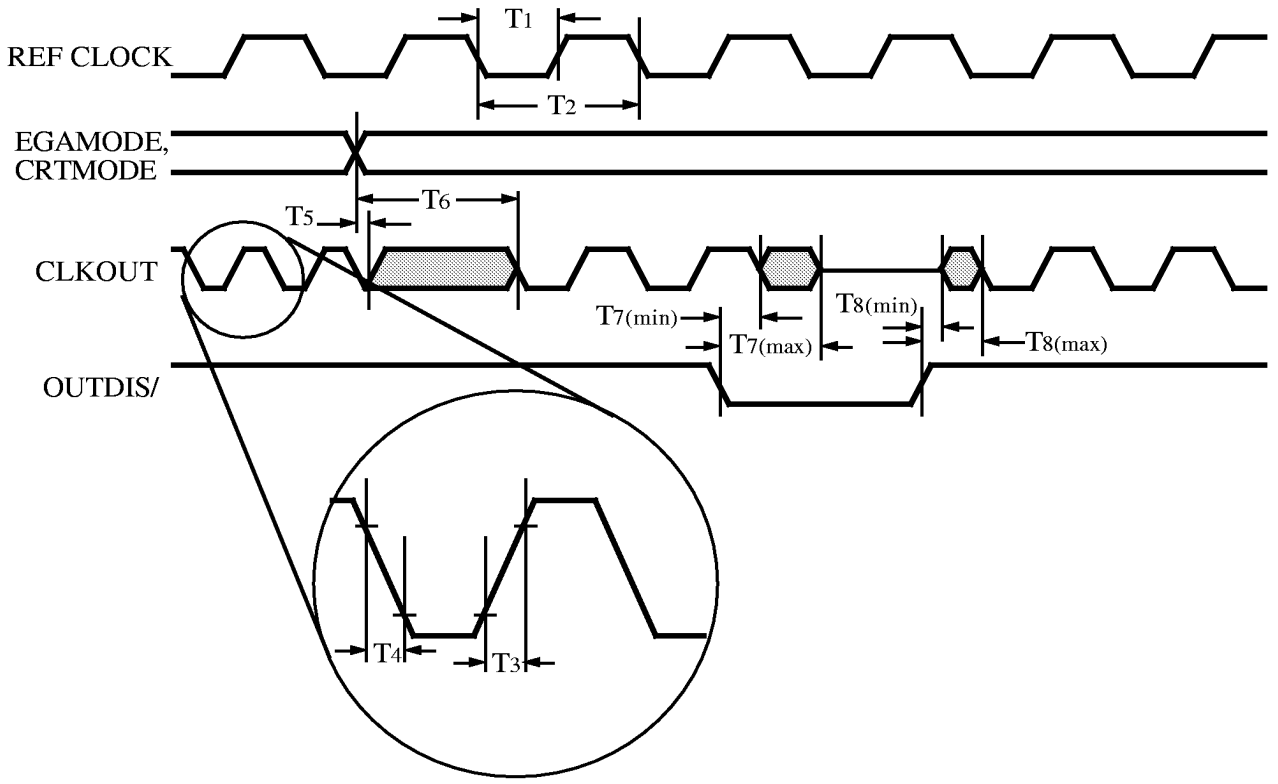
(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC1}	Power Supply (PWRDN)	@ 0°C (PWRDN = 1)		14	mA
I_{CC0}	Power Supply Current (Active)	@ 0°C (PWRDN = 0)	–	35	mA
I_{IL}	Input Low Leakage Current	V_I = 0.4 v	–	-500	µA
I_{IH}	Input High Current	V_I = 4.6 v	–	2.5	µA
I_{OZ}	Output Leakage Current	High Impedance	–	10	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.5	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA (CLKOUT2: 0)	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA (CLKOUT2: 0)	2.8	–	V
C_{IN}	Input Capacitance		–	10	pF
	Bit Jitter	(1σ)	–	±350	ps
	Bit Jitter	Absolute	–	500	ps

Electrical specifications contained herein are preliminary and subject to change without notice.

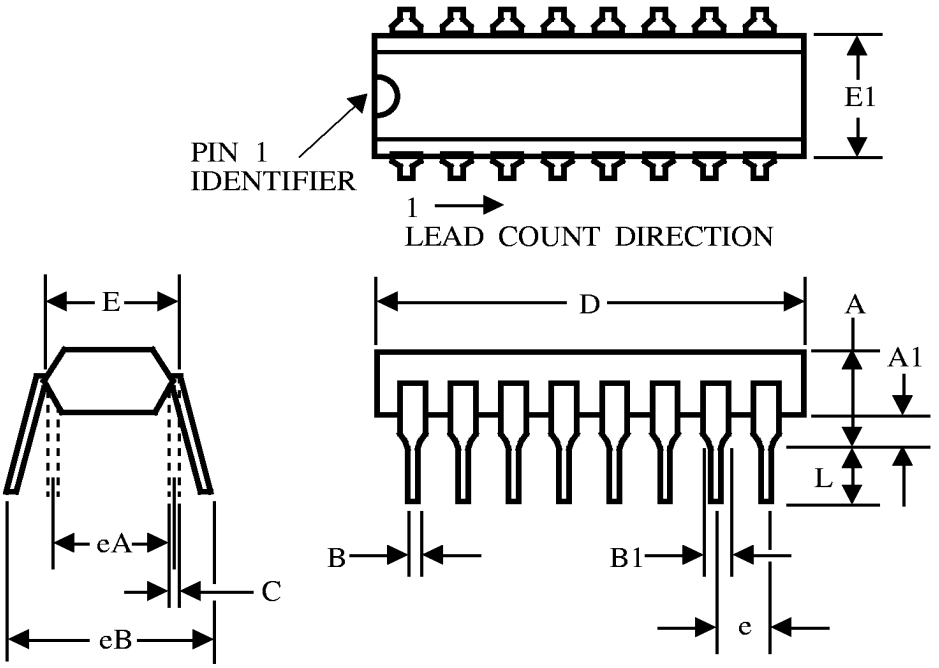
82C401 AC CHARACTERISTICS - Clock Timing

Symbol	Parameter	Notes	Min	Typ	Max	Units
f_{REF}	Reference Frequency	(± 10 ppm)	–	14.31818	–	MHz
T_2	Reference Clock Period		–	69.84128	–	ns
T_1/T_2	Reference Clock Duty Cycle		45	–	55	%
T_3	Output Clock Rise Time		–	–	3	ns
T_4	Output Clock Fall Time		–	–	3	ns
T_5	Frequency Select to Output Unstable		0	–	–	ns
T_6	Frequency Select to Output Stable		–	–	10	ms
T_7	OUTDIS/ Active to Output 3-state		–	–	12	ns
T_8	OUTDIS/ Inactive to Valid Clock Out		–	–	12	ns



82C401A Clock Timing

N82C401A Mechanical Specifications

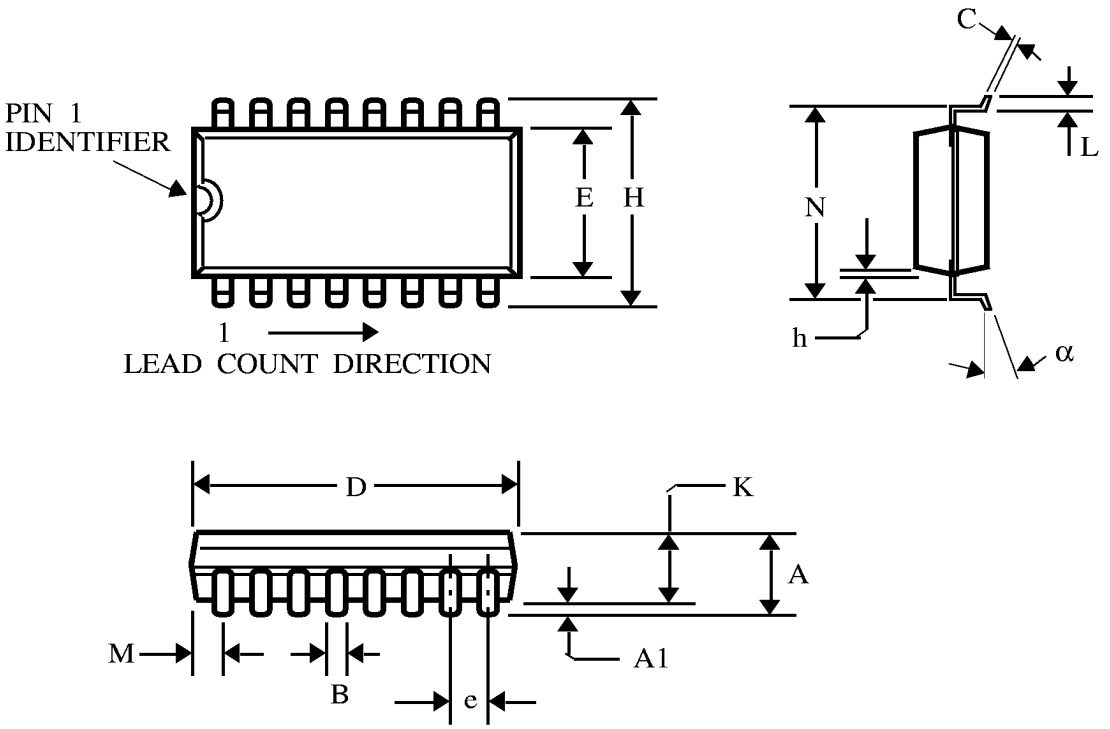


Plastic Dip Package (PDIP)

SYMBOL	LEAD COUNT = 16 MIN	TYP	MAX
A	0.195	–	0.200
A1	0.015	–	–
B	0.015	–	0.020
B1	0.050	–	0.070
C	0.008	–	0.012
D	0.745	–	0.790
E	0.290	–	0.310
E1	0.220	–	0.280
e	–	0.100	–
eA	0.290	–	–
eB	–	–	0.310
L	0.100	–	–

(Dimensions in Inches)

F82C401A Mechanical Specifications



Small Outline IC Package (SOIC)

SYMBOL	LEAD COUNT = 16 MIN	TYP	MAX
A	0.099	–	0.104
A1	0.004	–	0.009
B	0.014	–	0.019
C	0.009	0.010	0.013
D	0.405	–	0.410
E	0.294	–	0.299
e	–	0.050	–
H	0.402	–	0.419
h	–	0.025 x 45°	–
L	0.030	–	0.040
α	0 °	–	8 °
K	0.088	–	0.098
M	0.020	–	0.030
N	0.335	–	0.351

(Dimensions in Inches)