

82C54

CMOS Programmable Interval Timer

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- Compatible with all Intel and most other microprocessors
- High-speed, zero-wait-state operation with 10-MHz 8086/88 and 80186/188
- Three independent 16-bit counters
- Handles inputs from DC to 8 MHz
 - 10 MHz for 82C54-2
 - 12.5 MHz for 82C54-12
- Low-power CMOS
 - $I_{CC} = 50 \mu A$ military standby current I_{CC}
- Completely TTL compatible
- Six programmable counter modes
- Binary or BCD counting
- Status read-back command
- Available in 24-pin DIP

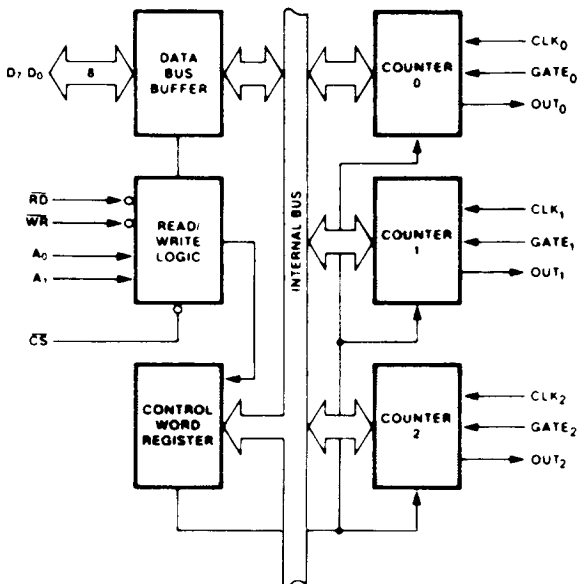
GENERAL DESCRIPTION

The AMD 82C54 is a high-performance, CMOS version of the industry-standard 8254 counter/timer which is designed to solve the timing-control problems common in microcomputer system design. It provides three independent 16-bit Counters — each capable of handling clock inputs up to 12.5 MHz. All modes are software-programmable. The 82C54 is pin-compatible with the NMOS 8254 and is a superset of the 8253.

Six programmable-timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications as well.

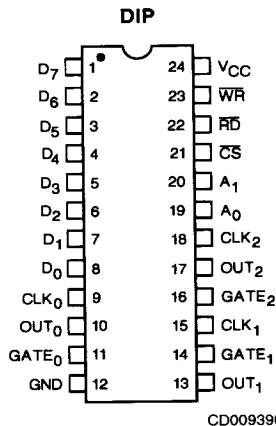
The 82C54 is fabricated with AMD's CMOS technology providing low-power consumption with performance equal to or greater than the equivalent NMOS product. The 82C54 is available in 24-pin DIP package.

BLOCK DIAGRAM



BD006111

CONNECTION DIAGRAM Top View



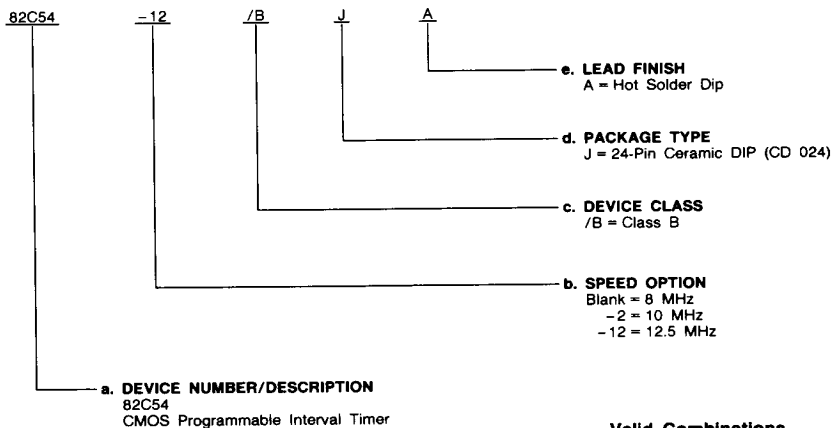
Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
82C54	/BJA
82C54-2	
82C54-12	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C
 Voltage on Any Pin
 with Respect to GND -0.5 to +7.0 V
 Power Dissipation 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
 Temperature (T_C) -55 to +125°C
 Supply Voltage (V_{CC}) 5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V _{IL}	Input LOW Voltage		-0.5*	0.8	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} +0.5 V*	V
V _{OL}	Output LOW Voltage	I _{OL} = 2.0 mA		.45	V
V _{OH}	Output HIGH Voltage	I _{OH} = -400 μA	2.4		V
I _{IL}	Input Load Current	V _{IN} = V _{CC} to 0 V		±10	μA
I _{OFL}	Output Float Leakage Current	V _{OUT} = V _{CC} to 0 V		±10	μA
I _{CC}	Operating Power-Supply Current (Note 1)	CLK Freq = 8 MHz		20	mA
		10 MHz		20	
		12.5 MHz		20	
I _{CCSB}	Standby Power-Supply Current (Note 2)	CLK Freq = DC, CS = HIGH, All Inputs/Data Bus HIGH, All Outputs Floating		±50	μA

CAPACITANCE (T_C = 25°C, V_{CC} = GND = 0 V)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C _{IN} †	Input Capacitance	f _c = 1 MHz Unmeasured pins returned to GND		10*	pF
C _{I/O} †	I/O Capacitance			20*	pF
C _{OUT} †	Output Capacitance			20*	pF

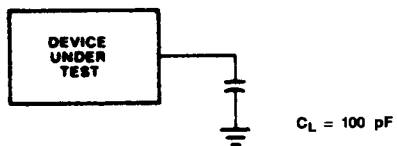
* Guaranteed by design; not tested.

† Not included in Group A tests.

Notes: 1. I_{CC} is measured in a dynamic condition with no output loads applied and inputs at rail levels.

2. Standby I_{CC} is measured in a static condition (CLK = DC) with no output loads applied, and CS and all inputs/databus at the V_{CC} rail level.

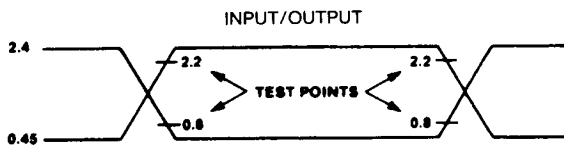
SWITCHING TEST CIRCUIT



TC003431

 $C_L = 100 \text{ pF}$ C_L includes jig capacitance

SWITCHING TEST WAVEFORM



WF021041

A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.2 V for a logic "1" and 0.8 V for a logic "0."

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 1).

No.	Parameter Symbol	Parameter Description	8 MHz		10 MHz		12.5 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
1	tAR	Address Stable Before $\overline{RD} \downarrow$	45		30		25		ns
2	tSR	$\overline{CS}$ Stable Before $\overline{RD} \downarrow$	0		0		0		ns
3	tRA	Address Hold Time After $\overline{RD} \uparrow$	0		0		0		ns
4	tRR	$\overline{RD}$ Pulse Width	150		95		90		ns
5	tRD	Data Delay from $\overline{RD} \downarrow$		120		85		80	ns
6	tAD	Data Delay from Address		220		185		150	ns
7	tDF	$\overline{RD} \uparrow$ to Data Floating	5	90	5	65	5	55	ns
8	tRV	Command Recovery Time	200		165		135		ns
WRITE CYCLE									
9	tAW	Address Stable Before $\overline{WR} \downarrow$	0		0		0		ns
10	tSW	$\overline{CS}$ Stable Before $\overline{WR} \downarrow$	0		0		0		ns
11	tWA	Address Hold Time After $\overline{WR} \uparrow$	0		0		0		ns
12	tWW	$\overline{WR}$ Pulse Width			95		80		ns
13	tDW	Data Setup Time Before $\overline{WR} \uparrow$			95		80		ns
14	tWD	Data Hold Time After $\overline{WR} \uparrow$	0		0		0		ns
15	tRV	Command Recovery Time	200		165		135		ns
CLOCK AND GATE CYCLE									
16	tCLK	Clock Period	125	DC	100	DC	80	DC	ns
17	tpWH	HIGH Pulse Width (Note 3)	60		30		30		ns
18	tpWL	LOW Pulse Width (Note 3)	60		50		40		ns
19	tR	Clock Rise Time (Note 4)		25		25		25	ns
20	tF	Clock Fall Time (Note 4)		25		25		25	ns
21	tGW	Gate Width HIGH	50		50		40		ns
22	tGL	Gate Width LOW	50		50		40		ns
23	tGS	Gate Setup Time to CLK $\uparrow$	50		40		30		ns
24	tGH	Gate Hold Time After CLK $\uparrow$ (Note 2)	50		50		40		ns
25	tOD	Output Delay from CLK $\downarrow$		150		100		80	ns
26	tODG	Output Delay from Gate $\downarrow$		120		100		80	ns
27	tWC	CLK Delay for Loading	0	55	0	55	0	45	ns
28	tWG	Gate Delay for Sampling	-5	50	-5	40	-5	35	ns
29	tWO	Out Delay from Mode Write		260		240		200	ns
30	tCL	CLK Set Up for Count Latch	-4	45	-4	40	-4	35	ns

Notes: 1. Timings measured at $V_{OH} = 2.2$ V, $V_{OL} = 0.8$ V, $C_L = 100$ pF ± 20 pF.

2. In Modes 1 and 5, triggers are sampled on each rising clock edge. A second trigger within 120 ns (70 ns for the 82C54-2) of the rising clock edge may not be detected.

3. LOW-going glitches that violate tp_{WH} , tp_{WL} may cause errors requiring Counter re-programming.

4. Clock rise and fall times are tested at 5 ns, guaranteed by Teradyne J941 test equipment.