

32K-bit TTL bipolar PROM (4096 x 8)

82HS321A

FEATURES

- Address access time:
 - 82HS321A: 45ns max
- Input loading: -250µA max
- Two chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are High level
- Fully TTL compatible
- Outputs: 3-State
- For slower speed options see SMD 82008

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

DESCRIPTION

The 82HS321 is field programmable, which means that custom patterns are immediately available by following the Philips Semiconductors Generic II fusing procedure. The 82HS321 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

ORDERING INFORMATION

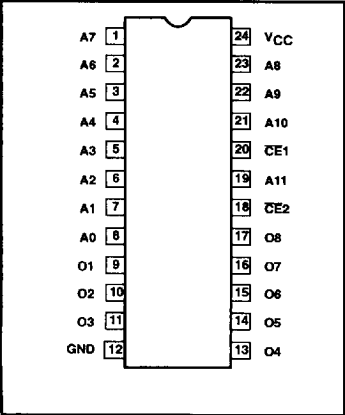
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-pin Ceramic DIP (600 mil-wide)	82HS321A/BJA	GDIP1-T24
24-pin Ceramic FlatPack	82HS321A/BKA	GDFP2-F24
28-pin Ceramic LLCC	82HS321A/B3A	CQCC2-N28

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

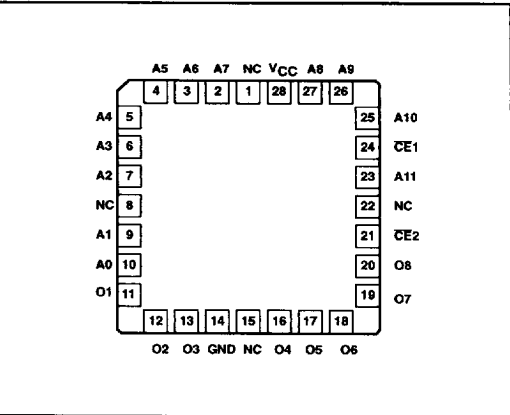
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	+7	V
V _I	Input voltage	+5.5	V
V _O	Output voltage Off-State	+5.5	V
T _{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



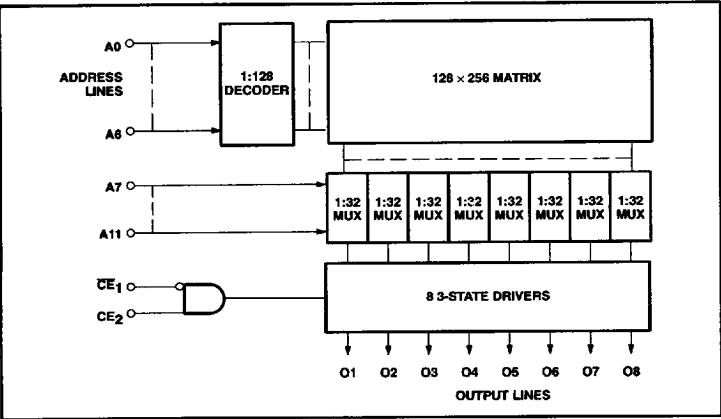
LLCC LEAD CONFIGURATION



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BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATINGS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH} ³	High level input voltage	2.0			V
V _{IL} ³	Low level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High level output current			-2	mA
I _{OL}	Low level output current			16	mA
T _{amb}	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

-55°C < T_{amb} < +125°C, 4.5V < V_{CC} < 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
			MIN	TYP ⁵	MAX	
V _{IK}	Input Clamp voltage	V _{CC} = MIN, I _I = I _{IK}		-0.8	-1.2	V
V _{OL}	Output Low level current	V _{CC} = MIN, I _{OL} = MAX, CE ₁ = Low, CE ₂ = High			0.5	V
V _{OH}	Output High level current	V _{CC} = MIN, CE ₁ = Low, CE ₂ = High, I _{OH} = MAX	2.4			V
I _{IL}	Input Low level current	V _{CC} = MAX, V _I = 0.4V			-250	µA
I _{IH}	Input High level current	V _{CC} = MAX, V _I = 5.5V			40	µA
I _{OLZ}	Off-State output current Low	V _{CC} = MAX, CE ₁ = High, CE ₂ = Low, V _O = 0.4V			-40	µA
I _{OHZ}	Off-State output current High	V _{CC} = MAX, CE ₁ = High, CE ₂ = Low, V _O = 5.5V			40	µA
I _{OS}	Short circuit ⁴	V _{CC} = MAX, CE ₁ = Low, CE ₂ = High, V _O = 0V with stored "1"	-20		-85	mA
I _{CC}	Supply current	V _{CC} = MAX, CE ₁ = High, CE ₂ = Low		130	185	mA
C _{IN}	Input Capacitance ⁷	CE ₁ = High, CE ₂ = Low, V _{CC} = Nom, V _I = 2.0V		5	10	pF
C _{OUT}	Output Capacitance ⁷	CE ₁ = High, CE ₂ = Low, V _{CC} = Nom, V _O = 2.0V		8	13	pF

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AC ELECTRICAL CHARACTERISTICS

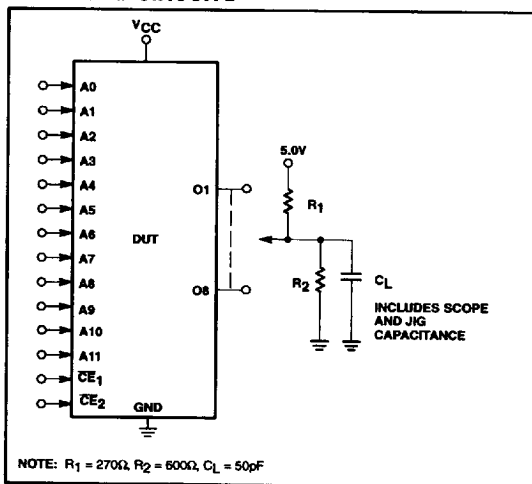
 $-55^{\circ}\text{C} < T_{\text{amb}} < +125^{\circ}\text{C}$, $4.5\text{V} < V_{\text{CC}} < 5.5\text{V}$

SYMBOL	PARAMETER	TO	FROM	82HS321A			UNIT
				MIN	TYP ⁵	MAX	
t_{AA}	Access time ⁶	Output	Address		25	30	ns
t_{CE}	Access time ⁶	Output	Chip enable		15	20	ns
t_{CD}	Disable time	Output	Chip disable		15	20	ns

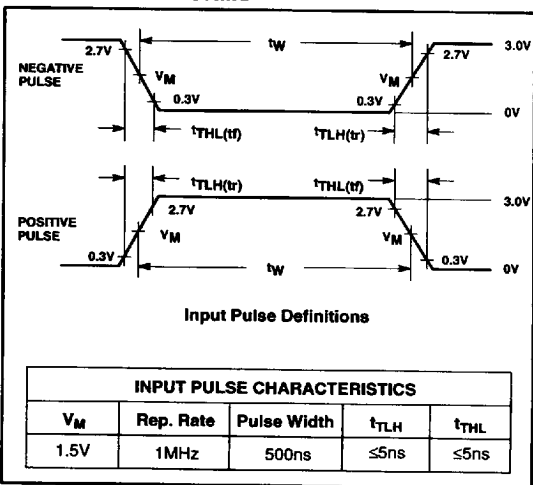
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from Logic "1" to a Logic "0". These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{\text{CC}} = 5\text{V}$, $T_{\text{amb}} = +25^{\circ}\text{C}$.
6. Tested at an address cycle time of $1\mu\text{s}$.
7. Guaranteed, but not tested.

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



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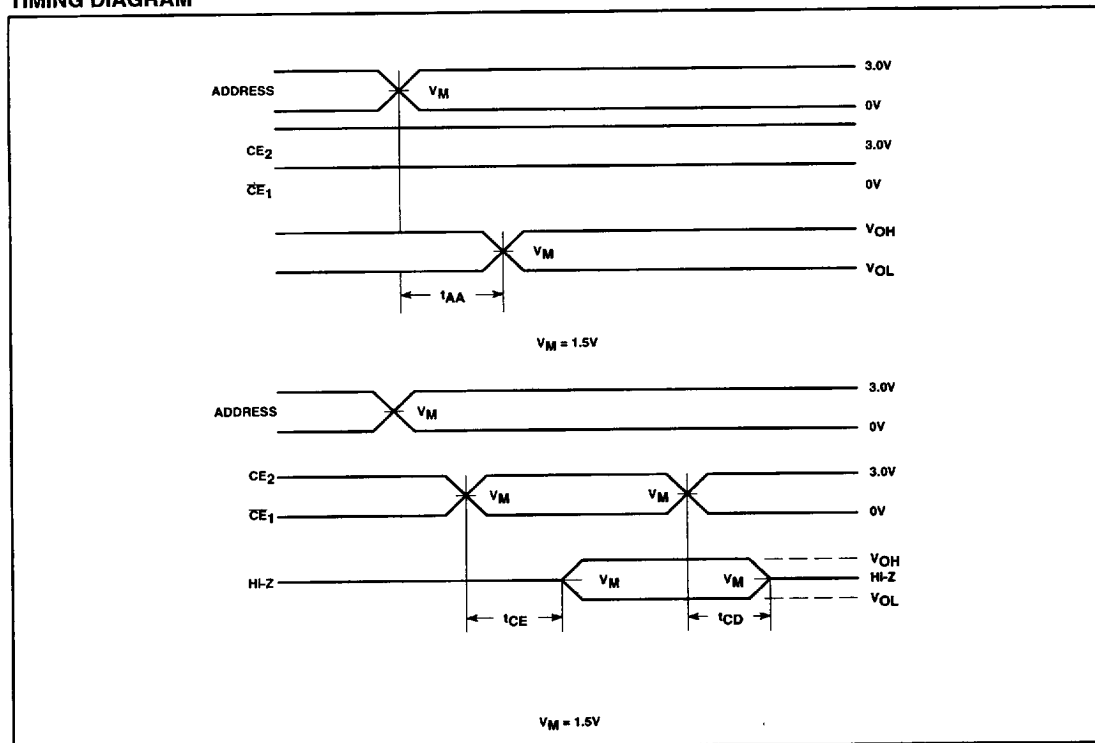
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TIMING DIAGRAM



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