Philips Components–Signetics

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Status	Product Specification
Memory Products	

82S115

4K-bit TTL bipolar PROM

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the 3-State output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines.

In the Latched Read mode, outputs are held in their previous state (High, Low, or Hi-Z) as long as Strobe is Low, regardless of the state of Address or Chip Enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the Hi-Z State if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

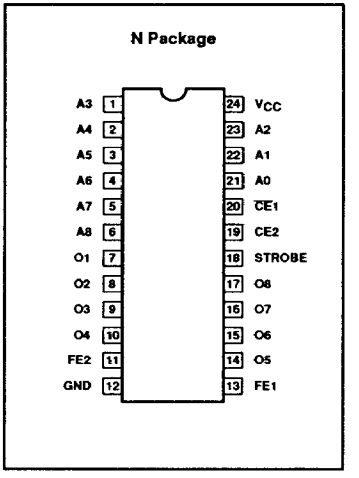
FEATURES

- Address access time: 60ns max
- Power dissipation: 165µA max
- Input loading: –100µA max
- Two Chip Enable inputs
- On-chip storage latches
- Schottky clamped
- Fully TTL compatible
- Outputs: 3-State

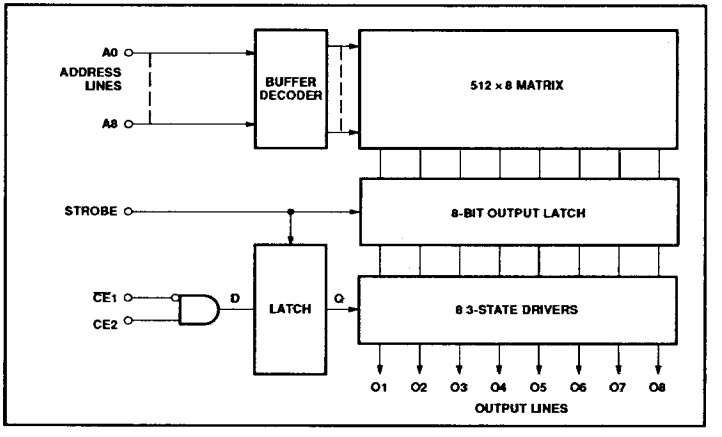
APPLICATIONS

- Microprogramming
- Hardware algorithms
- Character generation
- Control store
- Sequential controllers

PIN CONFIGURATION



BLOCK DIAGRAM



4K-bit TTL bipolar PROM (512 × 8) — 82S115

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 600mil-wide	N82S115 N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	I_{IN} = -12mA		-0.8	-1.2	V
Output voltage						
		$\overline{CE}1$ = Low, CE2 = High				
V_{OL}	Low	I_{OUT} = 9.6mA		0.4	0.45	V
V_{OH}	High	I_{OUT} = -2.0mA	2.7			V
Input current[1]						
I_{IL}	Low	V_{IN} = 0.45V			-100	μA
I_{IH}	High	V_{IN} = 5.5V			25	μA
Output current[1]						
I_{OZ}	Hi-Z state	$\overline{CE}1$ = High or CE2 = Low, V_{OUT} = 5.5V			40	μA
		$\overline{CE}1$ = High or CE2 = Low, V_{OUT} = 0.5V			-40	μA
I_{OS}	Short circuit[3]	$\overline{CE}1$ = Low or CE2 = High, V_{OUT} = 0V, High stored	-15		-70	mA
Supply current[4]						
I_{CC}		V_{CC} = 5.25V		130	175	mA
Capacitance						
		$\overline{CE}1$ = High or CE2 = Low, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5V, T_{amb} = +25°C.
3. No more than one output should be grounded at the same time and Strobe should be disabled. Strobe is in the High state.
4. Measured with all inputs grounded and all outputs open.

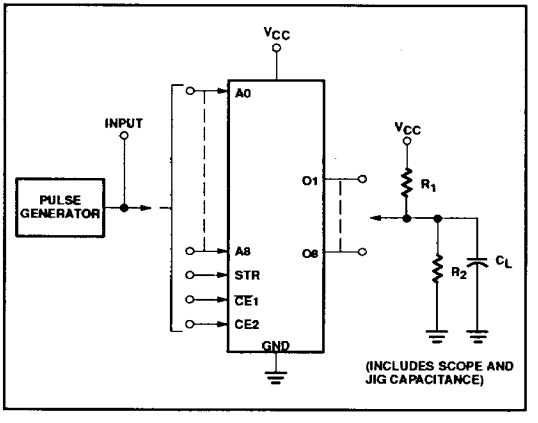
AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

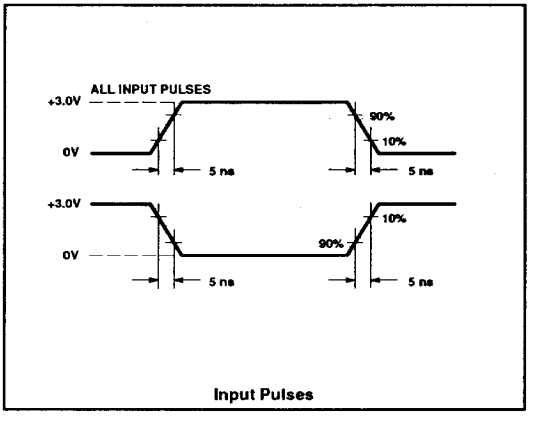
SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
Access time[1]								
t_{AA}		Output	Address	Latched or transparent read[3,4]		45	60	ns
t_{CE}		Output	Chip Enable			25	40	ns
Disable time[6]								
t_{CD}		Output	Chip Disable	Latched or transparent read[3,4]		25	40	ns
Setup and hold time								
t_{CDS}	Setup time	Output	Chip Enable	Latched read only[4,5]	40			ns
t_{CDH}	Hold time	Output	Chip Enable	Latched read only[4,5]	10			ns
Hold time								
t_{ADH}	Hold time	Address	Strobe	Latched read only[4,5]		0		ns
Pulse width								
t_{SW}	Strobe			Latched read only[4,5]	30	15		ns
Latch time								
t_{SL}	Strobe			Latched read only[4,5]	60	35		ns
Delatch time[6]								
t_{DL}	Strobe			Latched read only[4,5]			35	ns

NOTES:
1. Tested at an address cycle time of 1µs.
2. Typical values are $V_{CC} = 5V$, $T_{amb} = +25°C$.
3. If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear t_{AA} nanoseconds after the address has changed or t_{CE} nanoseconds after the output circuit is enabled.
4. During operation the fusing pins FE1 and FE2 must be grounded or left floating.
5. In latched Read Mode data from any selected address will be held on the output when Strobe is lowered. Only when Strobe is raised will new location data be transferred and Chip Enable conditions be stored. The new data will appear on the outputs if the Chip Enable conditions enable the outputs.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

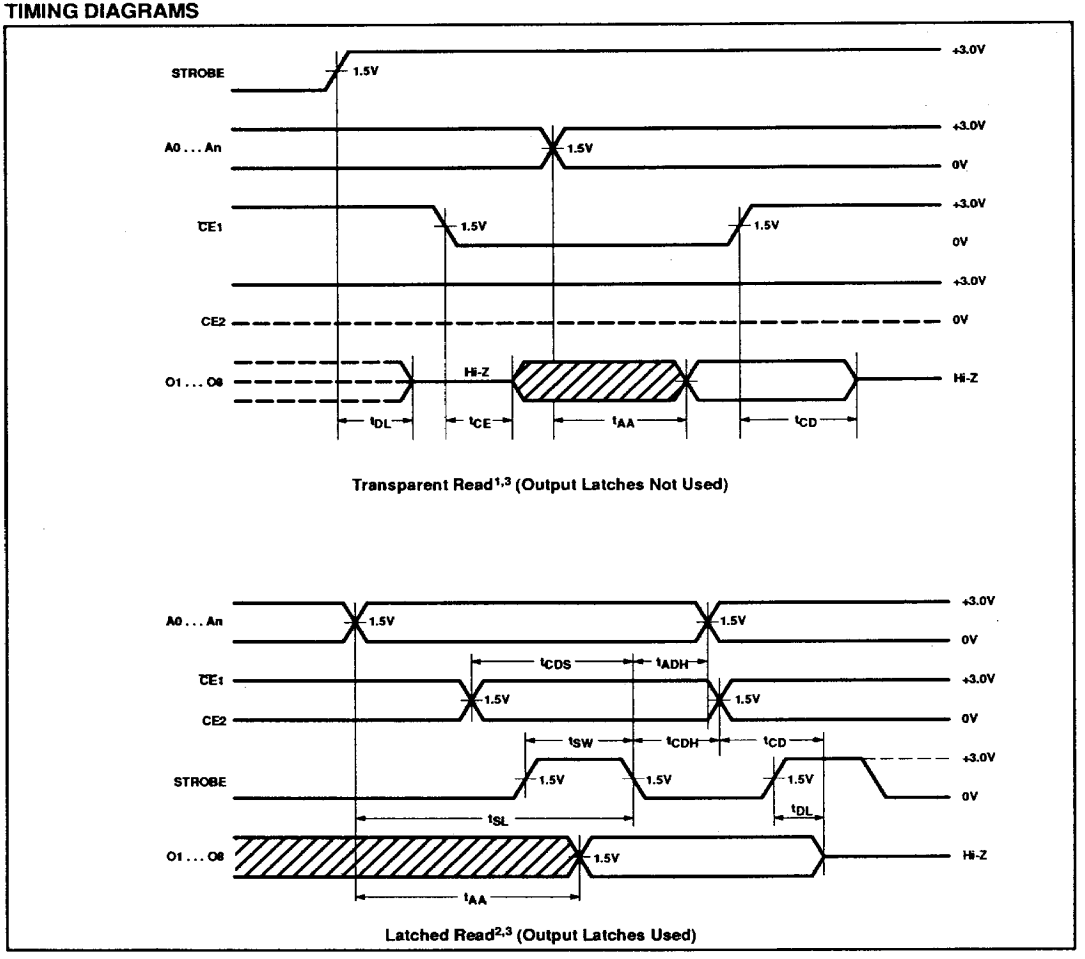
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAMS



Transparent Read[1,3] (Output Latches Not Used)

Latched Read[2,3] (Output Latches Used)

NOTES:

1. If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear t_{AA} nanoseconds after the address has changed or t_{CE} nanoseconds after the output circuit is enabled.
2. In Latched Read Mode data from any selected address will be held on the output when Strobe is lowered. Only when Strobe is raised will new location data be transferred and Chip Enable conditions be stored. The new data will appear on the outputs if the Chip Enable conditions enable the outputs.
3. Areas shown by crosshatch are latched data from prevous address.