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Memory Products	

82LS135

2K-bit TTL bipolar PROM

DESCRIPTION

The 82LS135 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82LS135 includes on-chip decoding and two Chip Enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

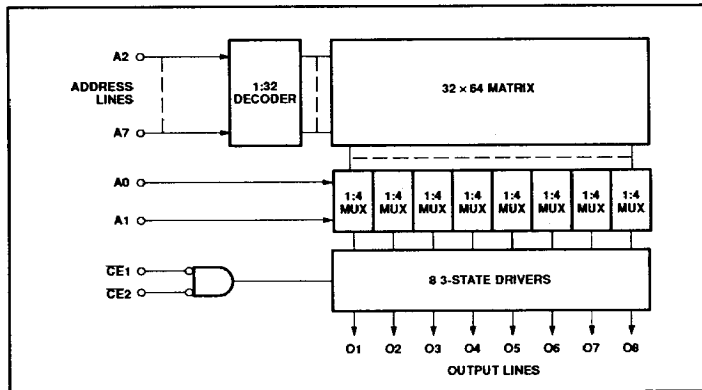
FEATURES

- Address access time: 100ns max
- Power dissipation: 200μW/bit typ
- Input loading: -100μA max
- Two Chip Enable inputs
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Unprogrammed outputs are Low level
- Outputs: 3-State

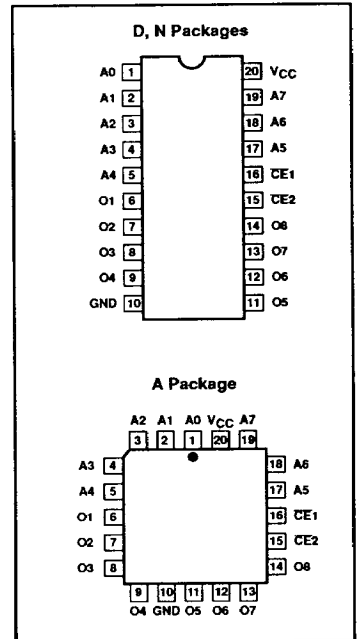
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATIONS



2K-bit TTL bipolar PROM (256 × 8)**82LS135****ORDERING INFORMATION**

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual-In-Line 300mil-wide	N82LS135 N
20-Pin Plastic Small Outline 300mil-wide	N82LS135 D
20-Pin Plastic Leaded Chip Carrier 350mil-square	N82LS135 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
			Min	Typ ³	Max	
Input voltage						
V _{IL} V _{IH} V _{IC}	Low High Clamp	I _{IN} = -12mA	2.0		0.8 -1.2	V V V
Output voltage						
V _{OL} V _{OH}	Low High	I _{OUT} = 16mA I _{OUT} = -2mA, High stored	2.4		0.5	V V
Input current						
I _{IL} I _{IH}	Low High	V _{IN} = 0.45V V _{IN} = 5.5V			-100 40	μA μA
Output current						
I _{OZ} I _{OS}	Hi-Z state Short circuit ⁴	CE1, CE2 = High, V _{OUT} = 0.5V CE1, CE2 = High, V _{OUT} = 5.5V CE1, CE2 = Low, V _{OUT} = 0V, High stored	 -15		-40 40 -75	μA μA mA
Supply current ⁵						
I _{CC}		V _{CC} = 5.25V		80	100	mA
Capacitance						
C _{IN} C _{OUT}	Input Output	V _{CC} = 5.0V, CE = High V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF pF

NOTES:

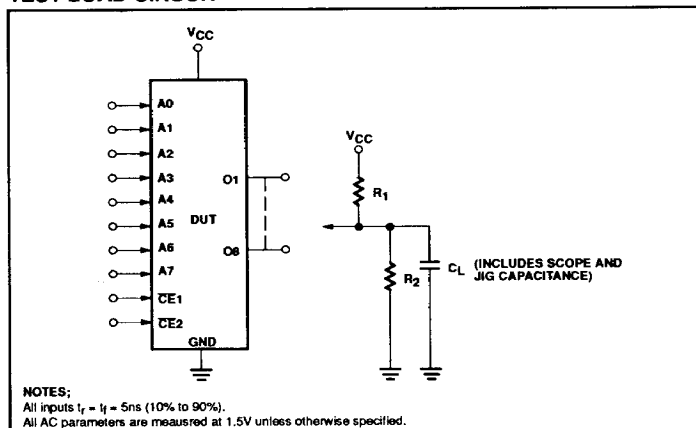
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = +25^\circ\text{C}$.
4. Duration of short circuit should not exceed 1 second.
5. Measured with all inputs grounded and all outputs open.

2K-bit TTL bipolar PROM (256 × 8)**82LS135****AC ELECTRICAL CHARACTERISTICS**
 $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$, $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ ¹	Max	
Access time ²							
t _{AA}		Output	Address		70	100	ns
t _{CE}		Output	Chip Enable		30	50	ns
Disable time ³							
t _{CD}		Output	Chip Disable		30	60	ns

NOTES:

- Typical values are at $V_{\text{CC}} = 5\text{V}$, $T_{\text{amb}} = +25^\circ\text{C}$.
- Tested at an address cycle time of $1\mu\text{s}$.
- Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5\text{pF}$.

TEST LOAD CIRCUIT**VOLTAGE WAVEFORMS**