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Memory Products	

# 82S212

## 82S212A

### 2304-bit TTL bipolar RAM

#### DESCRIPTION

The organization of the 82S212 and 82S212A allow byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212 and 82S212A are ideal for scratch pads, push down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

Data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of Read/Write operations using a common bus.

Ordering information can be found on the following page.

The 82S212 and 82S212A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

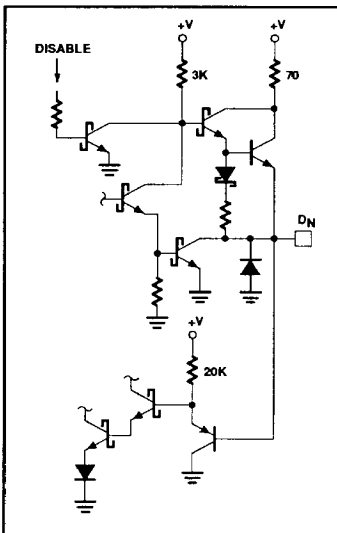
#### FEATURES

- Address access time:
  - N82S212: 45ns max
  - N82S212A: 35ns max
- Power dissipation: 0.3mW/bit typ
- Schottky clamped TTL
- One Chip Enable input
- Common I/O
  - Inputs: PNP Buffered
  - Outputs: 3-State

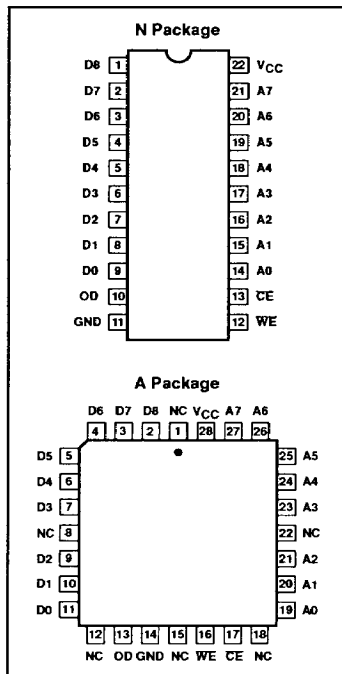
#### APPLICATIONS

- Cache memory
- Buffer storage
- Writable control store

#### TYPICAL I/O STRUCTURE



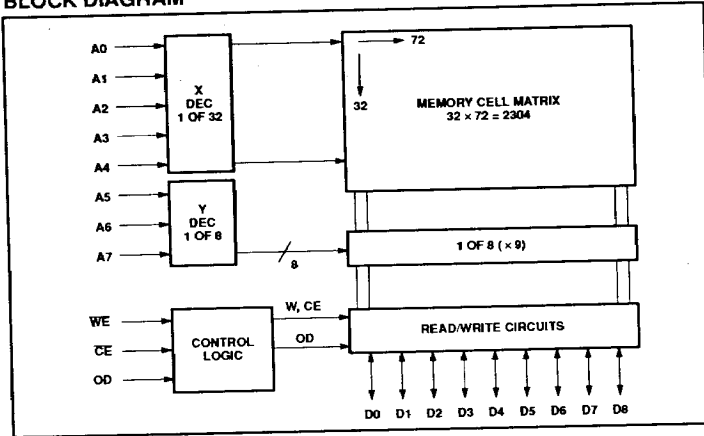
#### PIN CONFIGURATIONS



# 2304-bit TTL bipolar RAM (256 × 9)

82S212 / 82S212A

## BLOCK DIAGRAM



## ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-Pin Plastic Dual-In-Line 400mil-wide	N82S212 N, N82S212A N
28-Pin Plastic Leaded Chip Carrier 450mil-square	N82S212 A, N82S212A A

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	+7.0	$V_{DC}$
$V_{IN}$	Input voltage	+5.5	$V_{DC}$
$V_{OH}$	Output voltage High	+5.5	$V_{DC}$
$T_{amb}$	Operating temperature range	0 to +75	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

**2304-bit TTL bipolar RAM (256 × 9)****82S212 / 82S212A****DC ELECTRICAL CHARACTERISTICS**0°C ≤ T<sub>amb</sub> ≤ +75°C, 4.75V ≤ V<sub>CC</sub> ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP <sup>1</sup>	MAX		
Input voltage <sup>2</sup>							
V <sub>IL</sub>	Low	V <sub>CC</sub> = 4.75V	2.0		0.8	V	
V <sub>IH</sub>	High	V <sub>CC</sub> = 5.25V			V		
V <sub>IC</sub>	Clamp <sup>3</sup>	V <sub>CC</sub> = 4.75V, I <sub>IN</sub> = -12mA			-1.5	V	
Output voltage <sup>2</sup>							
V <sub>OH</sub>	High	I <sub>OL</sub> = -2mA	2.4		0.5	V	
V <sub>OL</sub>	Low <sup>3</sup>	V <sub>CC</sub> = 4.75V, I <sub>OL</sub> = 8.0mA				V	
Input current							
I <sub>IL</sub>	Low	V <sub>IN</sub> = 0.45V			-100	μA	
I <sub>IH</sub>	High	V <sub>IN</sub> = 5.5V			25	μA	
Output current							
I <sub>OZ</sub>	Hi-Z State	CE = High or OD = High, V <sub>OUT</sub> = 5.5V	-15		40	μA	
I <sub>OS</sub>	Short circuit <sup>3, 4</sup>	CE = High or OD = High, V <sub>OUT</sub> = 0.5V			-100	μA	
		CE = OD = Low, V <sub>OUT</sub> = 0V			-70	mA	
Supply current <sup>5</sup>							
I <sub>CC</sub>		V <sub>CC</sub> = 5.25V		135	185	mA	
Capacitance							
C <sub>IN</sub>	Input	V <sub>CC</sub> = 5.0V		5		pF	
C <sub>OUT</sub>	Output	V <sub>IN</sub> = 2.0V				8	pF
		V <sub>OUT</sub> = 2.0V					

**NOTES:**

1. All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Measured on one pin at a time.
4. Duration of I<sub>OS</sub> test should not exceed one second.
5. I<sub>CC</sub> is measured with the Write Enable and Memory Enable inputs grounded, all other inputs at 0.45V, and the outputs open.

**TRUTH TABLE**

MODE	WE	CE	OD	D <sub>N</sub> IN/OUT
Disable output	X	X	1	Hi-Z
Disable R/W	X	1	X	Hi-Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

2304-bit TTL bipolar RAM (256 × 9)

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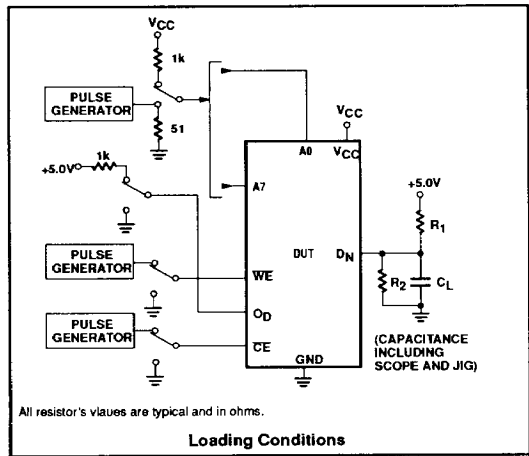
AC ELECTRICAL CHARACTERISTICS

$R_1 = 600\Omega$ ,  $R_2 = 900\Omega$ ,  $C_L = 30\text{pF}$ ,  $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$ ,  $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

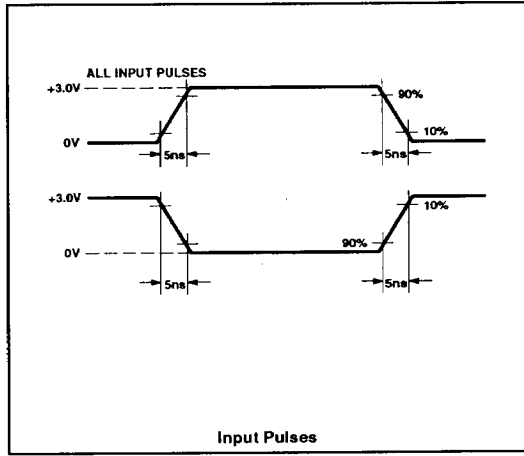
SYMBOL	PARAMETER <sup>1</sup>	TO	FROM	N82S212			N82S212A			UNIT
				MIN	TYP <sup>2</sup>	MAX	MIN	TYP <sup>2</sup>	MAX	
Access time										
t <sub>AA</sub>	Address	Output	Address			45			35	ns
Enable time										
t <sub>OD</sub>	Output	Output	OD	5		25			25	ns
t <sub>CE</sub>	Output	Output	Chip Enable			25			25	ns
Disable time <sup>3</sup>										
t <sub>OD</sub>	Output	Output	OD			25			25	ns
t <sub>CD</sub>	Output	Output	Chip Enable			25			25	ns
Pulse width										
t <sub>WP</sub> <sup>4</sup>	Write			25			25			ns
Setup and hold time										
t <sub>WSC</sub>	Setup time	Write	Chip Enable	5			5			ns
t <sub>WHC</sub>	Hold time	Chip Enable	Write	5			5			ns
t <sub>WSD</sub>	Setup time	Write	Data	25			25			ns
t <sub>WHD</sub>	Hold time	Data	Write	5			5			ns
t <sub>WSA</sub> <sup>5</sup>	Setup time	Write	Address	5			5			ns
t <sub>WHA</sub>	Hold time	Address	Write	5			5			ns
t <sub>SO</sub>	Setup time (from disabled state)	Chip Enable	OD	5			5			ns
t <sub>HO</sub>	Hold time	OD	Chip Enable	5			5			ns

- NOTES:
- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
  - All typical values are at  $V_{\text{CC}} = 5\text{V}$ ,  $T_{\text{amb}} = +25^\circ\text{C}$ .
  - Measured at a delta of 0.5V from Logic level with  $R_1 = 750\Omega$ ,  $R_2 = 750\Omega$  and  $C_L = 5\text{pF}$ .
  - Measured with minimum  $t_{\text{WSA}}$ .
  - Measured with minimum  $t_{\text{WP}}$ .

TEST LOAD CIRCUIT



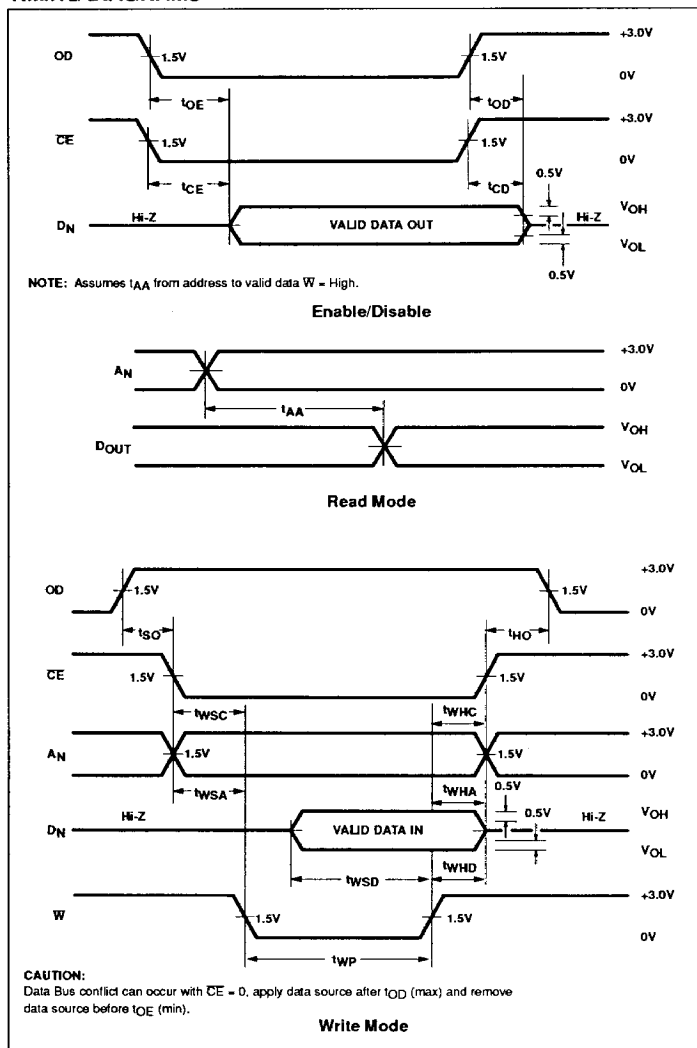
VOLTAGE WAVEFORMS



## 2304-bit TTL bipolar RAM (256 × 9)

## 82S212 / 82S212A

## TIMING DIAGRAMS



## MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
$t_{AA}$	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
$t_{OE}$	Delay between beginning of Output Disable Low (with Address valid) and when Data Output becomes valid.
$t_{CE}$	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
$t_{OD}$	Delay between when Output Disable becomes High and Data Output is in Off-State.
$t_{CD}$	Delay between when Chip Enable becomes High and Data Output is in Off-State.
$t_{WP}$	Width of Write Enable pulse.
$t_{WSC}$	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
$t_{WHD}$	Required delay between end of Write Enable pulse and end of valid input data.
$t_{WSD}$	Required delay between beginning of valid Data Input and end of Write Enable pulse.
$t_{WHD}$	Required delay between end of Write Enable pulse and end of valid input data.
$t_{WSA}$	Required delay between beginning of valid Address and beginning of Write Enable pulse.
$t_{WHA}$	Required delay between end of Write Enable pulse and end of valid Address.
$t_{SO}$	Set-up time between $\overline{OD}$ going High and $\overline{CE}$ going Low.
$t_{HO}$	Hold time for $\overline{OD}$ after $\overline{CE}$ goes High.