G118
Monolithic 6-Channel Enhancement-type MOSFET Switch

FEATURES

- Internal Zener Diode Protects the Gate
- Six Switches Per Chip

BENEFITS

- Reduces External Component Requirements

APPLICATIONS

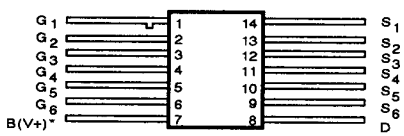
- Switching Analog Signals
- Multiplexing
- Designed to Operate with D125, D129 and D139

DESCRIPTION

The G118 contains six enhancement-mode P-channel MOSFETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak. The switches are integrated on a common substrate (body). They have a common drain terminal (D) which will function equally well as a common source; likewise, the source terminals will function as drains.

PIN CONFIGURATION

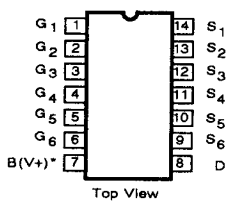
Flat Package



Top View

Order Number: G118AL

Dual-In-Line Package

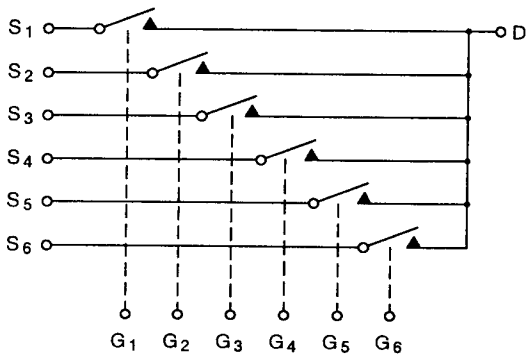


Top View

Order Numbers: G118AP or G118BP

* Common to Substrate and Base of Package

FUNCTIONAL BLOCK DIAGRAM



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Not Recommended for New Designs

ABSOLUTE MAXIMUM RATINGS

V_S to V_B ..... 2 V
V_B to V_S ..... 30 V
V_D to V_B ..... 2 V
V_B to V_D ..... 30 V
V_D to V_S ..... ±30 V
V_S to V_D ..... ±30 V
V_B to V_G ..... 35 V
I_S, I_D ..... 100 mA

I_G ..... 5 mA
Storage Temperature ..... -65 to 150°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C

Power Dissipation*
Flat Package** ..... 750 mW
14-Pin DIP*** ..... 825 mW

* All leads soldered or welded to PC board.
** Derate 10 mW/°C above 75°C.
*** Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_{DB} = 0 V, V_{PB} = 0 V		LIMITS 1=25°C 2=125,85°C 3=-55,-25°C TEMP	LIMITS TYP [d]	A SUFFIX -55 to 125°C MIN [b]	A SUFFIX -55 to 125°C MAX [b]	B SUFFIX -25 to 85°C MIN [b]	B SUFFIX -25 to 85°C MAX [b]	UNIT
STATIC										
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S = -1 mA	V_{DB} = 0 V, V_{GD} = -30 V	1,3			100		125	Ω
				2			125		150	
			V_{DB} = -10 V, V_{GD} = -20 V	1,3			200		250	
				2			250		300	
			V_{DB} = -20 V, V_{GD} = -10 V	1,3			450		500	
				2			600		600	
Source OFF Leakage Current	$I_{S(OFF)}$	V_{SD} = -20 V, V_{GD} = 0 V		1		-0.5		-0.5		nA
				2		-500		-500		
Drain OFF Leakage Current	$I_{D(OFF)}$	V_{DS} = -20 V, V_{GD} = 0 V, V_{SB} = 0 V		1		-3		-10		
				2		-3000		-1000		
Gate-Channel Leakage Current	I_{GSS}	V_{GB} = -20 V		1		-0.5		-5		
				2		-500		-500		
Gate-Source Threshold Voltage	$V_{GS(th)}$	I_D = -10 µA, V_{DG} = 0 V, V_{SB} = 0 V		1,2,3		-4	-1.5	-4	-1.5	V
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = -50 µA, V_{GS} = 0 V, V_{SB} = 0 V		1,2,3			-30		-30	
Source-Drain Breakdown Voltage	$V_{(BR)SDS}$	I_S = -10 µA, V_{GD} = 0 V		1,2,3			-30		-30	
Gate-Body Breakdown Voltage	$V_{(BR)GBS}$	I_G = -10 µA		1,2,3		-90	-35	-90	-35	
DYNAMIC										
Gate-Source Capacitance	C_{gs}	V_{GB} = 0 V, f = 1 MHz, V_{DB} = V_{SB} = 0, Body Guarded	Drain Guarded	1	0.9					pF
Gate-Drain Capacitance	C_{gd}		Source Guarded	1	0.9					
Drain-Source OFF Capacitance	$C_{ds(off)}$		Gate Guarded	1	0.4					

Not Recommended for New Designs

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_{DB} = 0 V, V_{PB} = 0 V	LIMITS 1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
DYNAMIC (Cont'd)									
Source-Body Capacitance	C_{sb}	V_{DB} = 0, V_{SB} = -5 V Drain and Gate Guarded	1	2.0					pF
Drain-Body Capacitance	C_{db}	V_{SB} = 0, V_{DB} = -5V Gate and Source Guarded	1	12					pF

NOTES:

a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

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