Global Mixed-mode Technology Inc. **G1421**

2W Stereo Audio Amplifier With No Headphone Coupling Capacitor Function

Features

- **Depop Circuitry Integrated**
- **Output Power at 1% THD+N, VDD=5V**
  --1.8W/CH (typical) into a 4Ω Load
  --1.2W/CH (typical) into a 8Ω Load
- **Eliminates Headphone Amplifier Output Coupling Capacitors**
- **Maximum Output Power Clamping Circuitry Integrated**
- **Bridge-Tied Load (BTL), Single-Ended (SE), and Stereo Headphone Amplifier (HP-IN) modes Supported**
- **Stereo Input MUX**
- **Mute and Shutdown Control Available**
- **Surface-Mount Power Package**
  24-Pin TSSOP-P

Applications

- **Stereo Power Amplifiers for Notebooks or Desktop Computers**
- **Multimedia Monitors**
- **Stereo Power Amplifiers for Portable Audio Systems**

General Description

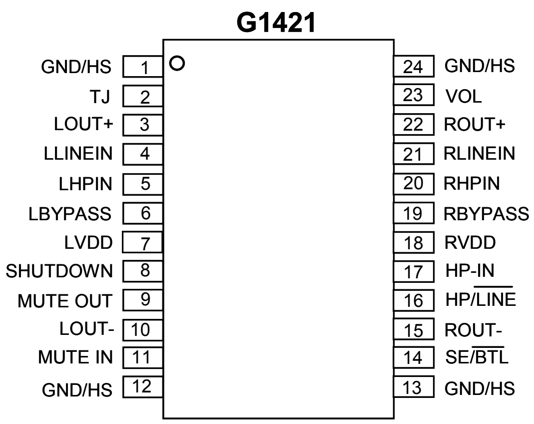
G1421 is a stereo audio power amplifier in 24pin TSSOP thermal pad package. It can drive 1.8W continuous RMS power into 4Ω load per channel in Bridge-Tied Load (BTL) mode at 5V supply voltage. Its THD is smaller than 1% under the above operation condition. To simplify the audio system design in the notebook application, G1421 supports the Bridge-Tied Load (BTL) mode for driving the speakers, Single-End (SE) mode for driving the headphone. In the HP-IN mode, it can support a DC value to the phone-jacket and drive the headphone without the audio amplifier outputs coupling capacitors. G1421 can mute the output when Mute-In is activated. For the low current consumption applications, the SHDN mode is supported to disable G1421 when it is idle. The current consumption can be further reduced to below 5μA.

G1421 also supports two input paths, that means two different gain loops can be set in the same PCB and choosing either one by setting HP/$\overline{\text{LINE}}$ pin. It enhances the hardware designing flexibility. G1421 also supports an extra function -- the maximum output power clamping function to protect the speakers or headphones from burned-out.

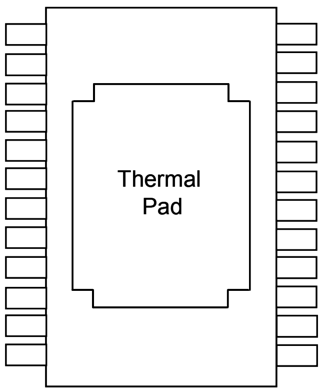
Ordering Information

ORDER NUMBER	TEMP. RANGE	PACKAGE
G1421	-40°C to +85°C	TSSOP-24L

Pin Configuration



Top View
TSSOP-24L



Bottom View

Absolute Maximum Ratings

Supply Voltage, V_{CC}……………………………………6V
Operating Ambient Temperature Range
T_A……………………………………-40°C to +85°C
Maximum Junction Temperature, T_J……………150°C
Storage Temperature Range, T_{STG}….-65°C to+150°C
Soldering Temperature, 10seconds, T_S…………..260°C

Power Dissipation (1)
$T_A \le 25°C$……………………………………2.7W
$T_A \le 70°C$……………………………………1.7W
$T_A \le 85°C$……………………………………1.4W
Electrostatic Discharge, V_{ESD}
Human body mode
Lout- pin……………………………-8000 to 8000V
Other pins…………………………...-3000 to 3000(2)

Note:
(1) : Recommended PCB Layout.
(2) : Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses

Electrical Characteristics

DC Electrical Characteristics, T_A=+25°C

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Supply Current	I_{DD}	V_{DD} =3.3V	HP-IN		5.5	7	mA
		V_{DD} = 5V	HP-IN		6.5	8	
		V_{DD} =3.3V	Stereo BTL		7	9	
			Stereo SE		3.5	5.6	
		V_{DD} = 5V	Stereo BTL		8	11	
			Stereo SE		4	6.5	
DC Differential Output Voltage	$V_{O(DIFF)}$	V_{DD} = 5V,Gain = 2			5	30	mV
Supply Current in Mute Mode	$I_{DD(MUTE)}$	V_{DD} = 5V	Stereo BTL		8	11	mA
			HP-IN		6.5	8	
			Stereo SE		4	6.5	
I_{DD} in Shutdown	I_{SD}	V_{DD} = 5V			2	5	µA

(AC Operation Characteristics, V_{DD} = 5.0V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω		1.8		W
		THD = 1%, BTL, R_L = 8Ω		1.12		
		THD = 10%, BTL, R_L = 4Ω		2		
		THD = 10%, BTL, R_L = 8Ω		1.4		
		THD = 1%, SE, R_L = 4Ω		500		mW
		THD = 1%, SE, R_L = 8Ω		320		
		THD = 10%, SE, R_L = 4Ω		650		
		THD = 10%, SE, R_L L = 8Ω		400		
		THD = 0.5%, SE, R_L = 32Ω		90		
Total harmonic distortion plus noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω		500		m%
		P_O = 1W, BTL, R_L = 8Ω		150		
		P_O = 75mW, SE, R_L = 32Ω		20		
		V_I = 1V, RL = 10KΩ, G = 1		10		
Maximum output power bandwidth	B_{OM}	G = 1, THD =1%		20		kHz
Phase margin		R_L = 4Ω, Open Load		60		°
Power supply ripple rejection	PSRR	f = 120Hz		75		dB
Mute attenuation				85		dB
Channel-to-channel output separation		f = 1kHz		82		dB
Line/HP input separation				80		dB
BTL attenuation in SE mode				85		dB
Input impedance	ZI			2		MΩ
Signal-to-noise ratio		P_O = 500mW, BTL		90		dB
Output noise voltage	V_n	Output noise voltage		55		µV (rms)

Note :Output power is measured at the output terminals of the IC at 1kHz.

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(AC Operation Characteristics, V_{DD} = 3.3V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω		0.8		W
		THD = 1%, BTL, R_L = 8Ω		0.5		
		THD = 10%, BTL, R_L = 4Ω		1		
		THD = 10%, BTL, R_L = 8Ω		0.6		
		THD = 1%, SE, R_L = 4Ω		230		mW
		THD = 1%, SE, R_L = 8Ω		140		
		THD = 10%, SE, R_L = 4Ω		290		
		THD = 10%, SE, R_L L = 8Ω		180		
		THD = 0.5%, SE, R_L = 32Ω		43		
Total harmonic distortion plus noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω		270		m%
		P_O = 1W, BTL, R_L = 8Ω		100		
		P_O = 75mW, SE, R_L = 32Ω		20		
		V_I = 1V, RL = 10KΩ, G = 1		10		
Maximum output power bandwidth	B_{OM}	G = 1, THD 1%		20		kHz
Phase margin		R_L = 4Ω, Open Load		60		°
Power supply ripple rejection	PSRR	f = 120Hz		75		dB
Mute attenuation				85		dB
Channel-to-channel output separation		f = 1kHz		80		dB
Line/HP input separation				80		dB
BTL attenuation in SE mode				85		dB
Input impedance	ZI			2		MΩ
Signal-to-noise ratio		P_O = 500mW, BTL		90		dB
Output noise voltage	V_n	Output noise voltage		55		μV (rms)

Note :Output power is measured at the output terminals of the IC at 1kHz.

Pin Description

PIN	NAME	I/O	FUNCTION
1,12,13,24	GND/HS		Ground connection for circuitry, directly connected to thermal pad.
2	TJ	O	Source a current inversely to the junction temperature. This pin should be left unconnected during normal operation. For more information, see the junction temperature measurement section of this document.
3	LOUT+	O	Left channel + output in BTL mode, + output in SE mode.
4	LLINE IN	I	Left channel line input, selected when HP/ pin is held low.
5	LHP IN	I	Left channel headphone input, selected when HP/pin is held high.
6	LBYPASS		Connect to voltage divider for left channel internal mid-supply bias.
7	LVDD	I	Supply voltage input for left channel and for primary bias circuits.
8	SHUTDOWN	I	Shutdown mode control signal input, places entire IC in shutdown mode when held high, I_{DD} = 5μA.
9	MUTE OUT	O	Follows MUTE IN pin, provides buffered output.
10	LOUT-	O	Left channel - output in BTL mode, high impedance state in SE mode. Supply VDD/2 to the phone jacket in HP-IN mode.
11	MUTE IN	I	Mute control signal input, hold low for normal operation, hold high to mute.
14	SE/	I	Mode control signal input, hold low for BTL mode, hold high for SE mode.
15	ROUT-	O	Right channel - output in BTL mode, high impedance state in SE mode.
16	HP/	I	MUX control input, hold high to select headphone inputs (5,20), hold low to select line inputs (4,21).
17	HP-IN		This pin can activate the HP-IN mode to supplied the VDD/2 at LOUT- onto the phone jacket. So the DC blocking capacitors can be removed in HP-IN type (like SE mode except no DC blocking capacitors). Hold high to activate this function. If this function is not used, it should be strongly tied to low.
18	RVDD	I	Supply voltage input for right channel.
19	RBYPASS		Connect to voltage divider for right channel internal mid-supply bias.
20	RHP IN	I	Right channel headphone input, selected when HP/pin is held high.
21	RLINE IN	I	Right channel line input, selected when HP/pin is held low.
22	ROUT+	O	Right channel + output in BTL mode, + output in SE mode.
23	VOL	I	The output power can be clamped by setting a low bound voltage to this pin. The high bound voltage will be generated internally. The output voltage will be clamped between high/low bound voltages. Then the output power is limited. It is weakly pull-low internally, let this pin floating or tied to GND can deactivate this function.

Typical Characteristics

Table of Graphs

		FIGURE
THD +N Total harmonic distortion plus noise	vs Frequency	2,4,5,7,8,11,12,14,15,17,18,20,21,23,24,28,29,30 31,32,34,35,37,38,40,41
	vs Output power	1,3,6,9,10,13,16,19,22,25,26,27,33,36,39
V_n Output noise voltage	vs Frequency	42,43,44
Supply ripple rejection ratio	vs Frequency	45,46,47
Crosstalk	vs Frequency	48,49,50,51,52
Closed loop response	vs Frequency	53,54,55,56
I_{DD} Supply current	vs supply voltage	57
P_O Output power	vs supply voltage	58,59
	vs Load resistance	60,61
P_D Power dissipation	vs Output power	62,63,64,65

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

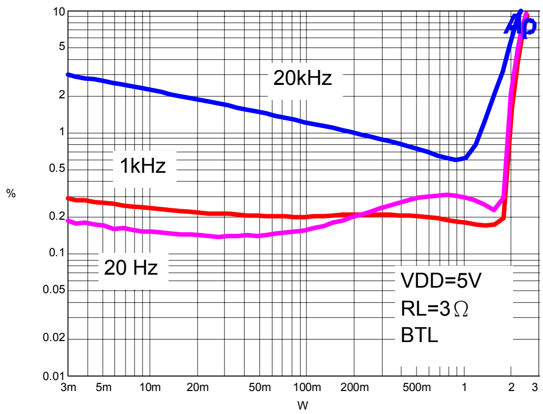

Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

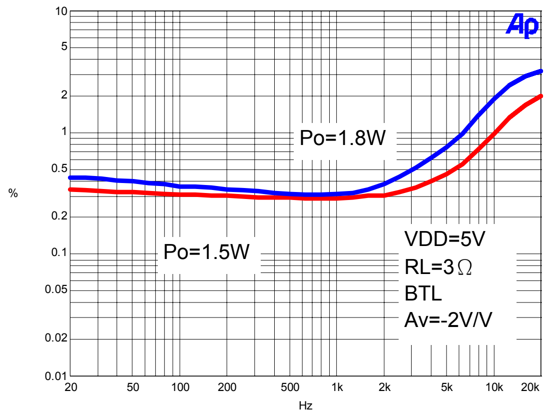

Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

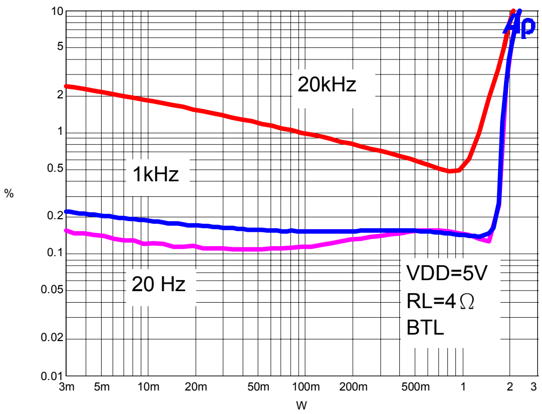

Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

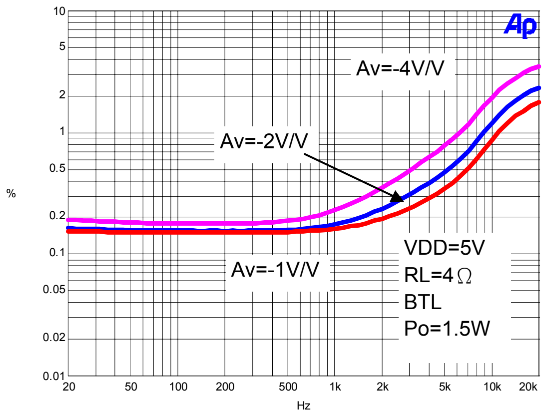

Figure 4

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

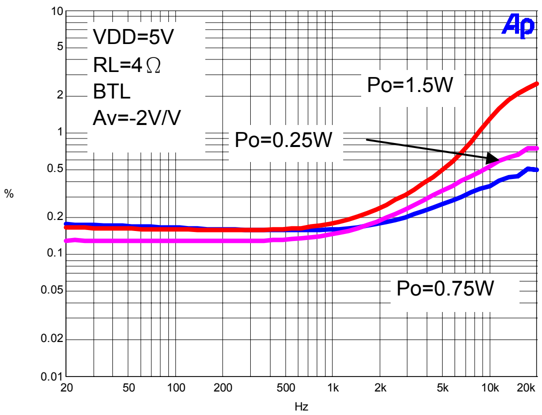

Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

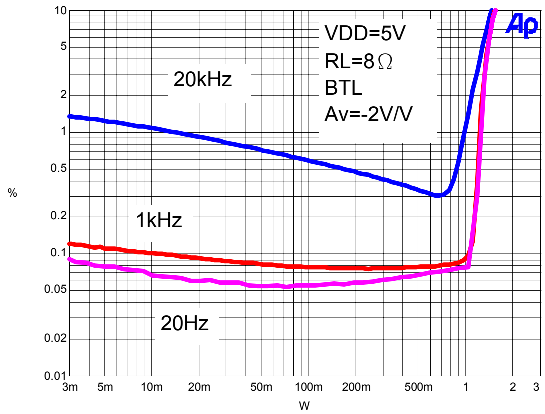

Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

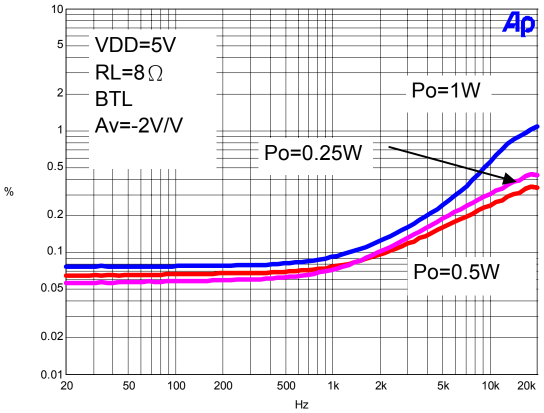

Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

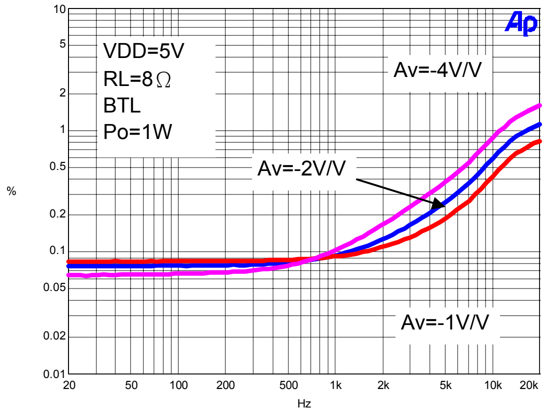

Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

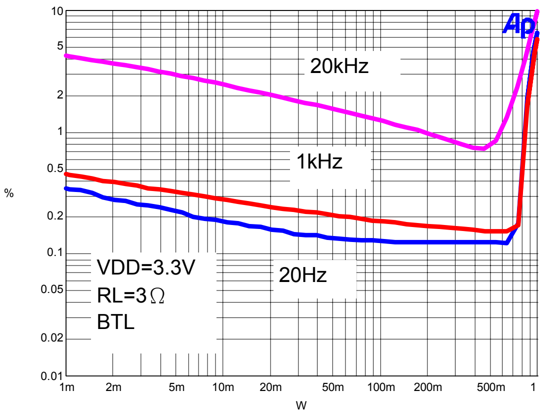

Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

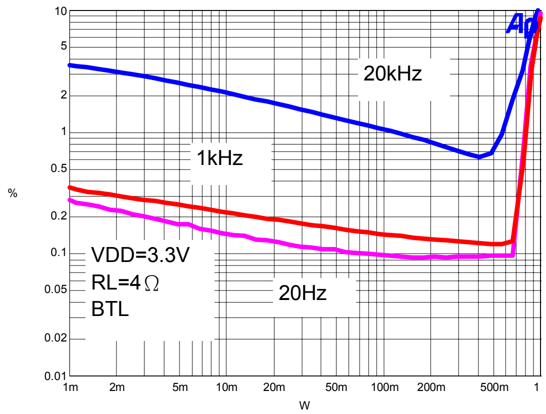

Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

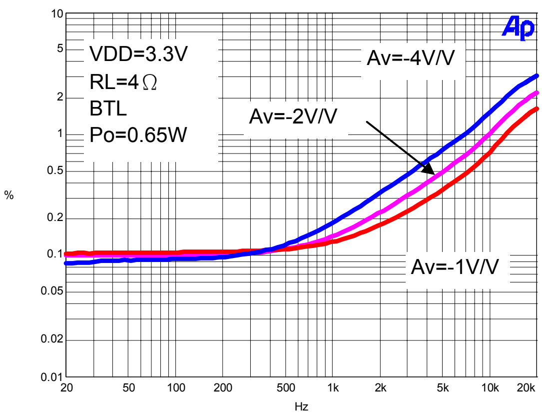

Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

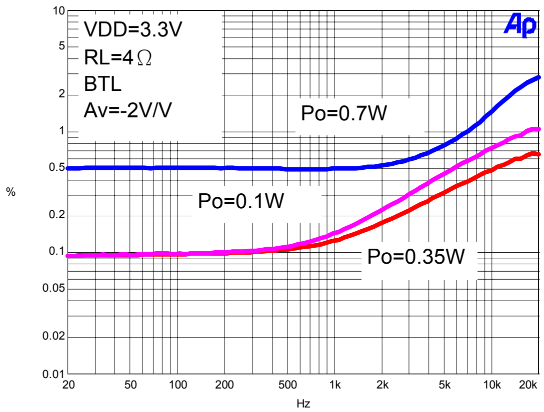

Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

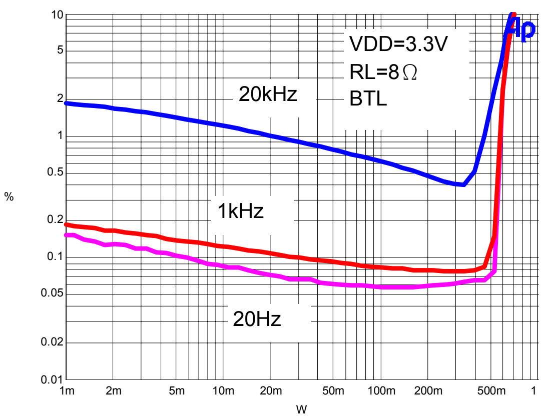

Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

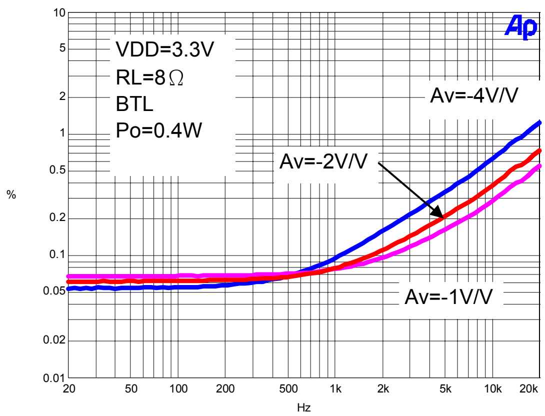

Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

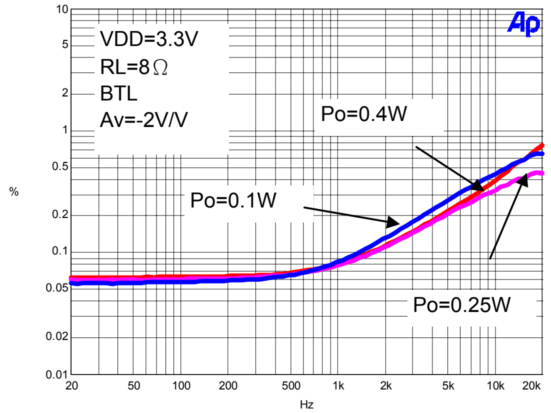

Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

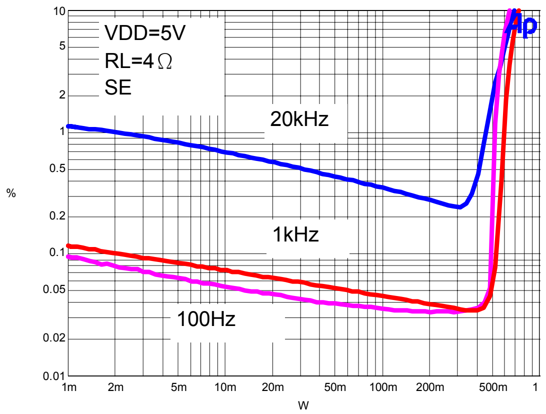

Figure 16

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

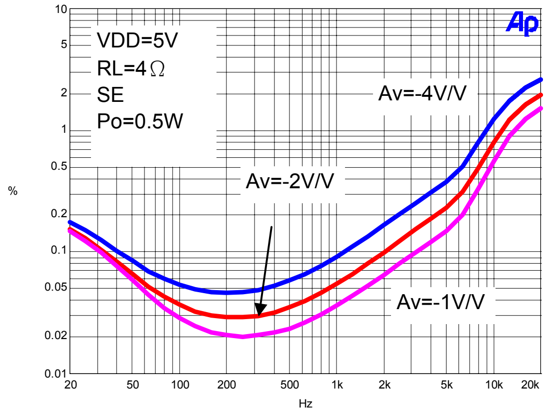

Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

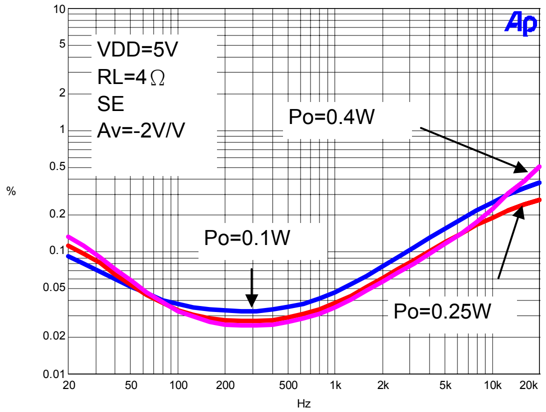

Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

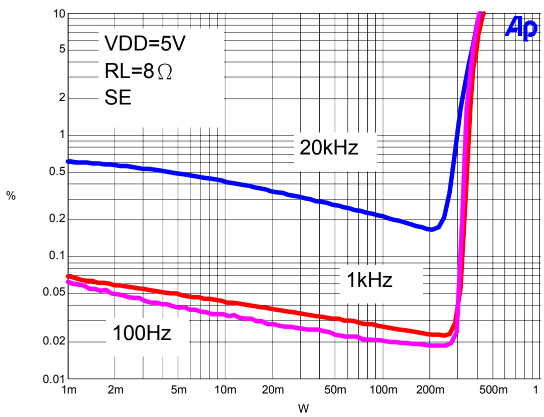

Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

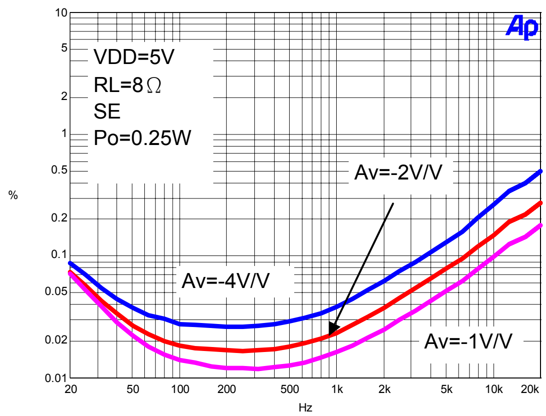

Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

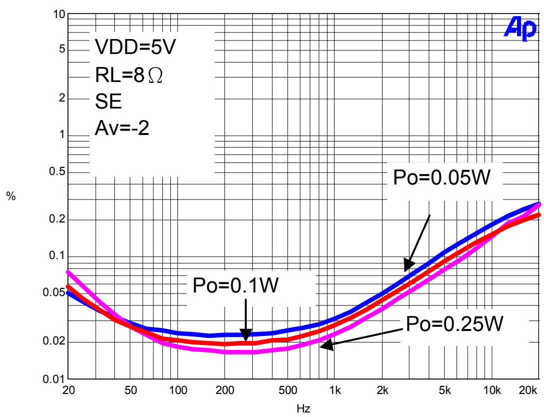

Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

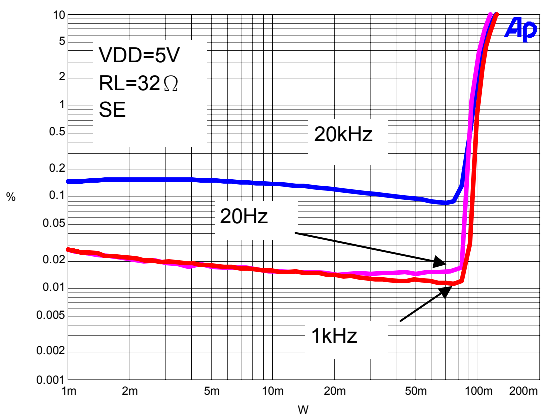

Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

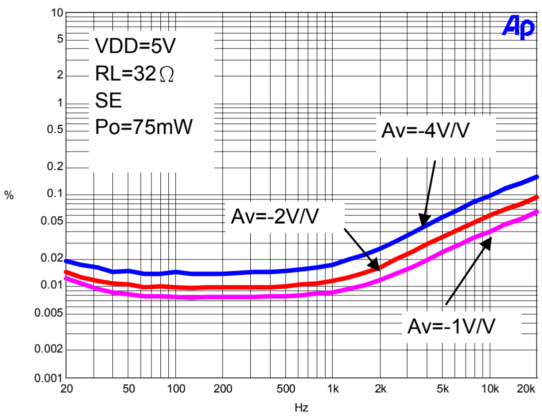

Figure 23

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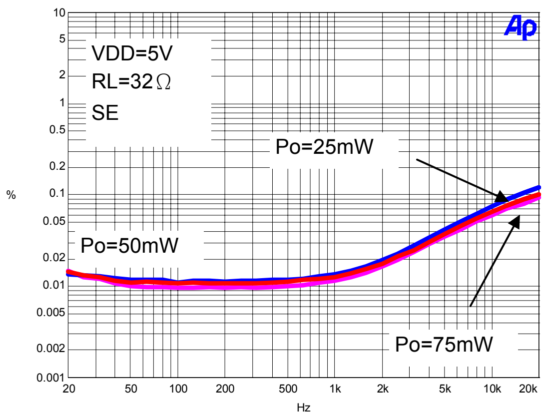

Figure 24

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

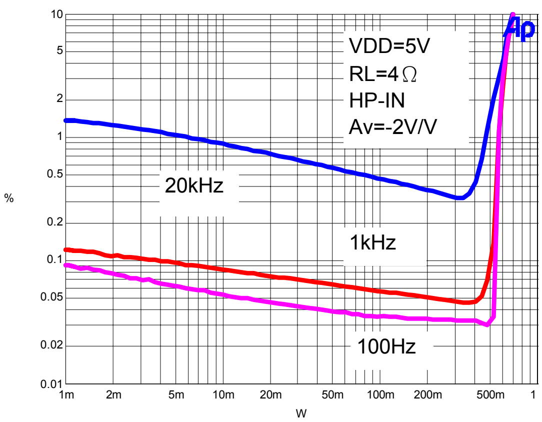

Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

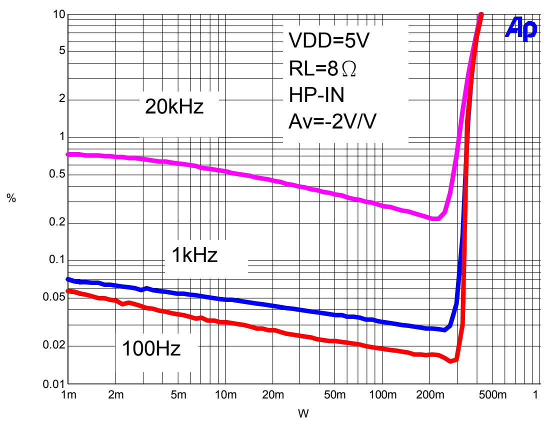

Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

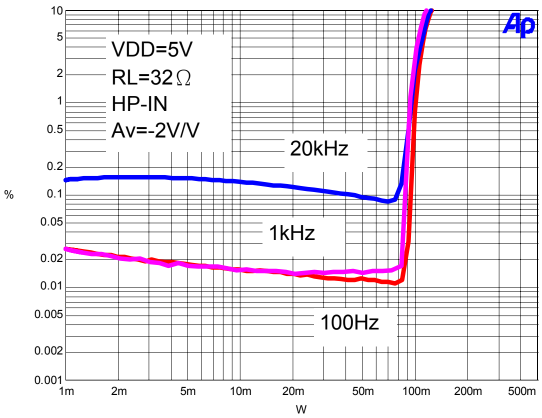

Figure 27

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

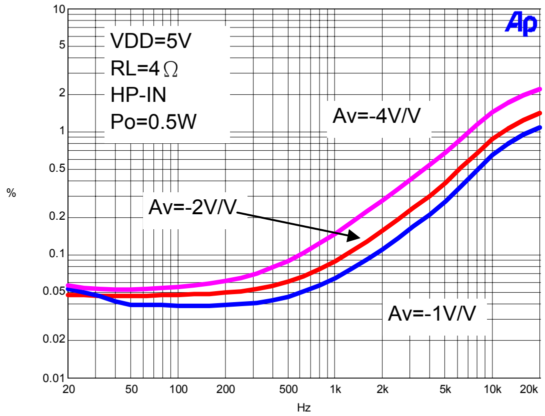

Figure 28

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

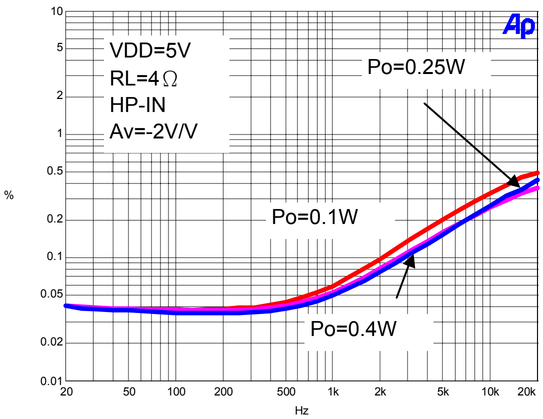

Figure 29

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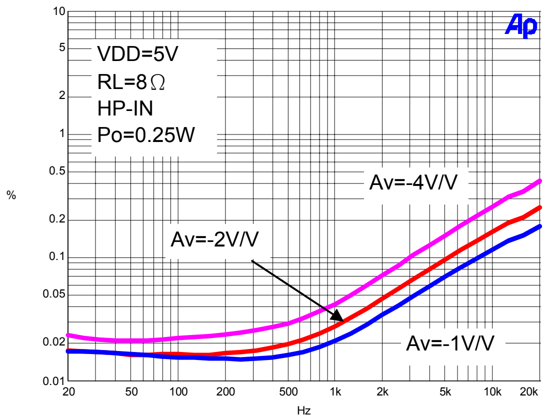


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

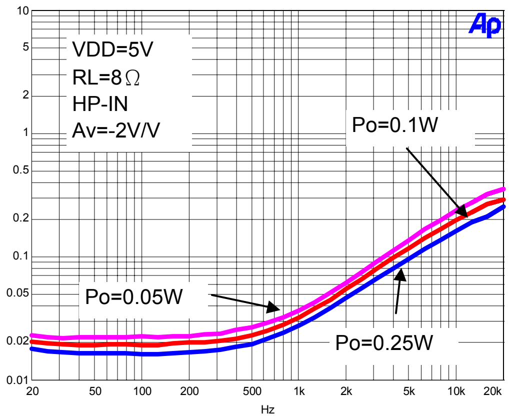


Figure 31

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

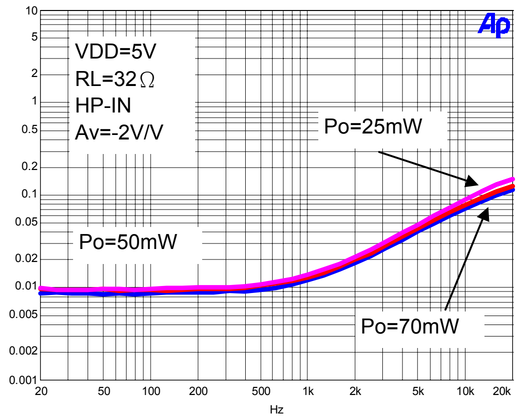


Figure 32

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

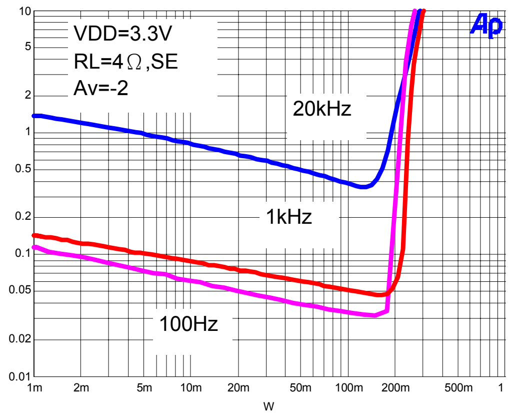


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

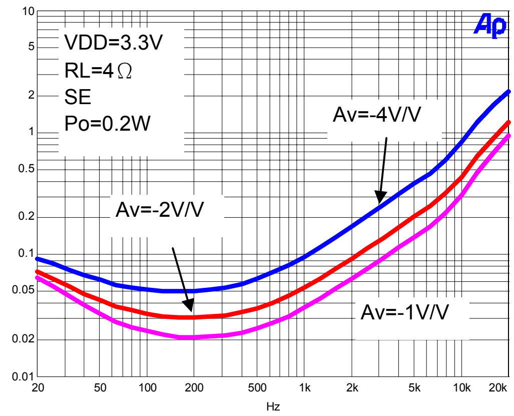


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

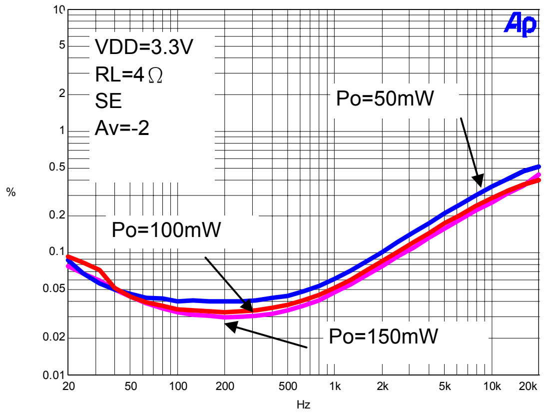


Figure 35

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

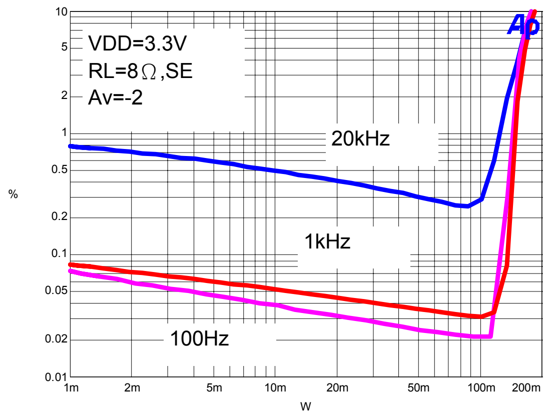


Figure 36

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

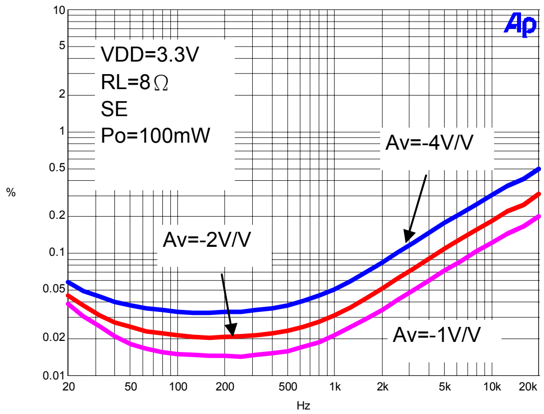


Figure 37

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

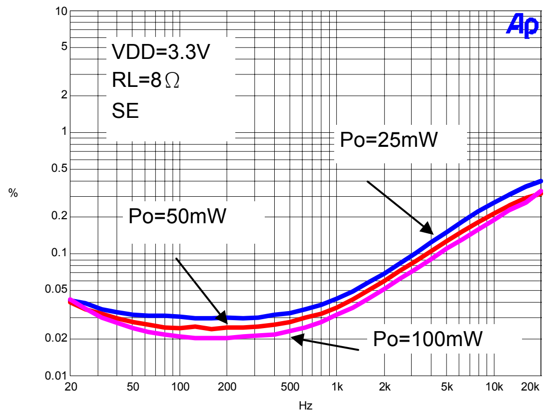


Figure 38

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

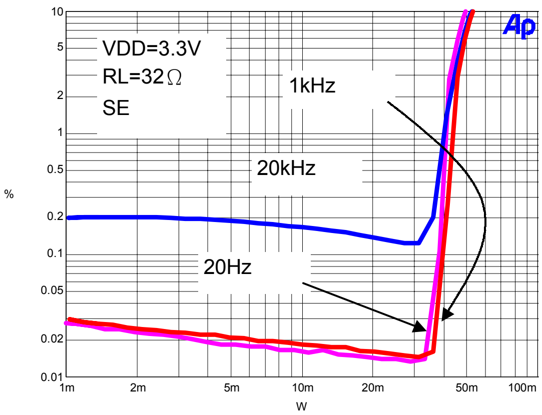


Figure 39

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

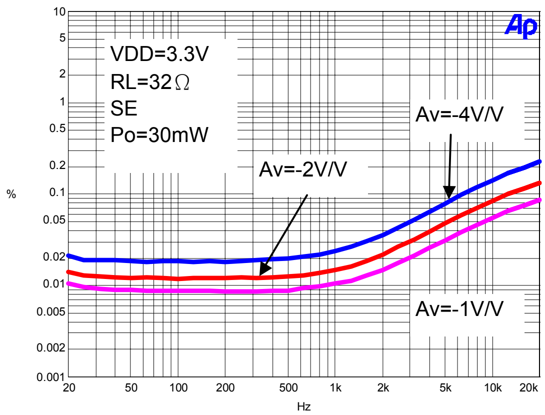


Figure 40

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

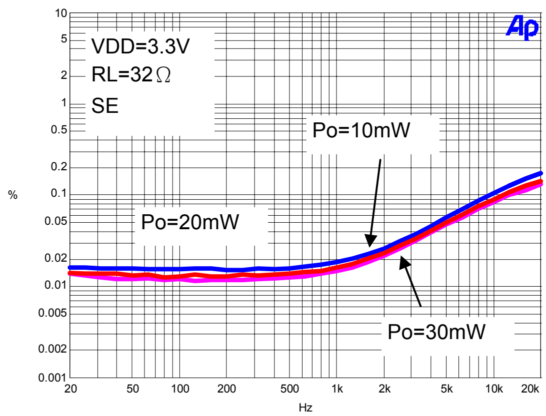


Figure 41

OUTPUT NOISE VOLTAGE vs FREQUENCY

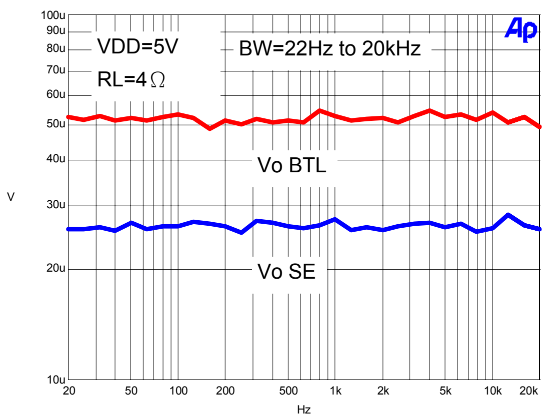


Figure 42

OUTPUT NOISE VOLTAGE vs FREQUENCY

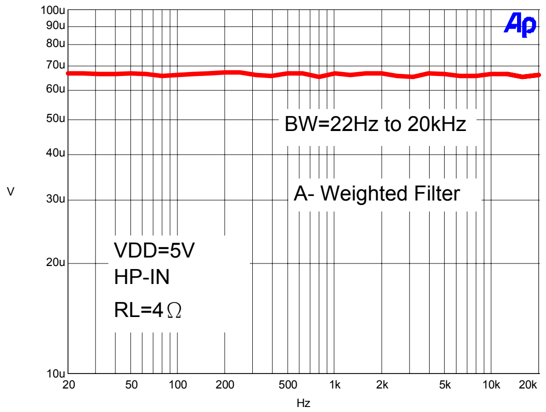


Figure 43

OUTPUT NOISE VOLTAGE vs FREQUENCY

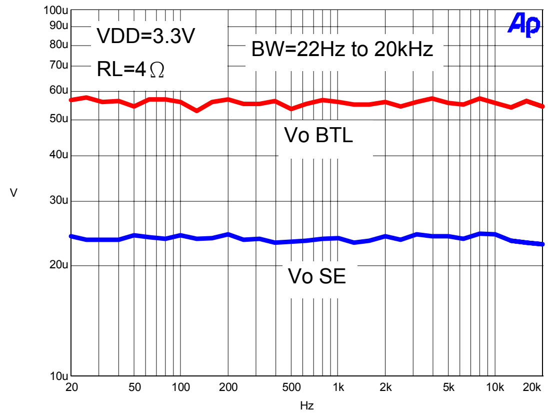


Figure 44

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

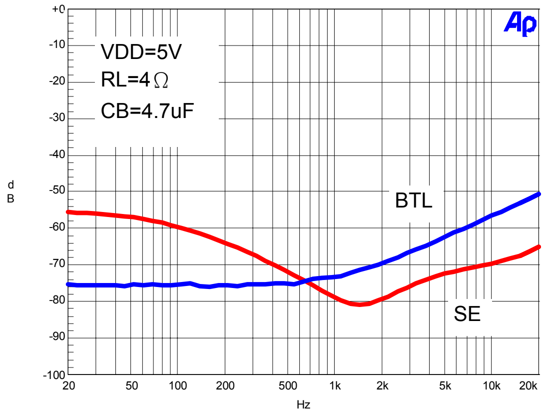


Figure 45

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

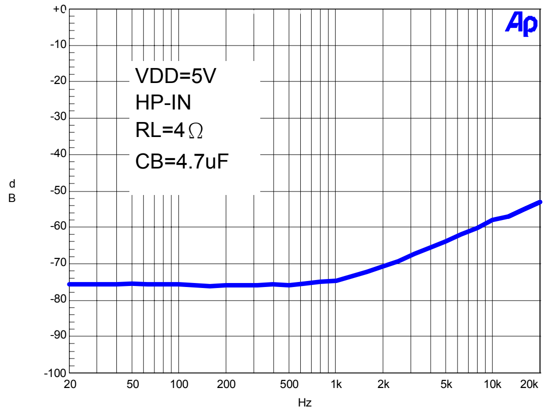


Figure 46

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

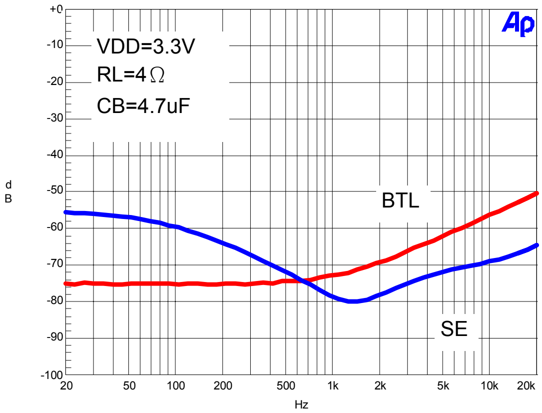


Figure 47

CROSSTALK vs FREQUENCY

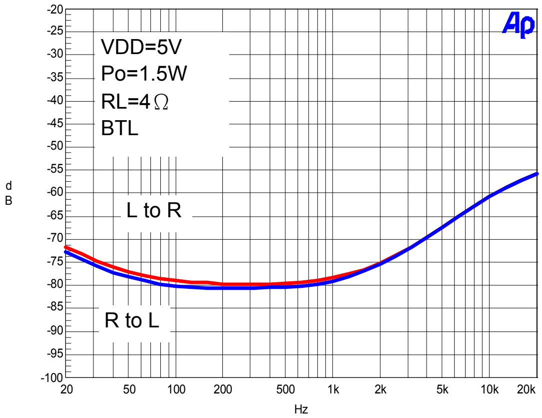


Figure 48

CROSSTALK vs FREQUENCY

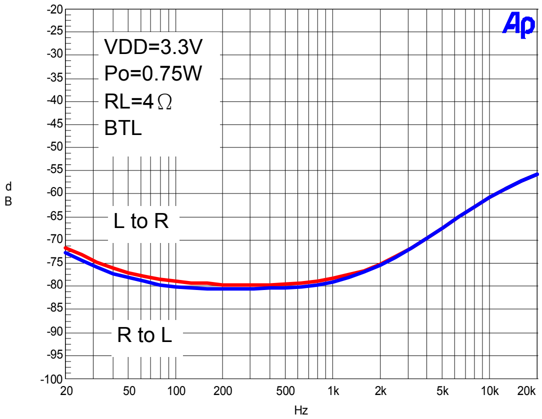


Figure 49

CROSSTALK vs FREQUENCY

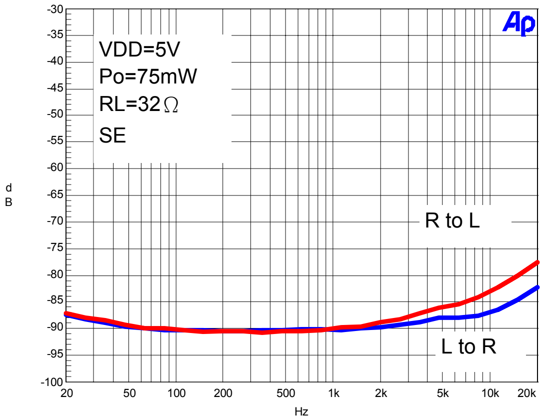


Figure 50

CROSSTALK vs FREQUENCY

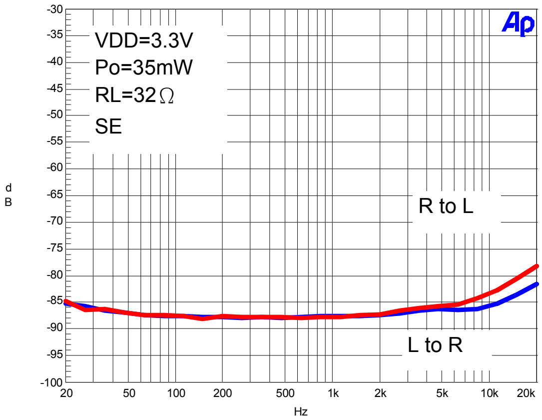


Figure 51

CROSSTALK vs FREQUENCY

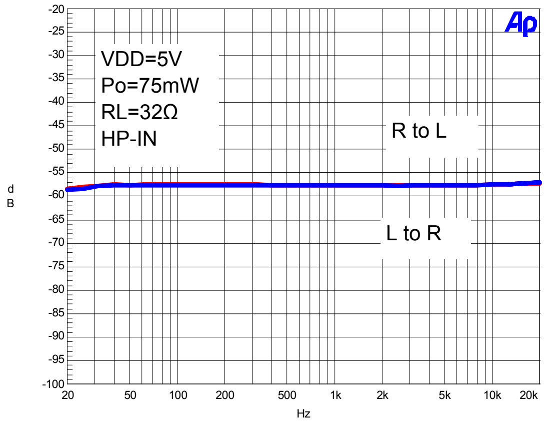


Figure 52

CLOSED LOOP RESPONSE

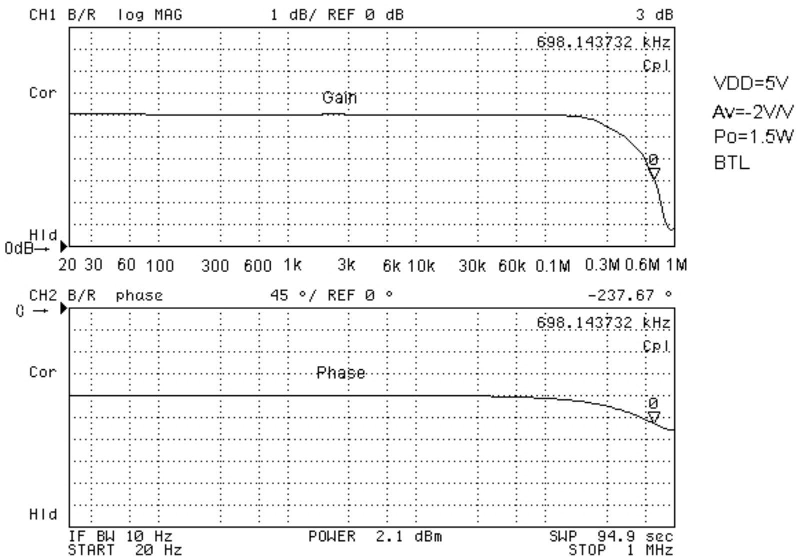


Figure 53

CLOSED LOOP RESPONSE

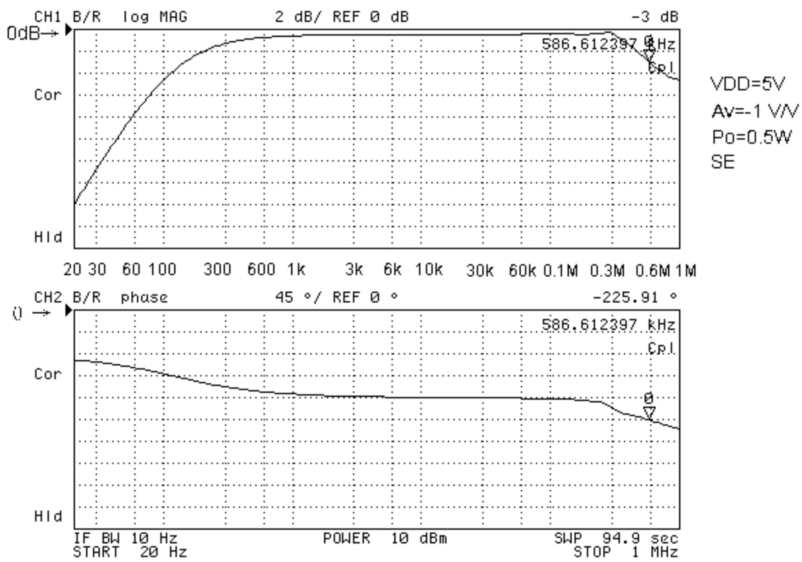


Figure 54

CLOSED LOOP RESPONSE

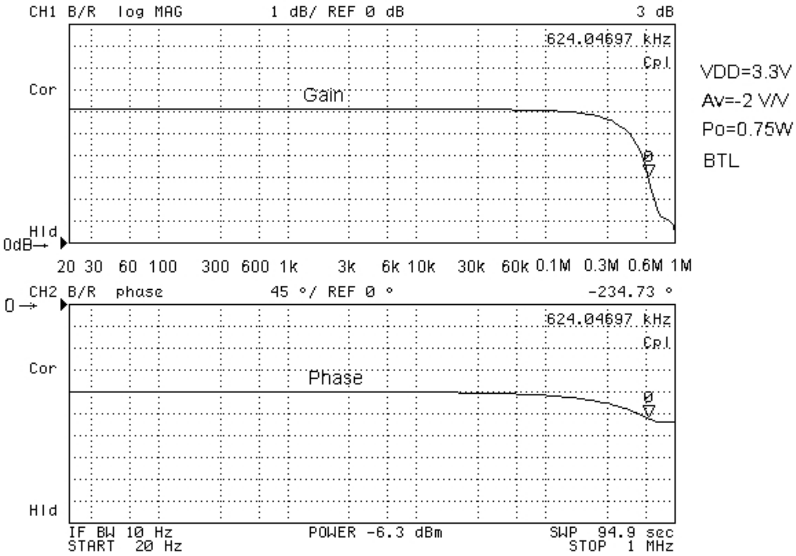


Figure 55

CLOSED LOOP RESPONSE

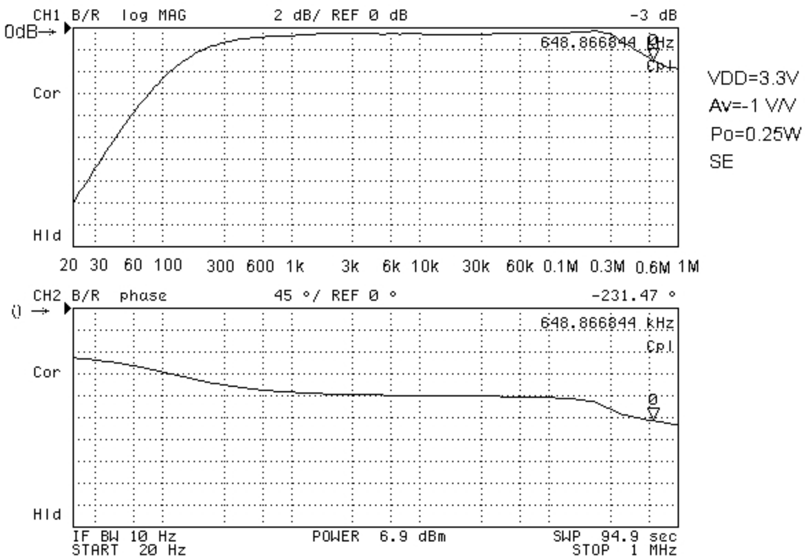


Figure 56

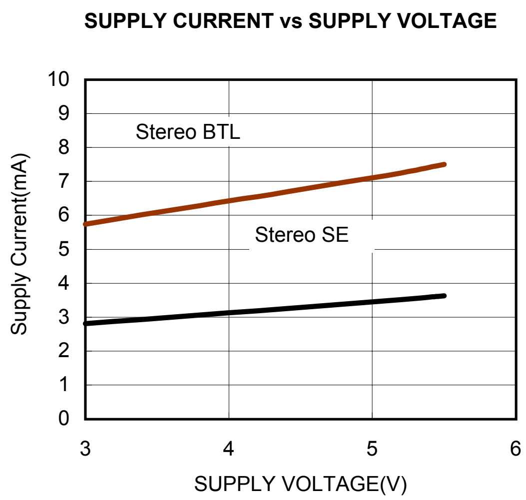


Figure 57

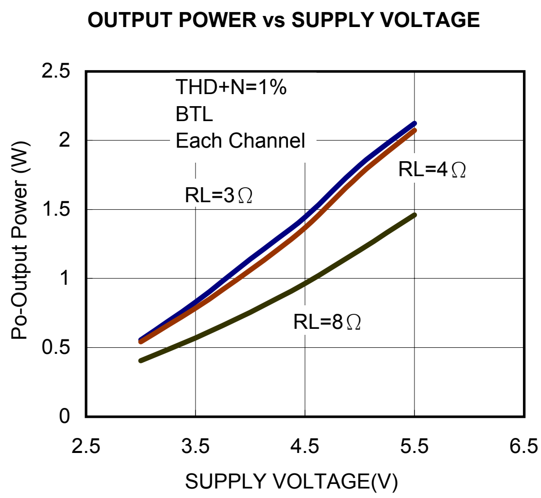


Figure 58

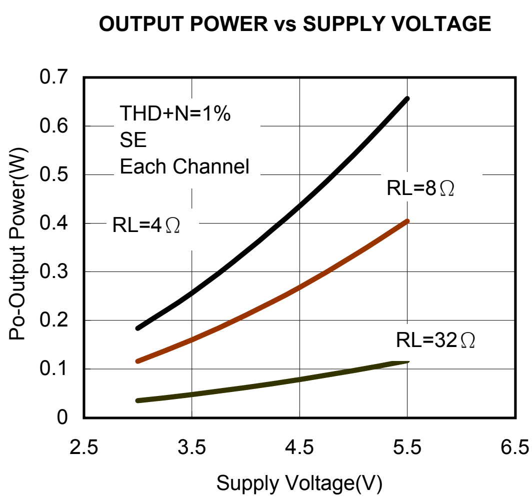


Figure 59

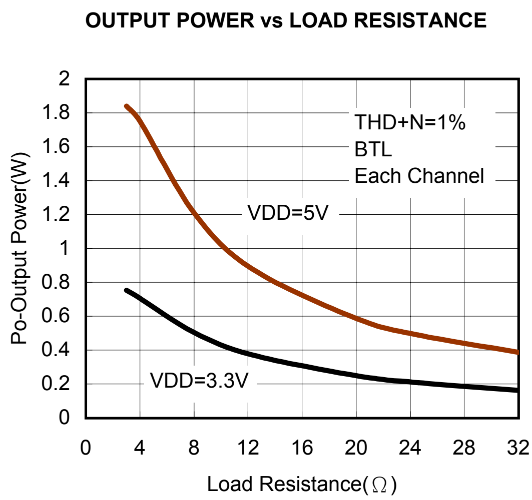


Figure 60

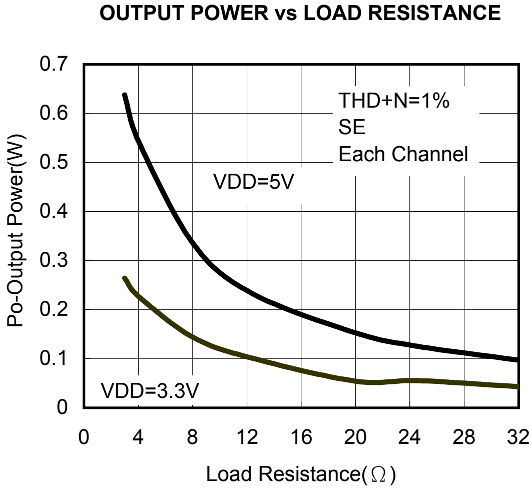


Figure 61

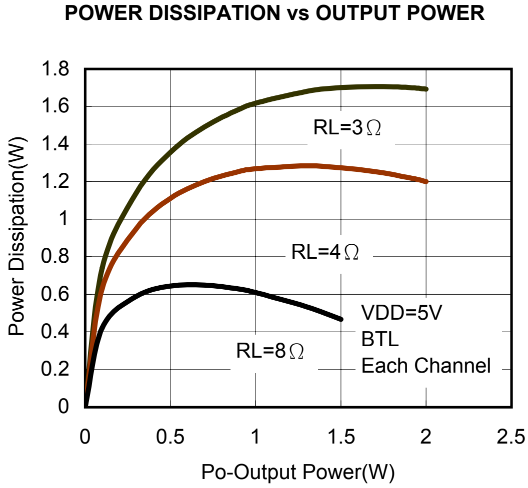


Figure 62

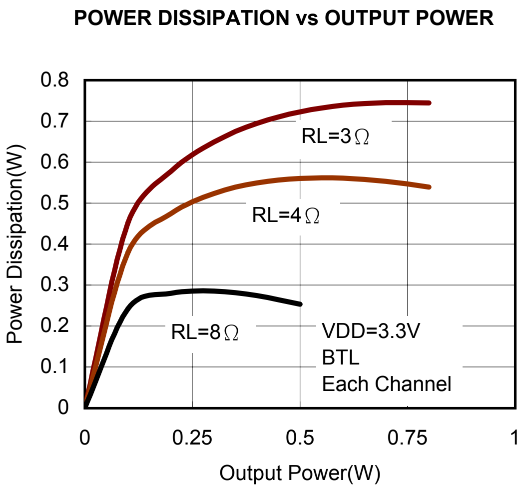


Figure 63

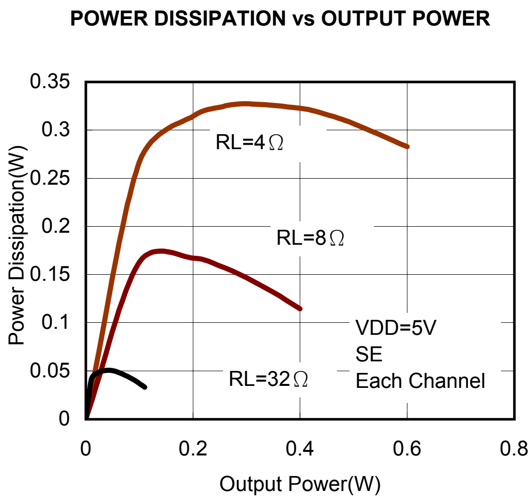


Figure 64

POWER DISSIPATION vs OUTPUT POWER

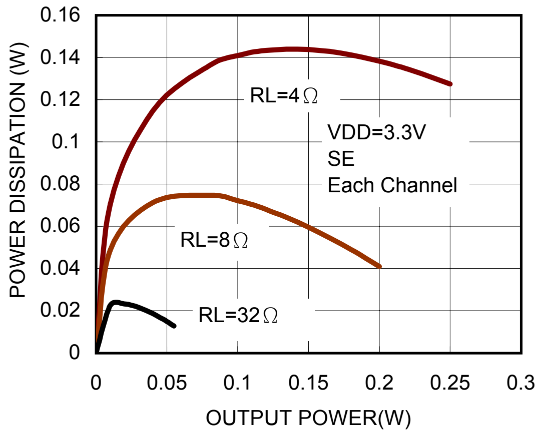
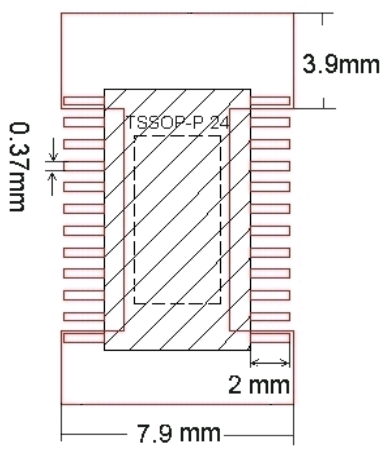
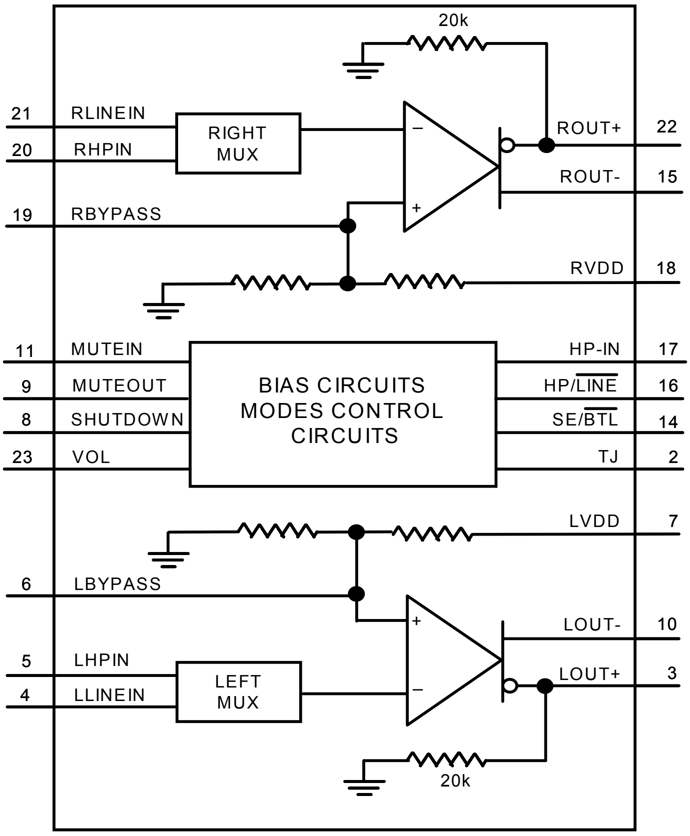


Figure 65

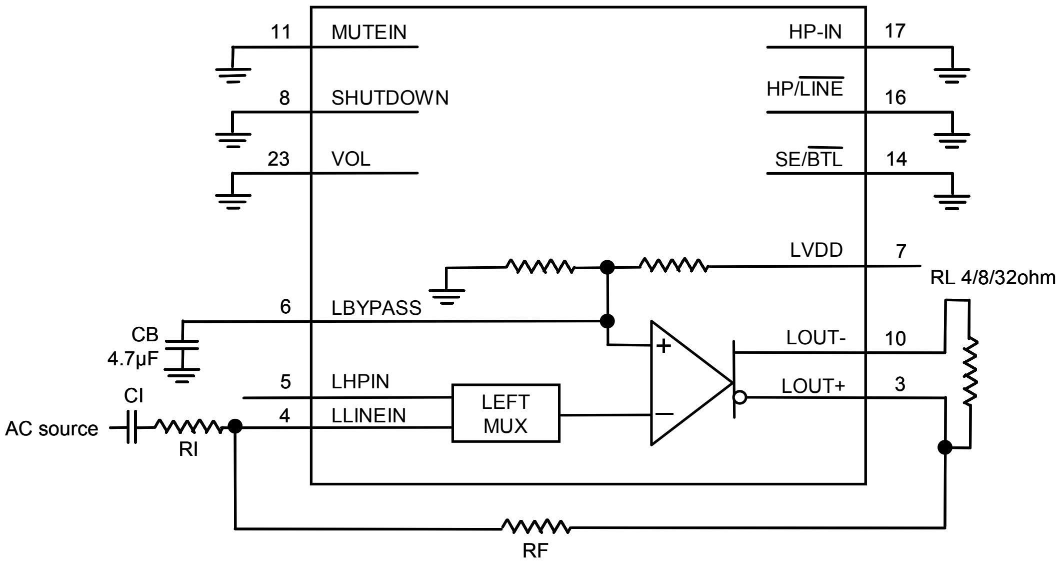
Recommended PCB Layout



Block Diagram

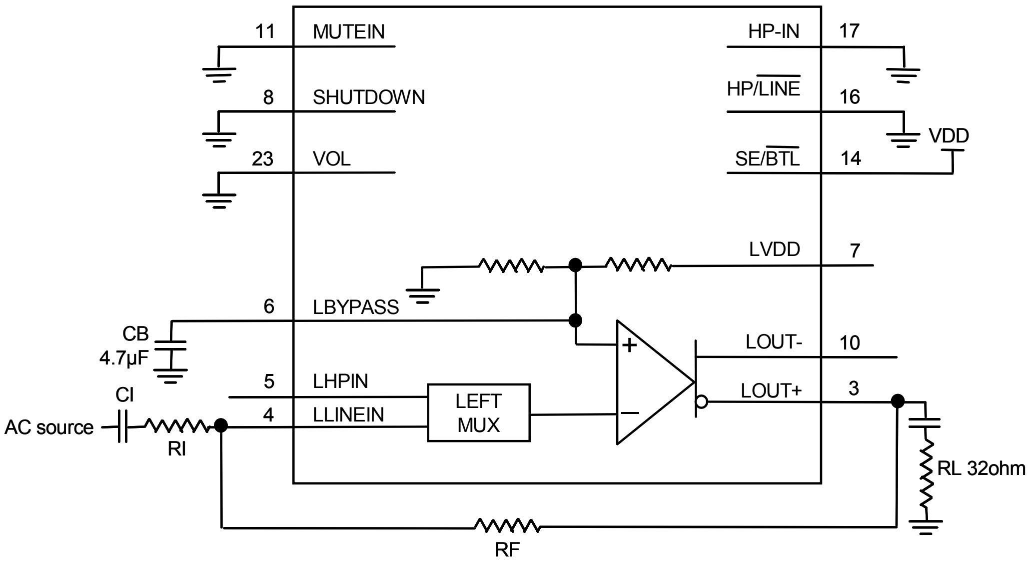


Parameter Measurement Information

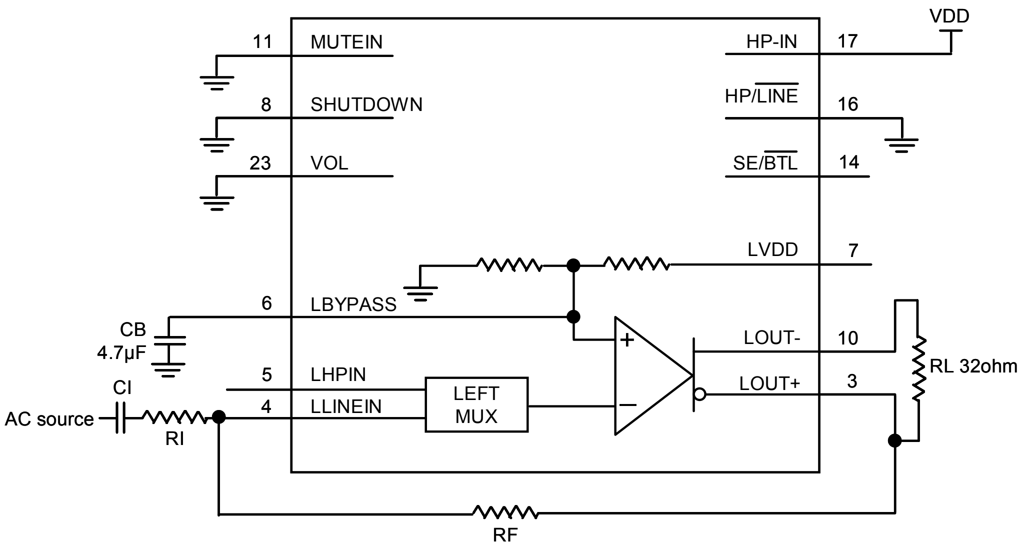


BTL Mode Test Circuit

Parameter Measurement Information (Continued)



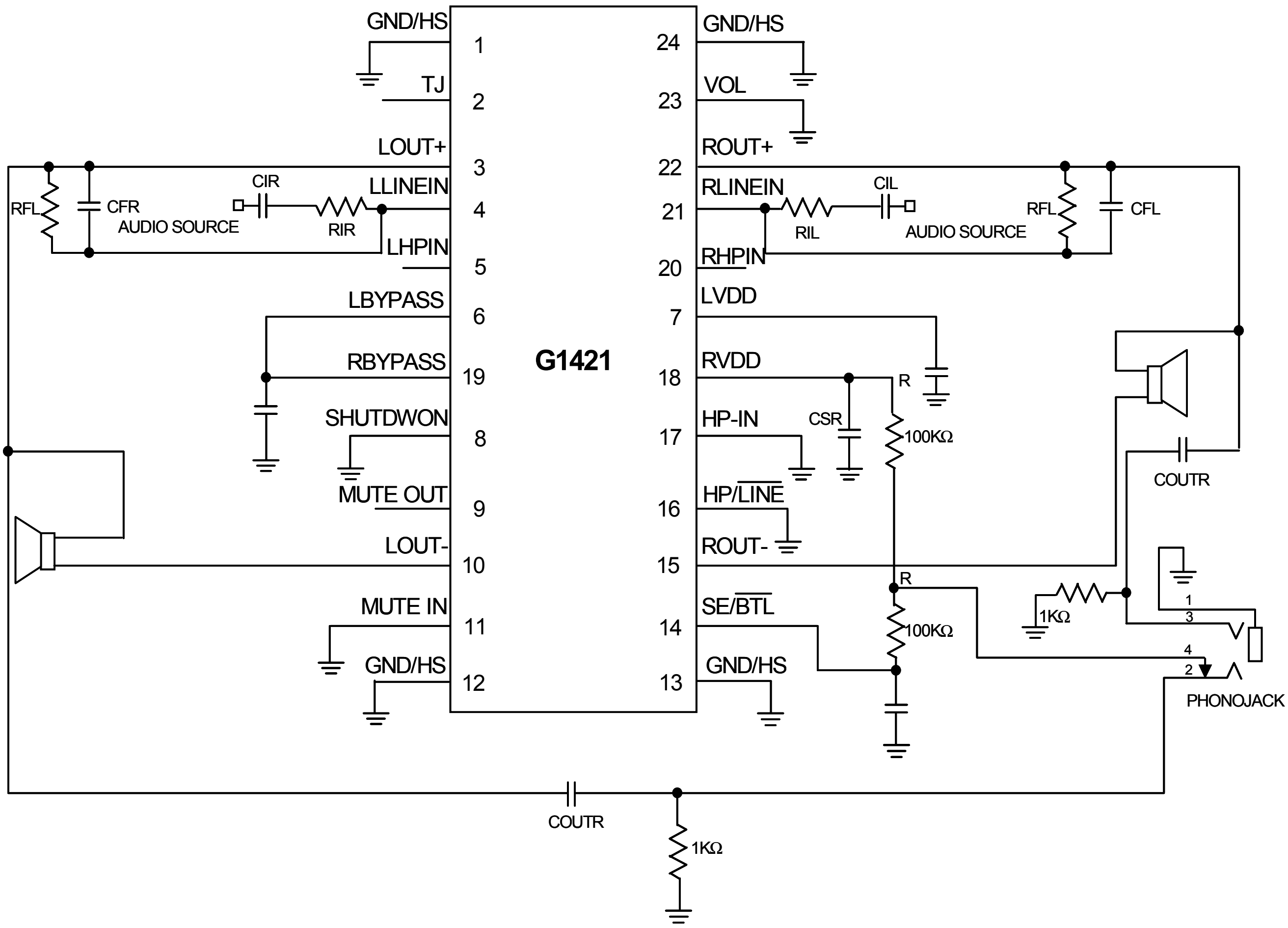
SE Mode Test Circuit



HP-IN Mode (Non-DC Blocking Cap) Test Circuit

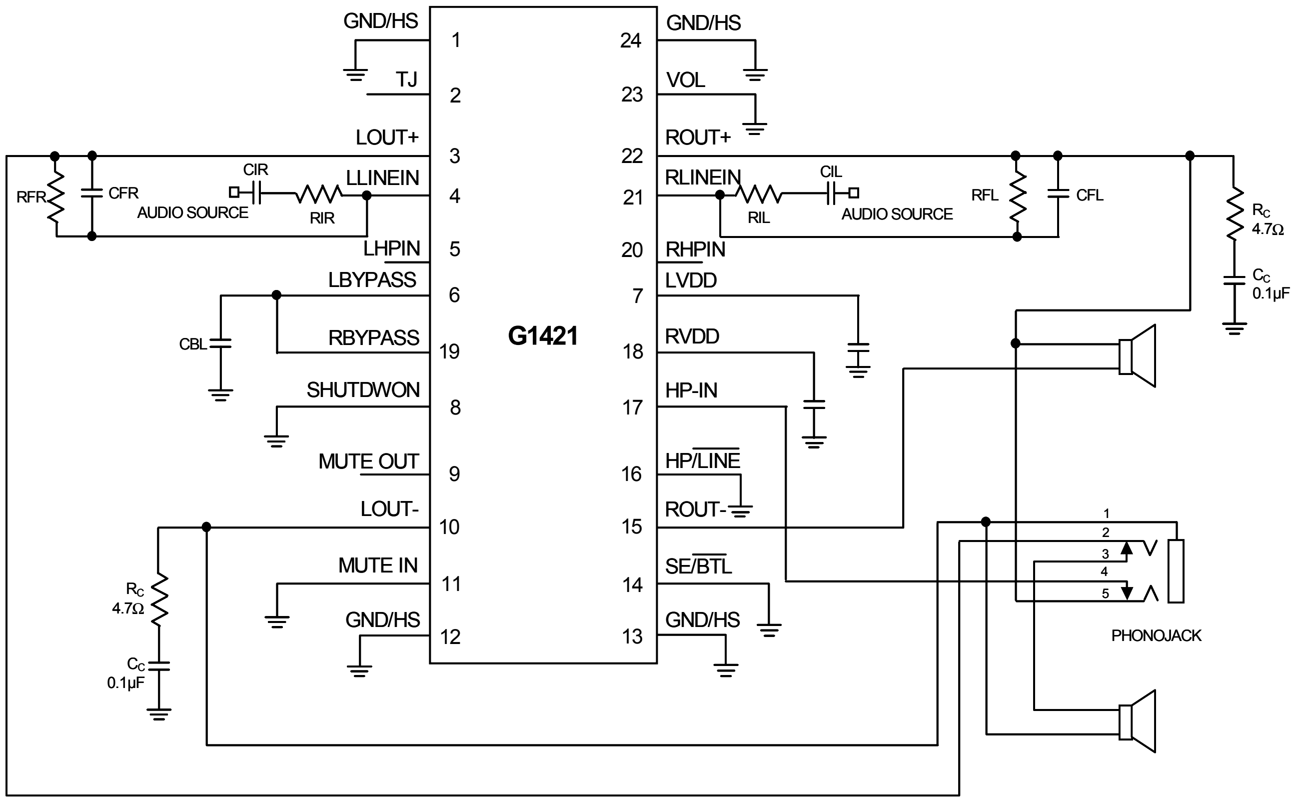
Application Circuits

With DC blocking Capacitors Application



Application Circuits (Continued)

No DC Blocking Capacitors Application



Logical Truth Table

INPUTS					OUTPUT	AMPLIFIER STATES				
SE/$\overline{BTL}$	HP/$\overline{LINE}$	HP-IN	Mute In	Shutdown	Mute Out	Input	L/R Out+	L Out-	R Out-	Mode
X	X	X	----	High	----	X	----	----	----	Mute
Low	X	X	High	----	High	X	VDD/2	VDD/2	VDD/2	Mute
High	X	X	High	----	High	X	VDD/2	----	----	Mute
X	X	High	High	----	High	X	VDD/2	VDD/2	----	Mute
Low	Low	Low	Low	Low	Low	L/R Line	BTL Output	BTL Output	BTL Output	BTL
Low	High	Low	Low	Low	Low	L/R HP	BTL Output	BTL Output	BTL Output	BTL
High	Low	Low	Low	Low	Low	L/R Line	SE Output	----	----	SE
High	High	Low	Low	Low	Low	L/R HP	SE Output	----	----	SE
X	Low	High	Low	Low	Low	L/R Line	SE Output	VDD/2	----	HP-IN
X	High	High	Low	Low	Low	L/R HP	SE Output	VDD/2	----	HP-IN

Application Information

Input MUX Operation

There are two input signal paths – HP & Line. With the prompt setting, G1421 allows the setting of different gains for BTL and SE modes. Generally, speakers typically require approximately a factor of 10 more gain for similar volume listening levels as compared with headphones.

$$\text{SE Gain}_{(HP)} = -(R_{F(HP)}/R_{I(HP)})$$

$$\text{BTL Gain}_{(LINE)} = -2(R_{F(LINE)}/R_{I(LINE)})$$

To achieve headphones and speakers listening parity, ($R_{F(LINE}/R_{I(LINE)}$) is suggested to be 5 times of ($R_{F(HP)}/R_{I(HP)}$). The ratio of ($R_{F(HP)}/R_{I(HP)}$) can be determined by the applications. When the optimum distortion performance into the headphones (clear sound) is important, gain of –1 (($R_{F(HP)}$ / $R_{I(HP)}$) = 1) is suggested.

Single Ended Mode Operation

G1421 can drive clean, low distortion SE output power into headphone loads (generally 16Ω or 32Ω) as in Figure 1. Please refer to **Electrical Characteristics** to see the performances. A coupling capacitor is needed to block the dc offset voltage, allowing pure ac signals into headphone loads. Choosing the coupling capacitor will also determine the 3 dB point of the high-pass filter network, as Figure 2.

$$f_C=1/(2\pi R_L C_C)$$

For example, a 68uF capacitor with 32Ω headphone load would attenuate low frequency performance below 73Hz. So the coupling capacitor should be well chosen to achieve the excellent bass performance when in SE mode operation.

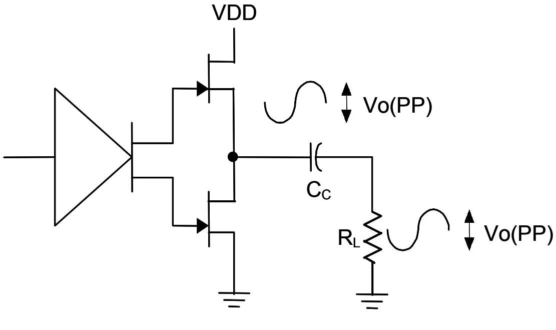


Figure 1

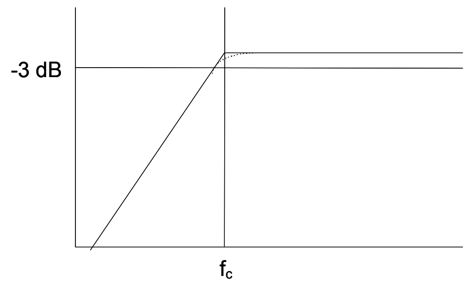


Figure 2

Bridged-Tied Load Mode Operation

G1421 has two linear amplifiers to drive both ends of the speaker load in Bridged-Tied Load (BTL) mode operation. Figure 3 shows the BTL configuration. The differential driving to the speaker load means that when one side is slewing up, the other side is slewing down, and vice versa. This configuration in effect will double the voltage swing on the load as compared to a ground reference load. In BTL mode, the peak-to-peak voltage V_O(PP) on the load will be two times than a ground reference configuration. The voltage on the load is doubled, this will also yield 4 times output power on the load at the same power supply rail and loading. Another benefit of using differential driving configuration is that BTL operation cancels the dc offsets, which eliminates the dc coupling capacitor that is needed to cancelled dc offsets in the ground reference configuration. Low-frequency performance is then limited only by the input network and speaker responses. Cost and PCB space can be minimized by eliminating the dc coupling capacitors.

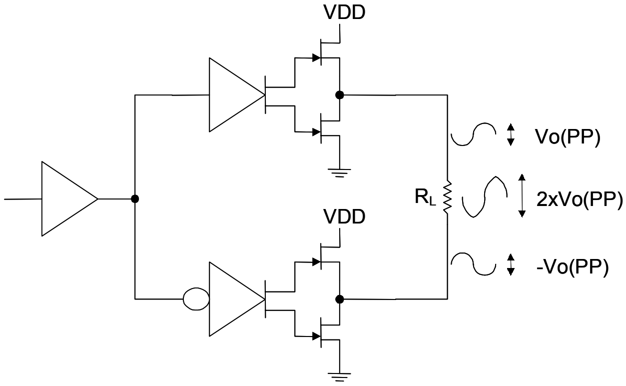


Figure 3

HP-IN Mode Operation

An internal weakly pull-up circuit is connected to HP-IN control pin (pin 17). When this pin is left unconnected or tied to VDD, HP-IN mode is activated, ignoring SE/$\overline{BTL}$ setting. In normal SE/$\overline{BTL}$ mode operations, this HP-IN pin should be tied to GND. In HP-IN mode, the linear amplifiers of LOUT+ (pin 3) /ROUT+ (pin 22) are still alive, the linear amplifier of ROUT- (pin 15) is deactivated, the linear amplifier of LOUT- (pin 10) supplies VDD/2 on this pin to cancel the dc offsets. (Please refer to Logical Truth Table and No DC CAP Application Circuit for detailed operation.) If connected VDD/2 on the LOUT- (pin 10) to the phone jacket, the dc offset can be eliminated without using coupling capacitors in headphone applications. By using HP-IN mode, cost and PCB space can be further minimized than traditional headphone applications with coupling capacitors. The HP-IN configuration is shown on Figure 4.

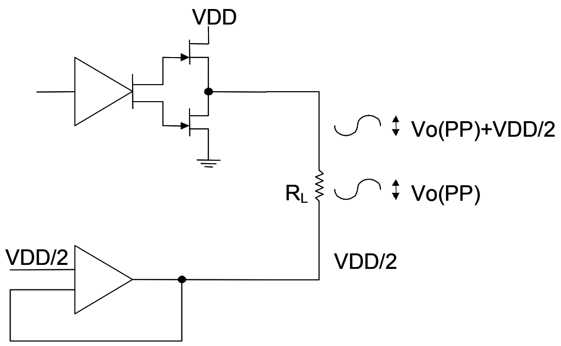


Figure 4

Short circuit protection is implemented on LOUT- (pin10) to avoid the short-circuit damage caused by the sleeve of the phone jack connected to ground accidentally during the module assembling. When short-circuit is detected, the linear amplifier of LOUT- (pin 10) will turn off for a period. After this period, it activates again. If the short circuit condition still exists, it will be turned off again. With this protection, the damage caused by larger dc short circuit current (from VDD/2 to GND) can be avoided.

MUTE and SHUTDOWN Mode Operations

G1421 implements the mute and shutdown mode operations to reduce supply current, $I_{DD,}$ to the absolute minimum level during nonuse periods for battery-power conservation. When the shutdown pin (pin 8) is pulled high, all linear amplifiers will be deactivated to mute the amplifier outputs. And G1421 enters an extra low current consumption state, I_{DD} is smaller than 5μA. If pulling mute-in pin (pin 11) high, it will force the activated linear amplifier to supply the VDD/2 dc voltage on the output to mute the AC performance. In mute mode operation, the current consumption will be a little different between BTL, SE and HP-IN modes. (SE < HP-IN < BTL) Typically, the supply current is about 2.5mA in BTL mute operation. Shutdown and Mute-In pins should never be left unconnected, this floating condition will cause the amplifier operations unpredictable.

Maximum Power Clampping Function

G1421 supports the maximum output power clamping function to avoid damaging the speaker when the amplifier output a power beyond the speaker tolerance. The Vol pin (pin 23) is weakly pull-low internally. If inputting a non-zero voltage (low boundary voltage) to the Vol pin, G1421 will generate a high boundary voltage which the difference between the VDD/2 and the high boundary voltage is the same as the difference between the VDD/2 and the low boundary voltage. (i.e. V_{OH} – VDD/2 = VDD/2 – V_{OL}) Then the outputs of linear amplifiers will be effectively limited between the high/low boundary voltage, the maximum output power is clamped. By setting the voltage of Vol, the maximum output power can be well controlled. When the maximum power clamping function is not used, the Vol pin should be floated or tied to GND.

Optimizing DEPOP Operation

Circuitry has been implemented in G1421 to minimize the amount of popping heard at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker and making the differential voltage generated at the two ends of the speaker. To avoid the popping heard, the bypass capacitor should be chosen promptly, $1/(C_B x 100k\Omega) \leqq 1/(C_I*(R_I+R_F))$. Where 100kΩ is the output impedance of the mid-rail generator, C_B is the mid-rail bypass capacitor, C_I is the input coupling capacitor, R_I is the input impedance, R_F is the gain setting impedance which is on the feedback path. C_B is the most important capacitor. Besides it is used to reduce the popping, C_B can also determine the rate at which the amplifier starts up during startup or recovery from shutdown mode.

De-popping circuitry of G1421 is shown on Figure 5. The PNP transistor limits the voltage drop across the 50kΩ by slewing the internal node slowly when power is applied. At start-up, the voltage at BYPASS capacitor is 0. The PNP is ON to pull the mid-point of the bias circuit down. So the capacitor sees a lower effective voltage, and thus the charging is slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an R-C circuit.

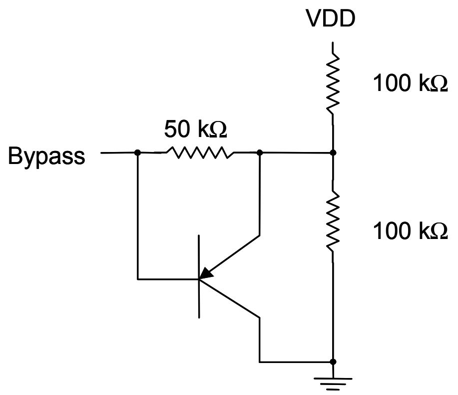


Figure 5

Junction Temperature Measurement

Characterizing a PCB layout with respect to thermal impedance is very difficult, as it is usually impossible to know the junction temperature of the IC. G1421 TJ (pin 2) sources a current inversely proportional to the junction temperature. Typically TJ sources–120µA for a 5V supply at 25°C. And the slope is approximately 0.22µA/°C. As the resistors have a tolerance of ±20%, these values should be calibrated on each device. When the temperature sensing function is not used, TJ pin can be left floating or tied to VDD to reduce the current consumption.

Temperature sensing circuit is shown on Figure 6.

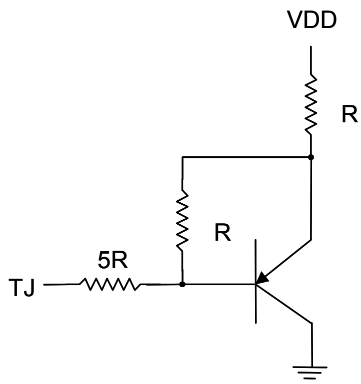
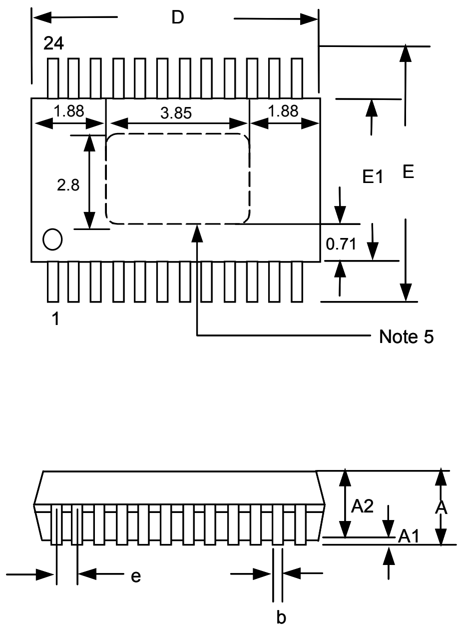
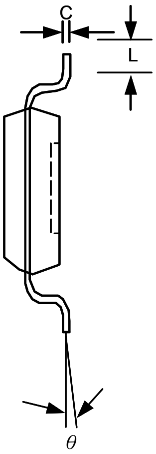


Figure 6

Package Information

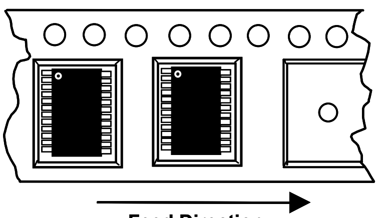




NOTE:
1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance ±0.1mm unless otherwise specified
3. Coplanarity : 0.1mm
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Follow JEDEC MO-153

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-----	-----	1.15	-----	-----	0.045
A1	0.00	-----	0.10	0.000	-----	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-----	0.30	0.007	-----	0.012
C	0.09	-----	0.20	0.004	-----	0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E	6.20	6.40	6.60	0.244	0.252	2.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-----	0.65	-----	-----	0.026	-----
L	0.45	0.60	0.75	0.018	0.024	0.030
y	-----	-----	0.10	-----	-----	0.004
θ	0º	-----	8º	0º	-----	8º

Taping Specification



Feed Direction
Typical TSSOP Package Orientation