INTERNATIONAL MICROCIRCUITS INC

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IMI7000 FAMILY

CMOS GATE ARRAY

PRODUCT FEATURES

- 1.5 micron CMOS
- Oxide-isolated silicon-gate process
- Dual level metalization
- Fully autoroutable
- 792 to 12,000 2-input NAND equivalents
- Up to 220 I/O connections
- All Inputs and Outputs TTL or CMOS compatible
- Fully supported by IMI's Easygate CAE enhancement software
- Extensive Macro Cell Library available for Daisy and Mentor workstations
- Full MIL-STD 883 screening available
- Wide selection of packages available

PRODUCT DESCRIPTION

The IMI7000 family of gate arrays from International Microcircuits Incorporated is fabricated from an advanced 1.5 micron double metal oxide-isolated CMOS process. This process is unmatched for speed and density, while offering users access to highly integrated logic solutions with the associated system advantages that large integration provides. The IMI7000 series also provides high noise immunity and very low power consumption typical of CMOS. All inputs and outputs may be compatible with either TTL or CMOS logic levels, and are fully protected from electrostatic discharge and latch-up. The size of the family ranges from 800 to 12,000 two-input NAND equivalents and offers up to 220 input or output connections to efficiently solve most applications with the best gate utilization.

IMI also offers complete design support using the powerful Easygate CAE enhancement software. The extensive macro cell library and other IMI proprietary software is available for Daisy or Mentor workstations. Combining this with IMI's internal CAD system offers the user unsurpassed assurance that his design will be integrated quickly and accurately.

PRODUCT SUMMARY

Part Number	Two Input Gates Equivalents	Total Pads	Dedicated Power Pads	Output Drivers
IMI7080	792	52	8	44
IMI7160	1632	78	8	70
IMI7220	2232	90	8	82
IMI7340	3432	112	8	104
IMI7490	4900	136	8	128
IMI7620	6210	158	8	150
IMI7800	8000	178	8	170
IMI712K	12,000	230	8	222

PRODUCT PACKAGING

Part Number	Epoxy Dual Inline 22 24 28 40 64	Ceramic Side—Braze Dip 22 24 28 40 48 64	LCC and Pin Grid Array 24 28 32 36 40 44 48 52 56 64 68 84 100 120 132 144 160 180
IMI7160			
IMI7220			
IMI7340			
IMI7490			
IMI7620			
IMI7800			

MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature	−55°C to +125°C
Voltage on any pin relative to V_{SS}	−0.3V, +7V
Voltage on any pin relative to V_{DD}	+0.3V

These ratings define stress parameters beyond which useful product performance may be impaired. Functional operation of these devices is specified only for subsets of these maximum ratings.

All MOS circuits are susceptible to damage from stress voltages, even where inputs are internally protected. It is suggested that conventional precautions be observed to avoid exposure to excessive voltages during storage, handling, and use.

OPERATING CHARACTERISTICS

Parameter		Condition	TA=+25°C V_{DD}=5.0V		TA=+70°C V_{DD}=4.75V		TA=+125°C V_{DD}=4.5V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{OH}	Output HIGH Current (Note 1)	$V_{OH} = V_{DD} - 0.1V$	0.7		0.6		0.5		mA
		V_{OH} = 2.4V	8.0		6.0		5.0		
I_{OL}	Output LOW Current (Note 1)	V_{OL} = 0.10V	1.7		1.3		1.0		
		V_{OL} = 0.40V	8.0		6.0		5.0		
V_{IH}	Input HIGH voltage (Note 2)	TTL Input	2.0		2.0		2.0		Volts
		CMOS Input	3.5		3.5		3.5		
V_{IL}	Input LOW Voltage (Note 2)	TTL Input		0.8		0.8		0.8	
		CMOS Input		1.5		1.5		1.5	
I_{IN}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{DD}$		±1.0		±1.0		±1.0	μA
I_{DD}	V_{DD} Supply Current (Note 3)	Active Per Cell Per MHz, typ.	2.0		2.5		3.0		
		Quiescent Per Chip, typ.	5		10		20		
CI	Input Capacitance (Note 4)	Typical:	4		4		4		pF
CO	Output Capacitance (Note 4)	Typical:	8		8		8		
Output Buffer Delay		Load = 10 LSTTL +40 pF		6.0		8.0		10.0	ns
Inverter Delay		Typical interconnect.	0.52	1.18	0.65	1.47	0.83	1.86	
2-Input NAND Delay		Worst case processing.	0.75	1.54	0.93	1.92	1.18	2.42	
2-Input NOR Delay		Average of both transitions.	0.90	1.76	1.12	2.19	1.41	2.76	
2-Input Exclusive NOR Delay		(Note 5)	2.72	3.38	3.39	4.21	4.28	5.32	
D-Type Flip-Flop	Clock to Q Delay	Maximum Values for	3.45	4.11	4.30	5.12	5.43	6.47	
	D Setup	F.O. = 1 and F.O. = 4	2.20		2.50		3.00		
	D Hold		2.20		2.50		3.00		
	Toggle Rate		100		85		70		MHz

Notes

1. Output currents indicated are available from a single output driver that actively pulls both high and low. The array can be designed to parallel outputs for more drive or to create special output configurations.
2. Users may select, for each interface signal, either CMOS-compatible or TTL-compatible logic levels. TTL interfaces require operation at TTL supply voltages.
3. Supply currents are a combination of DC leakage components and AC transient components. At idle or very low operating frequencies, supply current is heavily dominated by simple leakage, and attains extremely low values. Idle currents are only very roughly proportional to the number of gate-cells used. Operating currents include AC components that depend on frequency and on the average number of internal nodes that are changing state. In typical applications it is difficult to exceed the values shown per cell for cumulative logic designs, even at f_{max} operating frequencies.
4. Typical values are indicated for interface capacitance, since worst-case values will depend on the particular interface circuit configuration and on the particular package being used.
5. Actual internal logic delays depend on a number of factors, including processing parameters, supply voltage, temperature, fanout, and interconnect. The values shown are conservative representations of circuit performance actually experienced across a broad range of applications. Minimum values are stated for a fanout of one, while maximum values are stated for a fanout of four.

G4000 FAMILY

CMOS GATE ARRAY

PRODUCT FEATURES

- Standard Metal-Gate CMOS Technology
- 2V to 15V Power Supplies
- Up to 720 2-input NAND equivalents
- Up to 53 I/O connections
- Inputs and Outputs TTL or CMOS compatible
- All Inputs and Outputs protected from overload and latch-up
- Typical Internal Delays of 60ns at 5V
- Clock rates up to 2MHz at 5V, 6MHz at 15V
- Full MIL-STD 883 screening available
- Wide selection of packages available

PRODUCT DESCRIPTION

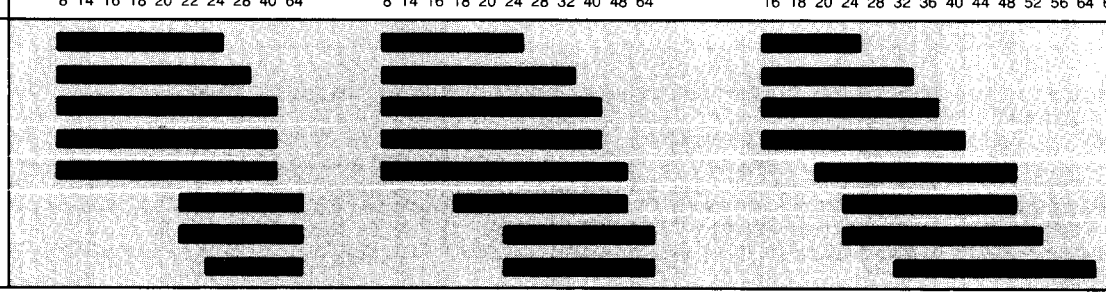
Metal-Gate CMOS technology is used in fabrication of the G4000 Master slice family of gate arrays. This provides both high noise immunity and low power consumption plus operation over a power supply range of 2V to 15V. The internal gate delays are typically 60 nsec, allowing use of worst-case clock rates up to 2MHz. All inputs may be compatible with either TTL or CMOS external logic levels, and include extensive protection networks to help prevent damage from static charge accumulation. All inputs and outputs are also protected from latch-up. Output buffers can directly interface either TTL or CMOS logic levels. Each output buffer can drive two LSTTL loads. Additional output drive current can be obtained from paralleling output buffers. Gate complexities range from 90 to 720 2-input NAND equivalents with pin counts ranging from 23 to 53. Full Military screening is also available.

PRODUCT SUMMARY

Part Number	Total Transistors	Two Input Gates Equivalents	Total Pads	Output Drivers
G4060	340	75	23	16
G4112	614	140	29	22
G4160	862	200	35	26
G4220	1174	275	37	30
G4264	1402	330	41	34
G4364	1916	455	47	40
G4420	2202	525	49	42
G4480	2510	600	53	46

PRODUCT PACKAGING

Part Number	Epoxy Dual Inline 8 14 16 18 20 22 24 28 40 64	Ceramic Side—Braze Dip 8 14 16 18 20 24 28 32 40 48 64	LCC and Pin Grid Array 16 18 20 24 28 32 36 40 44 48 52 56 64 68 84 100
G4060			
G4112			
G4160			
G4220			
G4264			
G4364			
G4420			
G4480			



OPERATING CHARACTERISTICS

Storage Temperature	−65°C to +150°C
Ambient Temperature	−55°C to +125°C
Voltage on any pin relative to V_{SS}	−0.3V, +15V
Voltage on any pin relative to V_{DD}	+0.3V

These ratings define stress parameters beyond which useful product performance may be impaired. Functional operation of these devices is specified only for subsets of these maximum ratings.

All MOS circuits are susceptible to damage from stress voltages, even where inputs are internally protected. It is suggested that conventional precautions be observed to avoid exposure to excessive voltages during storage, handling, and use.

MAXIMUM RATINGS

Parameter		Condition	TA=+25°C V_{DD}=5.0V		TA=+25°C V_{DD}=10.0V		TA=+25°C V_{DD}=15.0V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{OH}	Output HIGH Current (Note 1)	$V_{OH} = V_{DD} - 0.4V$	0.1		0.20		0.25		mA
		V_{OH} = 2.4V	1.0		3.0		4.0		
I_{OL}	Output LOW Current (Note 1)	V_{OL} = 0.10V	0.10		0.20		0.25		
		V_{OL} = 0.40V	0.40		0.80		1.00		
V_{IH}	Input HIGH voltage (Note 2)	TTL Input	2.0		2.0		2.0		Volts
		CMOS Input	3.5		7.0		10.5		
V_{IL}	Input LOW Voltage (Note 2)	TTL Input		0.8		0.8		0.8	
		CMOS Input		1.5		3.0		4.5	
I_{IN}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{DD}$		±1.0		±1.0		±1.0	μA
I_{DD}	V_{DD} Supply Current (Note 3)	Active Per Cell Per MHz, typ.	0.5		1.0		1.5		
		Quiescent Per Chip, typ.	2		4		6		
CI	Input Capacitance (Note 4)	Typical:	4		4		4		pF
CO	Output Capacitance (Note 4)	Typical:	6		6		6		
Output Buffer Delay		Load = 1 LSTTL +20 pF		150		100		75	ns
Inverter Delay		Typical interconnect.	25	90	15	60	10	45	
2-Input NAND Delay		Worst case processing.	30	110	20	70	15	55	
2-Input NOR Delay		Average of both transitions.	35	120	25	80	20	60	
2-Input Exclusive NOR Delay		(Note 5)	60	210	40	140	30	105	
D-Type Flip-Flop	Clock to Q Delay		65	220	45	150	35	110	
	D Setup		45		30		25		
	D Hold		0		0		0		
	Toggle Rate		2		4		6		MHz

Notes

1. Output currents indicated are available from a single output driver that actively pulls both high and low. The array can be designed to parallel outputs for more drive or to create special output configurations.
2. Users may select, for each interface signal, either CMOS-compatible or TTL-compatible logic levels. TTL interfaces require operation at TTL supply voltages.
3. Supply currents are a combination of DC leakage components and AC transient components. At idle or very low operating frequencies, supply current is heavily dominated by simple leakage, and attains extremely low values. Idle currents are only very roughly proportional to the number of gate-cells used. Operating currents include AC components that depend on frequency and on the average number of internal nodes that are changing state. In typical applications it is difficult to exceed the values shown per cell for cumulative logic designs, even at f_{max} operating frequencies.
4. Typical values are indicated for interface capacitance, since worst-case values will depend on the particular interface circuit configuration and on the particular package being used.
5. Actual internal logic delays depend on a number of factors, including processing parameters, supply voltage, temperature, fanout, and interconnect. If the component is not part of a documented critical path, additional interconnect may increase the delay. Minimum values are stated for a fanout of one, while maximum values are stated for a fanout of four.