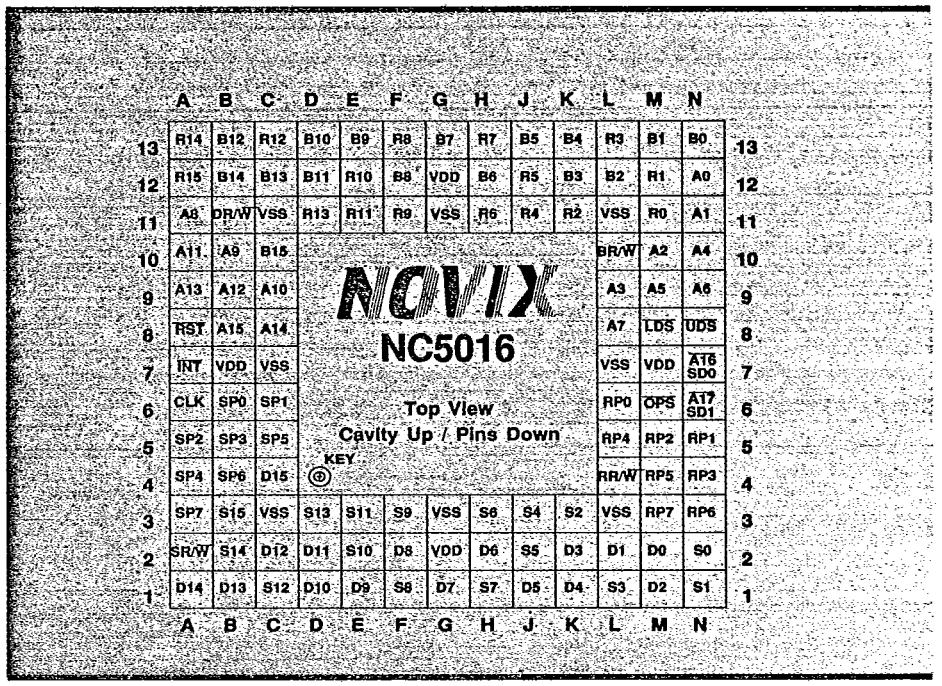
NC5016 12 MIPs MPU for high speed applications

Introduction

During the last decade technological advances in both computer hardware architecture and software development have been significant. These advances have been primarily propelled by the fact that new silicon processes can accommodation ever increasing number of transistors on one chip. In the mainstream of this evolution is the current generation of 16-bit microprocessors. Trailing closely behind hardware has been development in operating systems and languages. Recently introduced products have been intended for general purpose data processing designs. These products have been adopted for many applications, except those which require high speed, real time processing and control. To fill this gap NOVIX has developed the NC5016.



	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	R14	B12	R12	B10	B9	R8	B7	R7	B5	B4	R3	B1	B0	13
12	R15	B14	B13	B11	R10	B8	VDD	B6	R5	B3	B2	R1	A0	12
11	A8	DR/W	VSS	R13	R11	R9	VSS	R6	R4	R2	VSS	R0	A1	11
10	A11	A9	B15								BR/W	A2	A4	10
9	A13	A12	A10								A3	A5	A6	9
8	RST	A15	A14								A7	LDS	UDS	8
7	INT	VDD	VSS								VSS	VDD	A16 SDO	7
6	CLK	SP0	SP1								RP0	OPS	A17 SD1	6
5	SP2	SP3	SP5								RP4	RP2	RP1	5
4	SP4	SP6	D15								RR/W	RP5	RP3	4
3	SP7	S15	VSS	S13	S11	S9	VSS	S6	S4	S2	VSS	RP7	RP6	3
2	SR/W	S14	D12	D11	S10	D8	VDD	D6	S5	D3	D1	D0	S0	2
1	D14	D13	S12	D10	D9	S8	D7	S7	D5	D4	S3	D2	S1	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

General Description

The NC5016 is a single-chip microprocessor. It is not, by any means, a "clonic" design. It has no microcode and is compact in design. It is a stack/pointer design. Its design is optimized for direct execution of the primitives underlying the high level powerful programming language called FORTH. This microprocessor was designed and implemented with the latest in HCMOS technology (2 micron) for its low power consump-tion and high operating speed. It is an asynchronous static device with a nominal clock rate of 10 MHz. Since most FORTH instructions can be executed in one machine cycle, some in less, this processor is capable of exceeding 12 MIPs in performance.

This high operating speed, when coupled with a highly structured language - FORTH - which benefits from a stack/pointer approach, provides an ideal solution for applications in color bit-mapped graphics, imaging processing, simulation, animation, robotics, various forms of digital signal processing and scientific/engineering number crunching.

Features

- Word and byte addressability
- Direct execution of most FORTH language primitives in one machine cycle
- Single cycle subroutine call within 64-kByte page.
- No overhead required for sub-routine return
- Single cycle to set, clear or toggle any bit of Top Parameter
- Multiple FORTH words can be executed in one cycle
- Multiple bus structure to optimize parallel operations
- Efficient memory to memoy transfer by using repeated Fetches or Stores
- Fixed point, 16/32-bit MULTIPLY in 20 cycles
- Fixed point, 32/16-bit DIVIDE in 22 cycles
- 31/16-bit fixed point SQUARE ROOT operations in 23 cycles
- 100ns machine cycle, 10 MHz clock rate
- Hardware support provided for 16 external registers via B-port and Program Status Register
- One non-maskable and two maskable interrupts
- Extended memory to include three (3) Memory Spaces:

  Program Space

  Data Space

  Local Space
- Total memory capacity expandable to 512K bytes
- Hardware facilities provided to handle multi-tasking (128 tasks)

The NC5016 is upwards pin compatible from the NC4016.

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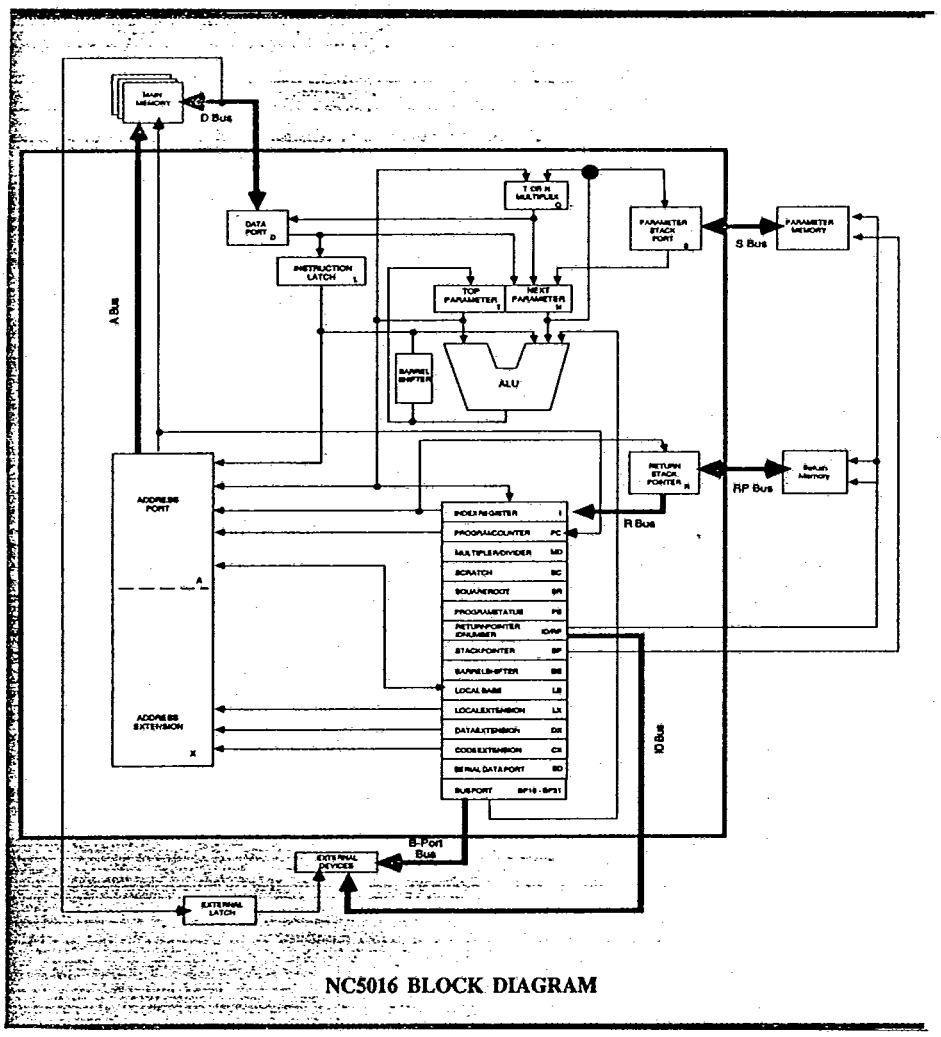
THE NC5016 Architecture

The NC5016 employs the most straight forward hardware architecture with emphasis on high speed and highly parallel operations. The hardware design has been optimized for direct execution of the FORTH programming language without the use of microcode. As shown in the Block Diagram the Novix NC5016 architecture is a stack oriented structure which is supported with multiple buses. This multiple-stack and multiple-bus structure is primarily responsible for high speed instruction execution of up to 12 million instructions per second.

A functional description of major hardware elements is shown in the Block Diagram of the architecture.



NC5016 BLOCK DIAGRAM

Major Buses

A Bus: This is a 26-bit wide Address Bus, (A22 through A0) and three additional pins dedicated to "Local", "Data" and "Code" segments. It connects the Address Port to the Main Memory, and it may be used as input under certain conditions. It consists of the Address Port and the Address Extension Port.

D Bus: This 16-bit wide (D15 through D0) Data Bus is bi-directional. It connects the Data Port to the Main Memory.

RP Bus: The Return Stack Address Bus is 9-bits wide (RP8 through RP0). It provides the return stack pointer address to the External Return Memory.

ID Bus: (ID6 through ID0), the upper 7 bits of the RP register may be used for the user task selection.

R Bus: The Return Stack Data Bus is 16-bits wide (R15 through R0). This bus is bi-directional, connecting the on-chip Index Register via the R-Port and the External Return Memory.

B-Port Bus: The B-Port Data Bus is 16-bits wide (B15 through B0). It is bi-directional, connecting the Top Parameter Register on-chip and the External Register File/IO Port.

SP Bus: The parameter Stack Address Bus is a 9-bit address bus (SP8 through SP0), connecting the on-chip Stack Pointer Register to the External Parameter Memory.

S Bus: The Parameter Stack Data Bus (S15 through S0) is a 16-bit bi-directional bus, connecting the on-chip Next Parameter Register via the S-Port to the External Parameter.

Hardware Functional Blocks

Address Port: 15-bit bi-directional port which provides the address to the main memory. The contents of this port are driven from the Index Register, Program Counter, Instruction Latch or the Top Parameter Register, in conjunction with the Segment Registers DX, LX and CX.

Address Extension Port: 11-bit output port which extends the addressable memory to 48 megabytes.

Instruction Latch: A 16-bit, bi-directional input/output port. It holds the data to/from the main memory. Internally, it is connected to the Instruction Latch, Top Parameter Register and the Next Parameter Register.

Data Port: A 16-bit, bi-directional input/output port. It holds the data to/from the main memory. Internally, it is connected to the Instruction Latch, Top Parameter and the Next Parameter.

Top Parameter Register (T): A 16-bit register which is the top parameter on the stack. It is one of the sources and the only destination of all ALU functions (such as +, -, AND, XOR, etc.) required to execute FORTH arithmetic and logic primitives. See description of Next Parameter for additional functions.

Next Parameter Register (N): A 16-bit register which contains the next location on the parameter stack as described in FORTH. This register is used in conjunction with the Top Parameter Register to perform left and right shift operations to implement various MULTIPLY and DIVIDE Primitive steps. When used in such operations, it holds the lower order 16 bits of the operand while the Top Parameter Register holds the upper 16 bits.

Internal Registers: This is a group of 16 registers, each holds up to a 16-bit word (some hold less). They are preassigned as shown in the Block Diagram. These registers can be duplicated by a group of equally numbered external registers **(Shadow Registers)**, connected via the B-Port.

Program Counter: A 15-bit register/counter (P14 through P0). It holds the word address of the next instruction to be fetched from main memory.

MD Register: A 16-bit register which holds a multiplier or divisor for "math steps" of MULTIPLY, DIVIDE or SQUARE ROOT.

BC Register: A 16-bit register which is used to hold the 5-bit shift count for the barrel shifter.

SR Register: A 16-bit register which holds a special value to accomplish a SQUARE ROOT or CRC step.

PS Register: A pseudo 16-bit register which holds the configuration/status bits internal to the processor (such as carry, data cycle byte order, interrupt flag) and status bits external to the b-Port for user expansion of the definition of the machine status.

Parameter Stack Pointer: A 9-bit register which holds the address with which the Parameter Stack is accessed in a pre-increment push/post-increment pop operation.

Index Register (I): A 16-bit register which represents the top of the return stack as described in FORTH. It is decremented by the NEXT and TIMES opcodes with zero detect function to terminate these primitives.

Scratch Register (SC): A 16-bit scratch register.

LB Register: A 16-bit register which holds an offset into the "local" memory space for positioning local variables within a 32K-word segment.

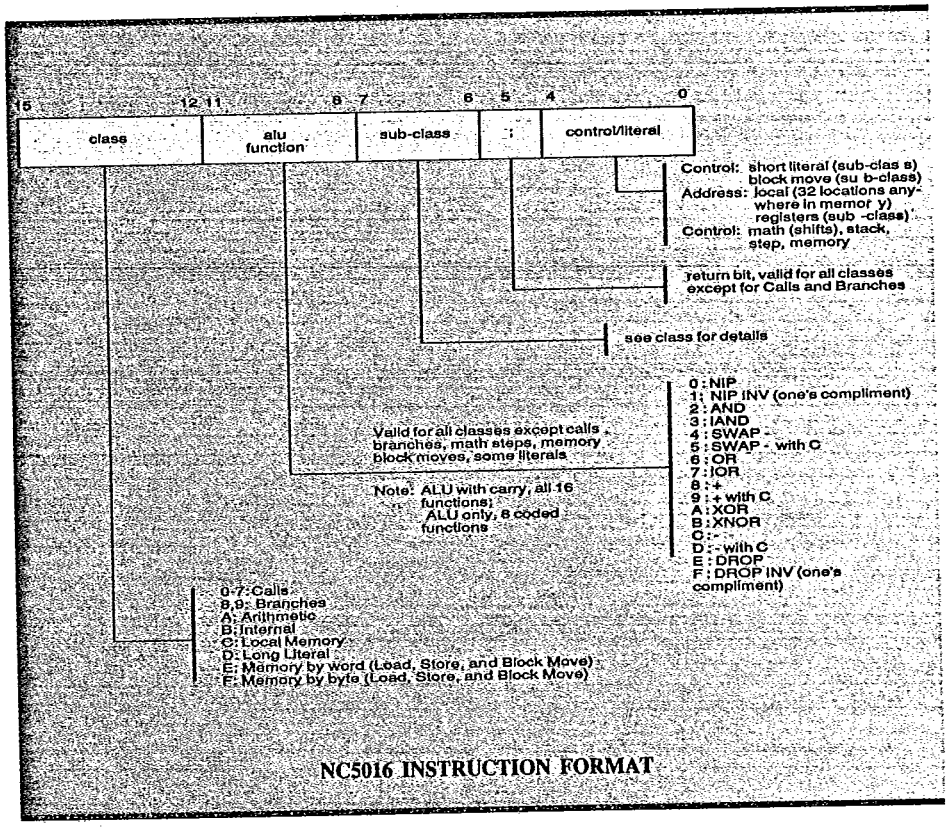
LX Register: An 8-bit segment register for defining the address extension to be used during a local variable fetch/store operation.

DX Register: An 8-bit segment register which defines the address extension to be used to access data during a local variable fetch/store operation.

CX Register: An 8-bit segment register which defines the address extension to be used to access program code and/or literal data.

SD Register: 2 bits of serial I/O plus mask, direction, and tri-state control bits for each data bit.

External Registers: (BP16 through BP31); 16 B-Port I/O locations.



NC5016 INSTRUCTION FORMAT

External Memory Spaces and Stacks

These facilities are to be provided by the user to implement a complete system. The following represents maximum capacity supported by the 144-lead version NC5016.

Main Memory: Maximum capacity of three (3) segmented spaces, each with 16 megabytes. Each space consists of 256 segments of 32K words each. A word is a 16-bit field.

Return Stack: This memory contains a maximum of 64 pages. Each page has 512 words. The pages are accessed by the User ID, RP15 through RP9. Within a page, all locations within the Return Stack are accessed with address bus RP8 through RP0.

Parameter Stack: The Parameter Stack is similar to the Return Stack in size. Pages are accessed by the User ID, (RP15 through RP9), and all locations within a page are accessed by SP8 through SP0. An external stack pointer may be accessed via SP15 through SP9, increasing the available stack depth to 64K words.

B-Port Registers: 32 16-bit registers or memory locations. The lower order 16 are assigned as shadow registers to the on chip Internal Registers; the upper order 16 are assigned as external general purpose register file. These 32 locations are accessed by the externally latched D4 through D0 of an instruction during the fetch cycle signaled by the OPS pin. These registers are provided to facilitate efficient communications between the NC5016 to other systems or subsystems provided by the user. The presence of the upper 16 locations provides general purpose facilities for holding array pointers intermediate results or constants.

Instruction Format

The NC5016 uses a very simple format for its instruction set. The 16-bit word field is divided into five (5) sub-fields as shown in the Instruction Set Diagram. These five (5) sub-fields are called Class, ALU Functions, Sub-Class, Return (;) and the Control/Literal.

Market Segments	Applications
EDP	Multi-processor systems Transaction systems Laser printer controller Background processors Expert systems Laser disk controllers Array processors
Telecommunications	Image compression Signal processing Multiplexer/Demux Satellite communications Fiber Optics controllers Voice compression Network processors PBX/PABX Echo cancellor
Industrial	Computer graphics Data acquisition Laser scanner Test/diagnostic equipment Animation/simulation Robotics and Vision systems Signal generator
Military	Communications Fault-tolerant systems Avionics
Consumer	High-end games/toys PC-turbo PC add-on (SBC)

POTENTIAL APPLICATIONS

Why Use FORTH

The choice of FORTH as the programming language executable directly by the Novix NC5016 creates an environment which is capable of providing better performance than conventional machines. The simplicity and ease of use of FORTH are major factors in its choice. FORTH is an evolving language. Unlike Basic and Fortran, FORTH is much more powerful for scientific, engineering and especially process control applications. The following illustrates this point:

1. FORTH is extremely interactive, making program debug a snap.

2. FORTH is fast and efficient, analogous to pure machine language (the NC5016 treats it as machine language). All operations are highly parallel.

3. FORTH produces highly compact code with minimum "housekeeping" necessary. Typically, FORTH requires only 30% of the memory of an equivalent Basic or Fortran system.

4. As a structured language, FORTH is highly subroutine oriented. This is further enhanced by the NC5016 hardware which supports multiple stacks.

5. FORTH uses the building block approach to programming. All of the 300 some core words in FORTH can be combined in many ways to form complex operations. This process can be extended in an unlimited fashion.

6. It is possible that an entire task can be specified by a single word definition.

FORTH is a high level language, a low level language, a compiler and an assembler.

Preliminary information, subject to change.

This product is not approved for inclusion in or to be attached to devices which are primarily used as medical devices or sub parts of medical systems.

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