G5364
G5365

Microcircuits

CMOS 8192 x 8 ROM

Features

- Low power CMOS technology
  200 μA Standby
  15 mA Operating
- Single +5 volt power supply
- Three-state data outputs
- Fully TTL compatible
- User-selected power down
- Output Enable (G5365)
- Three programmable chip selects (G5365)
- Pin compatible with 2764 EPROM (G5365)

General Description

The GTE G5364/65 Read Only Memories are 8192-word by 8-bit devices with a maximum access time of 250 nanoseconds. The devices are manufactured using the state-of-the-art CMOS process. For both devices, a manufacturing mask stage defined by the user programs the non-volatile memory.

The 5364 is packaged in a 24-pin package which offers upward compatibility with the GTE 2316 and GTE 2332 ROMs. The user has the option of a $\overline{CE}$ pin, which offers a power down feature, or a CS/$\overline{CS}$ pin, which offers faster CS access times (t_{ACS}).

The 5365 is packaged in the industry standard 28-pin package which offers campatibility with 64K EPROMs (2764). The user has the option of three user programmed CS/$\overline{CE}$ pins.

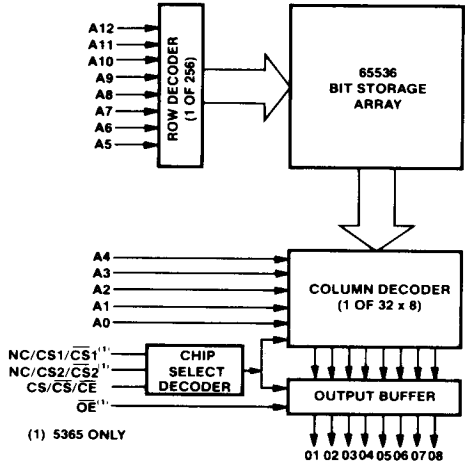
Bus-oriented application systems are catered for by the inclusion of three-state data outputs. The G5365 also provides an output enable to reduce system bus contention. The G5364/65s are available in both cerdip and plastic dual-in-line packages.

Pin Function

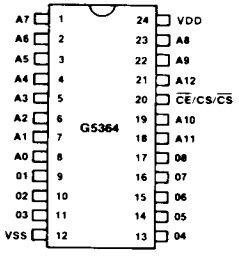
Pin	Description
A0-A12	Address
$\overline{CE}$	Chip Enable
CS/$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable

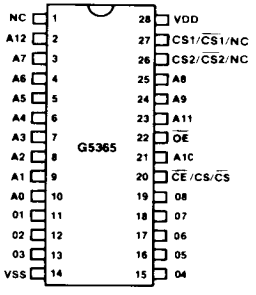
Pin	Description
01-08	Outputs
V_{DD}	+5 Volt Power Supply
V_{SS}	Ground
NC	No Connection

Block Diagram



Pin Configuration





MEMORIES

PRELIMINARY INFORMATION

Supplementary data may be published at a later date

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Voltage to Any Pin With Respect to V_{SS} (Note 9)	V_{DC}	-0.5V to 7.0V
Current Into/From Output	I_{DD}	50 mA
Operation Ambient Temp. Range	T_A	0°C to 70°C
Storage Temp. Range	T_S	-65°C to 150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

DC Characteristics: V_{DD} = 5.0V ±10%, T_A = 0°C to 70°C

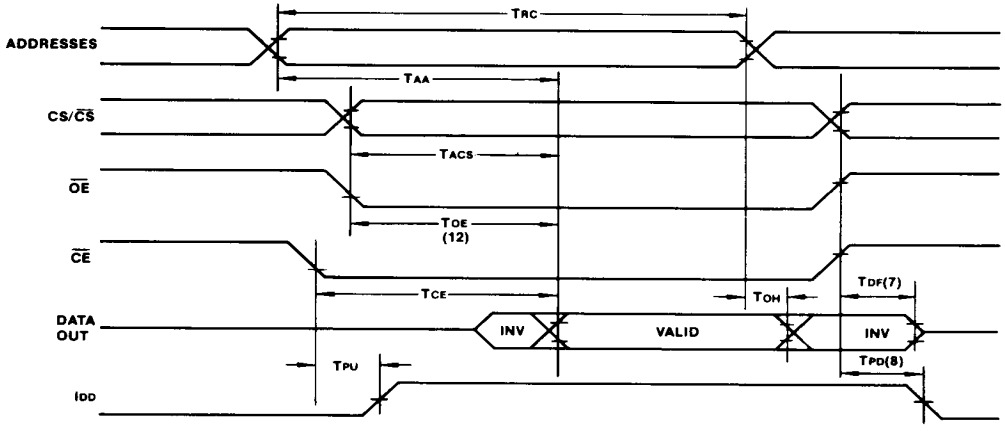
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input High Level	V_{IH}	2.0		V_{DD}	V	
Input Low Level	V_{IL}	-0.5		+0.8	V	
Input Leakage Current	I_{LI}	-10		+10	μA	Note 2
Output Leakage Current	I_{LO}	-10		+10	μA	Note 3
Output Voltage High	V_{OH}	2.4			V	I_{OH} = -220 μA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 3.3 mA
Power Supply Current (Active)	I_{DD}		6	15	mA	Note 11
Power Supply Current (Standby)	I_{DD}			200	μA	Note 6
Input Capacitance	C_{IN}		4	7	pF	Note 5
Output Capacitance	C_{OUT}		5	10	pF	V_O = 0V, Note 5

MEMORIES

AC Characteristics—Read Cycle: V_{DD} = 5.0V ±10%, T_A = 0°C to 70°C. See Notes 4, 10.

Parameter	Symbol	-25		-3		-4		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address Access Time	T_{AA}		250		300		450	nS	
Read Cycle Time	T_{RC}	250		300		450		nS	
Chip Select Access Time	T_{ACS}		100		120		150	nS	
Output Enable to Output Delay	T_{OE}		100		120		150	nS	Note 12
Chip Enable Access Time	T_{CE}		250		300		450	nS	
Power Up Time	T_{PU}	0		0		0		nS	
Data Valid After Address Change	T_{OH}	20		20		20		nS	
Chip Deselect Delay Time	T_{DF}	0	110	0	130	0	150	nS	Note 7
Power Down Time	T_{PD}		60		60		100	nS	Note 8

Timing Diagram



Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.
2. V_{IN} = 0V (V_{DD} = 5.5V)
3. Devices unselected, V_{OUT} =0V to 5.5V (V_{DD} = 5.5V)
4. Measured with two TTL loads and 100 pF (transition times = 10 nS)
5. Capacitance measured with Boonton meter or effective capacitance calculated from the equation:

   $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3.0 volts
6. $\overline{CE}$ is high, all address inputs at V_{SS} to V_{SS} + 0.5V, or V_{DD} to V_{DD} -0.5V
7. T_{DF} is specified from $\overline{OE}$, CS/$\overline{CS}$ or $\overline{CE}$ whichever occurs first.
8. T_{PD} is specified $\overline{CE}$ only
9. Output voltage minimum = -0.3V
10. Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Input timing reference level = 0.8V and 2.0V. Output timing reference = 0.8V and 2.0V.
11. Ouput load disconnected.
12. These AC characteristics are for the G5365 only.

Order Entry Information

GTE Microcircuits' preferred method of receiving a ROM code is by submittal of a set of programmed EPROM(s). Two sets of EPROMs must be submitted for each code. One set has the ROM code; the other set is blank. GTE Microcircuits will load the ROM code from the EPROM set into our computer system. This information will then be used to program the blank EPROM set, which will be sent back to the customer along with a listing of the code. The customer will approve this listing and return it to GTE.

Chip Select information must also be provided with the ROM code. For the G5364/G5365, Pin 20 may be programmed as a Chip Enable ($\overline{CE}$), high active Chip Select (CS), or a low active Chip Select ($\overline{CS}$). On the G5365, Pin 26 and Pin 27 may be programmed as a high active Chip Select (CS), low active Chip Select ($\overline{CS}$), or a No Connection (NC).

ROM code information may also be transmitted in the following optional methods:

1. ROMs
2. Paper Tape
3. Card Deck

Please consult the GTE Microcircuits factory for details.