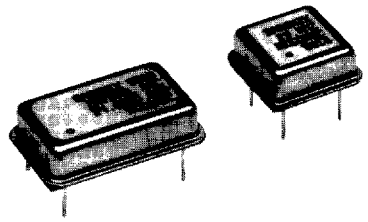
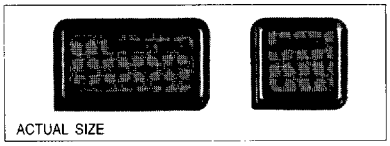
SaRonix

Crystal Clock Oscillator — CMOS

Technical Data — NCC Series





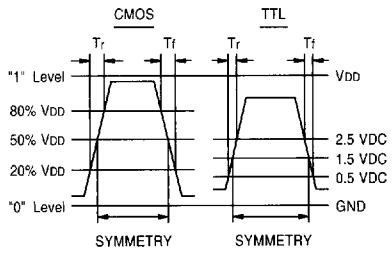
Description

A crystal controlled, low current hybrid oscillator providing precise rise and fall times to drive CMOS and NMOS microprocessors. Compatible with both CMOS and TTL. Can drive up to 2 LSTTL loads. Device is packaged in 14-pin or an 8-pin DIP compatible full size or half size, resistance welded, all metal case. Pin 7 (pin 4 for ½ size) is grounded to the case to reduce RFI.

Applications & Features

- Low power
- CMOS and TTL compatible output
- Enable/disable feature available
- Grounded, all metal full size and half size case

Output Waveform



Frequency Range:	62.5 kHz to 24 MHz (½ size - 250 kHz to 24 MHz)
Frequency Stability:	±25, ±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.
Temperature Range:	
Operating:	0°C to +70°C
Storage:	-55°C to +125°C
Supply Voltage:	
Rated:	+5 VDC ±10%
Operating:	+3 VDC min, +7 VDC max
Supply Current @ 5.0V:	(See Input Current vs. Frequency Graph, page 2)
Output Drive:	
CMOS	
Symmetry	50% ±10% @ 50% V_{DD}
Rise & Fall Times:	12ns max, 20% V_{DD} to 80% V_{DD}
Logic 0:	V_{CC} +0.5V max
Logic 1:	V_{DD} -0.5V min
Output Load:	2 CMOS
TTL	
Symmetry	50% ±10% @ 1.5V
Rise & Fall Times:	12ns max, 0.5V to 2.5V
Logic 0:	.5V max
Logic 1:	2.5V min
Output Load:	2 LSTTL
Mechanical:	
Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-202, Method 211, Conditions A and C
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition B
Environmental:	
Gross Leak Test:	MIL-STD-883, Method 1014, Condition C
Fine Leak Test:	MIL-STD-883, Method 1014, Condition A2 <5 x 10^{-8} ATM cc/sec
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

Part Numbering Guide

NCC 060 C E — 4.0000

Type

Model
030 = 62.5 kHz ~ 3.9999 MHz, Full Size
060 = 4 MHz ~ 24 MHz, Full Size
039 = 250 kHz ~ 3.9999 MHz, Half Size
069 = 4 MHz ~ 24 MHz, Half Size

Stability Tolerance
A = ±25 ppm (0.0025%)
B = ±50 ppm (0.005%)
C = ±100 ppm (0.010%)

Blank = No Enable/Disable
E = Enable/ Disable

Frequency (MHz)

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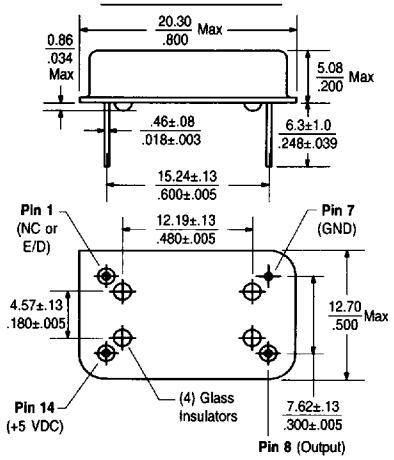
Technical Data

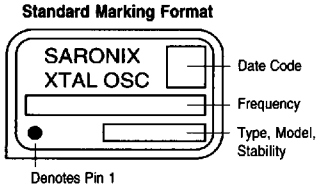
NCC Series

Package Details

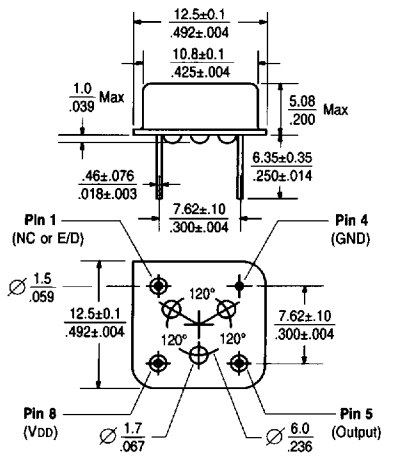
FULL SIZE PACKAGE



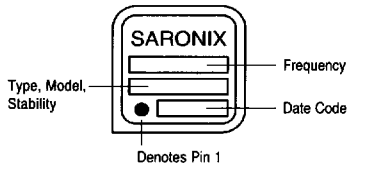
Standard Marking Format



HALF SIZE PACKAGE

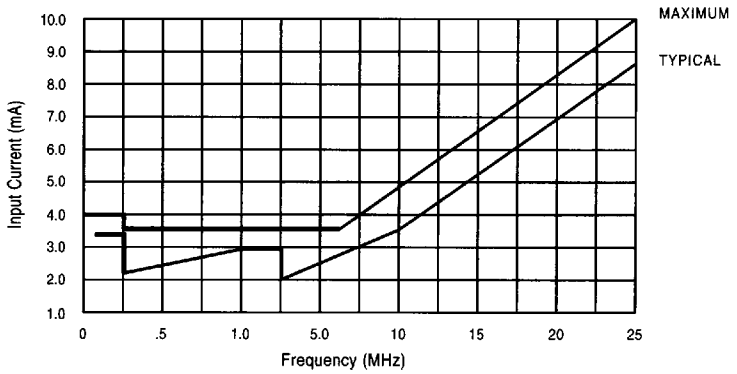


Standard Marking Format

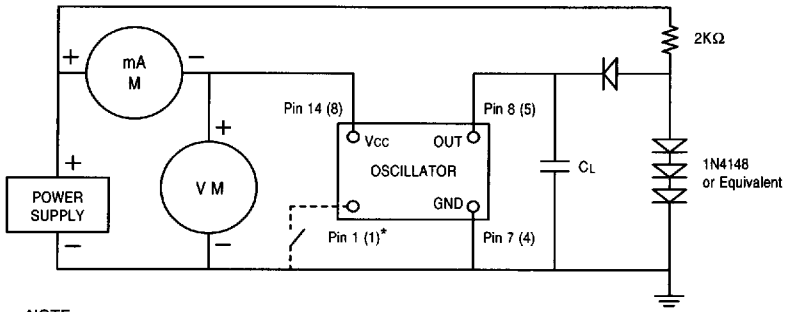


Scale: None (Dimensions in $\frac{mm}{inches}$)

Input Current vs. Frequency at +5.0V

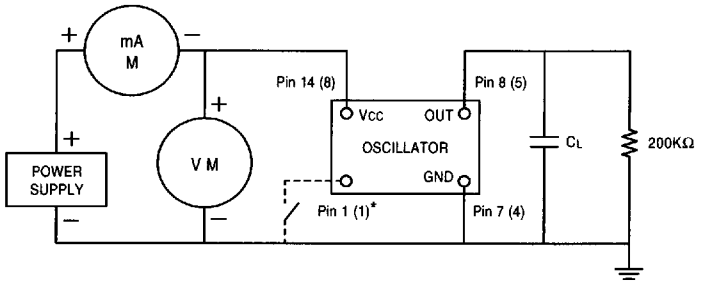


Test Circuits



NOTE:
C_L = 15 pF max (Includes probe and fixture capacitance)
Pin 1 = No connection or Enable/Disable function optional (Enable = "1" level, Disable = "0" level).
*( ) Indicates pin numbers for half-size package

TTL TEST CIRCUIT (used by SaRonix)



NOTE:
C_L = 15 pF max (Includes probe and fixture capacitance)
Pin 1 = No connection or Enable/Disable function optional (Enable = "1" level, Disable = "0" level).
*( ) Indicates pin numbers for half-size package

CMOS TEST CIRCUIT (Optional)

49372 Y

All specifications are subject to change without notice.

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2